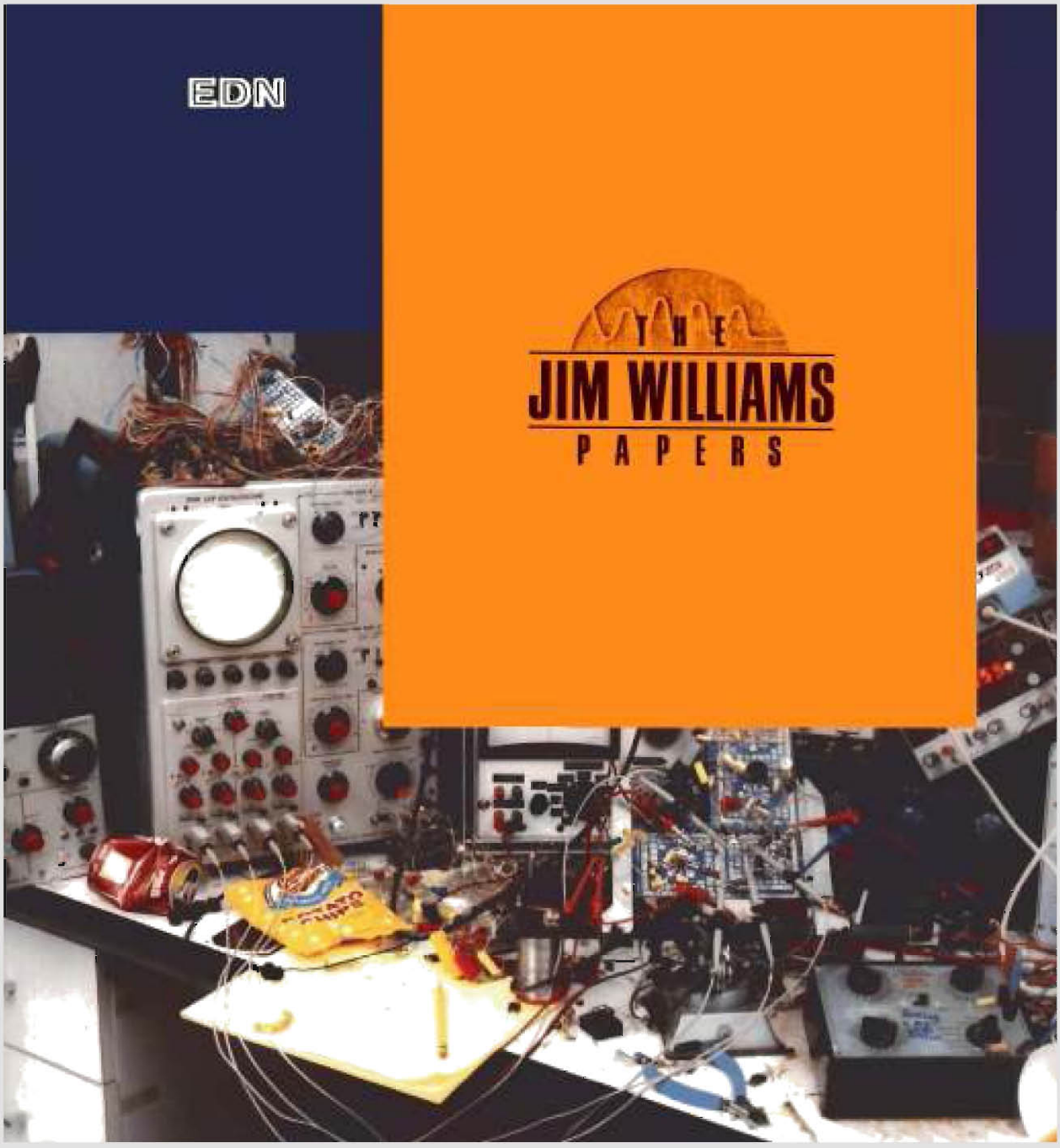
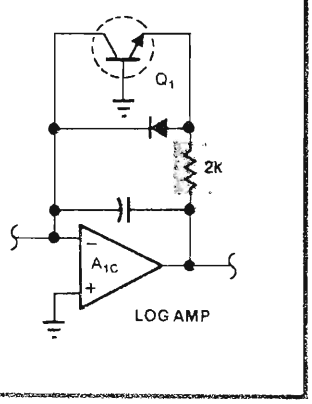
A Tribute to Jim Williams

EDN – 1 (1980-1989)



Breaking up a log jam

An error of omission converted an accurate logarithmic amplifier into a hard limiter in Jim Williams' humidity-measurement circuit (EDN, June 5, pg 149). If you've wondered where the range went, try adding a 2-kΩ resistor as shown; it will unjam the amp.



A few proven techniques ease sine-wave-generator design

Perhaps the most fundamental of all signals, sine waves present generating-circuit design tasks that are anything but fundamental. Next time you design such a circuit—whether it's for 1 Hz or 1 MHz—try one of the techniques described here.

Jim Williams, National Semiconductor Corp

Because sine-wave oscillators come in as many forms as the units that use them, choosing the best circuit type and implementation for an application can prove difficult. This article, however, helps simplify those choices and furnishes guidelines for controlling critical design specs such as frequency, amplitude and distortion.

You can apply many analog and digital techniques to achieve your sine-wave-generator design goals; each realization offers unique strengths and weaknesses. You'll probably find that one of those listed in the **table** will meet your requirements. The specific circuit

SINE-WAVE-GENERATION TECHNIQUES

TYPE	TYPICAL FREQUENCY RANGE	TYPICAL DISTORTION (%)	TYPICAL AMPLITUDE STABILITY (%)	COMMENTS
PHASE SHIFT	10 Hz-1 MHz	1-3	3 (TIGHTER WITH SERVO CONTROL)	SIMPLE, INEXPENSIVE TECHNIQUE. EASILY AMPLITUDE SERVO CONTROLLED. RESISTIVELY TUNABLE OVER 2:1 RANGE WITH LITTLE TROUBLE. GOOD CHOICE FOR COST-SENSITIVE, MODERATE-PERFORMANCE APPLICATIONS. QUICK STARTING AND SETTLING.
WEIN BRIDGE	1 Hz-1 MHz	0.01	1	EXTREMELY LOW DISTRORTION. EXCELLENT FOR HIGH-GRADE INSTRUMENTATION AND AUDIO APPLICATIONS. RELATIVELY DIFFICULT TO TUNE—REQUIRES DUAL VARIABLE RESISTOR WITH GOOD TRACKING. TAKES CONSIDERABLE TIME TO SETTLE AFTER A STEP CHANGE IN FREQUENCY OR AMPLITUDE.
LC NEGATIVE RESISTANCE	1 kHz-10 MHz	1-3	3	DIFFICULT TO TUNE OVER WIDE RANGES. HIGHER Q THAN RC TYPES. QUICK STARTING AND EASY TO OPERATE IN HIGH FREQUENCY RANGES.
TUNING FORK	60 Hz-3 kHz	0.25	0.1	FREQUENCY-STABLE OVER WIDE RANGES OF TEMPERATURE AND SUPPLY VOLTAGE. RELATIVELY UNAFFECTED BY SEVERE SHOCK OR VIBRATION. BASICALLY UNTUNABLE.
CRYSTAL	30 kHz-200 MHz	0.1	1	HIGHEST FREQUENCY STABILITY. ONLY SLIGHT (PPM) TUNING POSSIBLE. FRAGILE
TRIANGLE-DRIVEN BREAK-POINT SHAPER	<1 Hz-500 kHz	1-2	1	WIDE TUNING RANGE POSSIBLE WITH QUICK SETTLING TO NEW FREQUENCY OR AMPLITUDE.
TRIANGLE-DRIVEN LOGARITHMIC SHAPER	<1 Hz-500 kHz	0.3	0.25	WIDE TUNING RANGE WITH QUICK SETTLING TO NEW FREQUENCY OR AMPLITUDE. TRIANGLE AND SQUARE WAVE ALSO AVAILABLE. EXCELLENT CHOICE FOR GENERAL-PURPOSE REQUIREMENTS NEEDING FREQUENCY-SWEEP CAPABILITY WITH LOW-DISTORTION OUTPUT.
DAC-DRIVEN LOGARITHMIC SHAPER	<1 Hz-500 kHz	0.3	0.25	SIMILAR TO ABOVE BUT DAC-GENERATED TRIANGLE WAVE GENERALLY EASIER TO AMPLITUDE-STABILIZE OR VARY. ALSO, DAC CAN BE ADDRESSED BY COUNTERS SYNCHRONIZED TO A MASTER SYSTEM CLOCK.
ROM-DRIVEN DAC	1 Hz-20 MHz	0.1	0.01	POWERFUL DIGITAL TECHNIQUE THAT YIELDS FAST AMPLITUDE AND FREQUENCY SLEWING WITH LITTLE DYNAMIC ERROR CHIEF DETRIMENTS ARE REQUIREMENT FOR HIGH-SPEED CLOCK (EG, 8-BIT DAC REQUIRES A CLOCK THAT IS 256 × OUTPUT SINE-WAVE FREQUENCY) AND DAC GLITCHING & SETTLING, WHICH WILL INTRODUCE SIGNIFICANT DISTORTION AS OUTPUT FREQUENCY INCREASES.

1-IC Wein-bridge oscillators provide low-distortion signals

examples presented in this article, implementing the design techniques summarized in the **table,** demonstrate how easy it is to design a sine-wave source and achieve the kind of performance you need.

Phase-shift oscillators operate simply

Fig 1 depicts a 1-IC, 1-supply, amplitude-stabilized, phase-shift sine-wave oscillator. The LM389 audio-power-amplifier package contains the three discrete npn transistors shown (Q_1 through Q_3) in addition to the amplifier. Q_2 and the RC network constitute a phase-shift configuration that oscillates at about 12 kHz. The remaining circuitry provides amplitude stability.

The high-impedance output at Q_2's collector drives the LM389 amplifier's input via the 10-μF, 1-MΩ series network; the 1-MΩ resistor, in combination with the LM389 amplifier's internal 50-kΩ resistance, divides Q_2's output by 20—necessary because the amplifier has a fixed gain of 20. In this manner, the amplifier functions as a unity-gain current buffer capable of driving an 8Ω load.

The amplifier's positive output peaks are rectified and stored in the 5-μF capacitor, and the resulting potential then feeds to Q_3's base. As a result, Q_3's collector current varies with the difference between its base and emitter voltages. Because the LM313 1.2V reference fixes the emitter voltage, Q_3 performs a comparison function and utilizes its collector current to modulate Q_1's base voltage. Q_1 (an emitter follower) provides servo-controlled drive to the Q_2 oscillator.

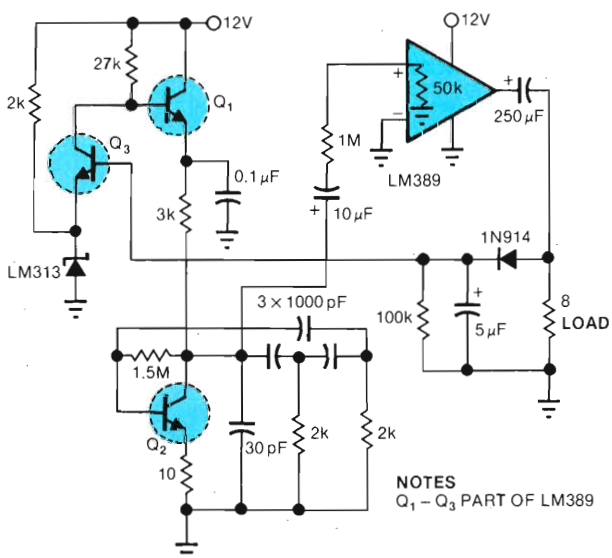


Fig 1—Phase-shift sine-wave oscillators *combine simplicity with versatility. This 12-kHz design can deliver 5V p-p to the 8Ω load with about 2% distortion.*

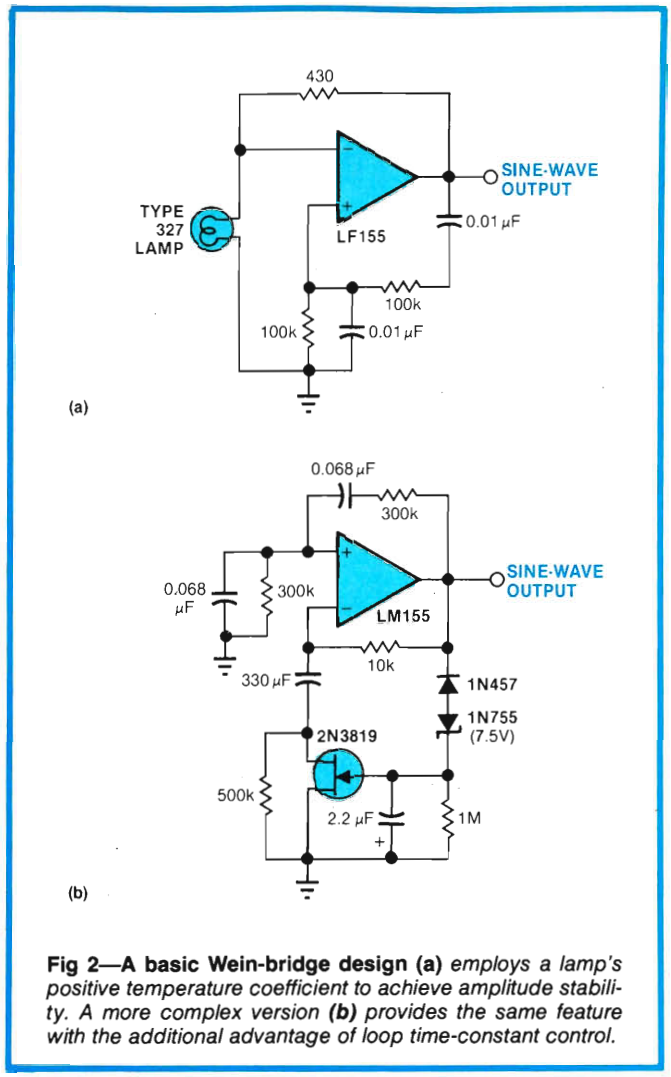


Fig 2—A basic Wein-bridge design (a) *employs a lamp's positive temperature coefficient to achieve amplitude stability. A more complex version* ***(b)*** *provides the same feature with the additional advantage of loop time-constant control.*

Note that you can realize an amplitude-control function with this circuit if you open Q_3's emitter and drive it with an external voltage. The LM389 output can deliver 5V p-p (1.75V rms) into an 8Ω load with about 2% distortion. A ±3V power-supply variation causes less than ±0.1-dB amplitude shift at the output.

A Wein bridge yields low distortion

In many applications, a phase-shift oscillator's distortion levels become unacceptable. A Wein bridge, however, can provide very low distortion levels. With this configuration, stable oscillation can occur only if loop gain remains at unity at the oscillation frequency. The circuit depicted in **Fig 2a** achieves this control by using a small lamp's positive temperature coefficient to regulate gain as the oscillator output attempts to vary—a classic technique for achieving low distortion that's been used by numerous circuit designers (including William Hewlett and David Packard, who built a few of this type of circuit in a Palo Alto garage about 40 yrs ago). The smooth limiting action of the bulb, in combination with the Wein network's near-ideal characteristics, yields very high performance.

The circuit shown in **Fig 2b** indicates how an electronic equivalent of a light bulb can also control loop gain. The zener diode determines output amplitude,

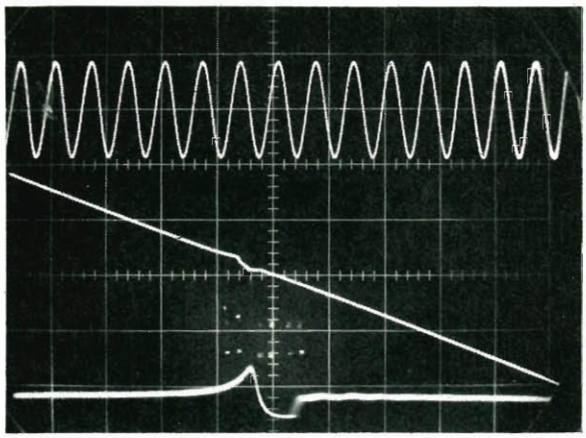
and the 1-MΩ/2.2-μF combination sets the loop time constant. The 2N3819 FET, biased by the voltage across the 2.2-μF capacitor, controls ac loop gain by shunting the oscillator's feedback path. This circuit is more complex than the one diagrammed in **Fig 2a,** but it offers a way to control the loop time constant while maintaining almost the same distortion performance.

Fig 3 shows the performance of the **Fig 2a** circuit. The upper trace is the oscillator's output, and the middle trace shows that waveform's downward slope, greatly expanded. The slight aberration in the latter results from crossover distortion in the FET-input LF155, distortion almost totally responsible for the design's measured 0.01% distortion level. A distortion analyzer's output appears in the bottom trace.

You can achieve high voltages, too

Another dimension in sine-wave-oscillator design is stable amplitude control. In **Fig 4**'s oscillator version, not only does servo control stabilize the amplitude, but the servo loop includes voltage gain.

The circuit's ability to produce a 100V rms output stabilized to 0.025% demonstrates the technique's value. Although complex in appearance, the circuit requires only three IC packages. An LS-52 audio transformer provides voltage gain within a tightly controlled servo loop, and the LM3900 Norton amplifiers constitute a 1-kHz amplitude-controllable oscillator. The LH0002 buffer furnishes low-impedance drive to the transformer. By driving the transformer's secondary and taking the ouput from the primary, the circuit achieves a voltage gain of 100.



TRACE	VERTICAL	HORIZONTAL
TOP	10V/DIV	10 mSEC/DIV
MIDDLE	1V/DIV	500 NSEC/DIV
BOTTOM	0.5V/DIV	500 NSEC/DIV

Fig 3—Low-distortion output (top trace) *is a Wein-bridge-oscillator feature. The very low crossover-distortion level (middle) results from the LF155's output stage. A distortion analyzer's output signal (bottom) indicates this design's 0.01% distortion level.*

A current-sensitive negative-absolute-value amplifier—composed of two amplifiers in an LF347 quad—generates a negative, rectified feedback signal. The third LF347 amplifier (A_7) compares this signal with the LM329 dc reference and amplifies the

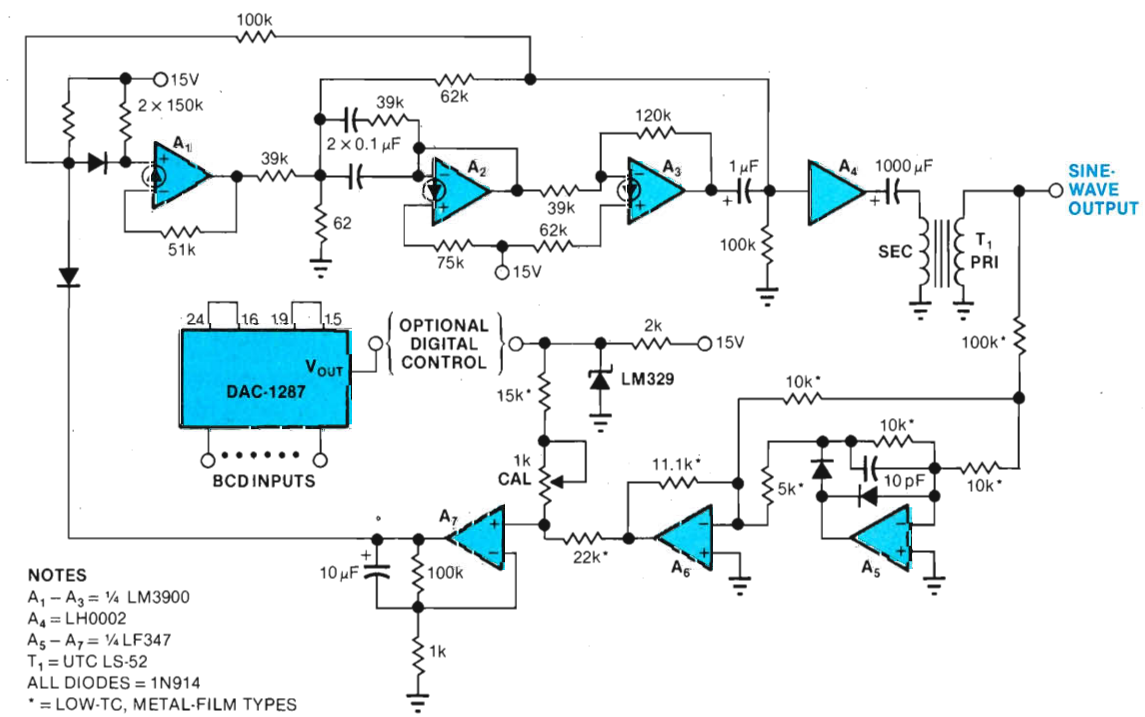


Fig 4—Generate high-voltage sine waves *using IC-based circuits by driving a transformer in a step-up mode. You can realize digital amplitude control by replacing the LM329 voltage reference with the DAC1287.*

Combining Ls, Cs and a few ICs yields high-stability sine waves

difference at a gain of 100. The 10-μF feedback capacitor sets the loop's frequency response. This stage's output controls the amplitude of the LM3900 oscillator, thereby closing the loop.

As shown, the circuit oscillates at 1 kHz with less than 0.1% distortion for a 100V rms (285V p-p) output. If you replace the summing resistors from the LM329 with a potentiometer, you can adjust the loop to remain stable for output settings ranging from 3 to 190V rms (542V p-p) with no frequency change. And if a DAC1287 D/A converter replaces the LM329 reference, a digital input code can control the ac output voltage with 3-digit calibrated accuracy.

Combine L, C and negative R for stability

All of the circuits presented so far rely on RC time constants to achieve resonance. But LC combinations can also serve and offer good frequency stability, high Q and fast starting.

A negative-resistance LC sine-wave oscillator appears in **Fig 5**, for example. The Q_1, Q_2 pair provides a 15-μA current source; Q_2's collector current in turn sets Q_3's peak collector current. The 300Ω pot and the Q_4, Q_5

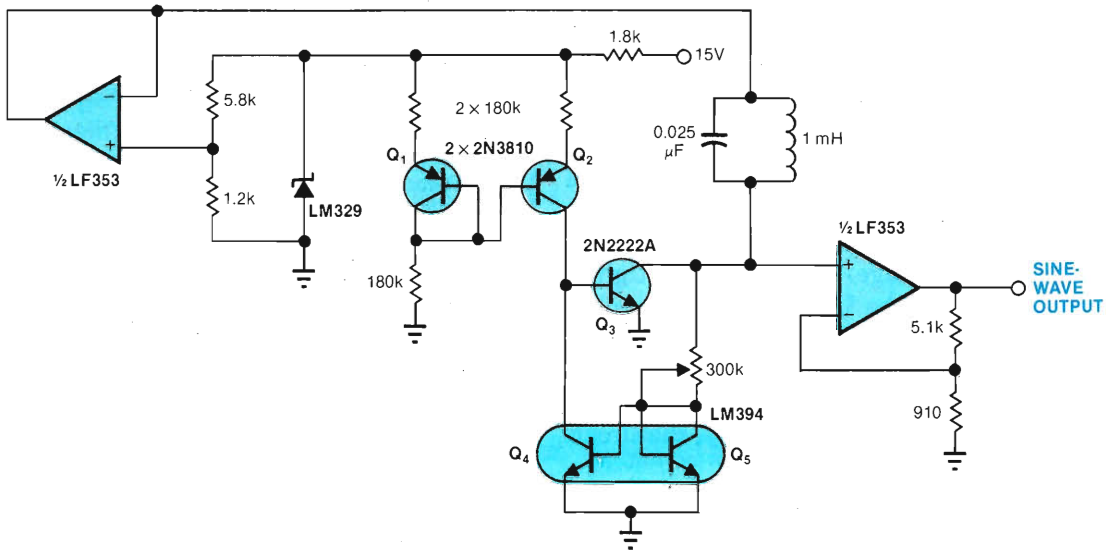


Fig 5—LC sine-wave sources *offer high stability and reasonable distortion levels. Transistors Q_1 through Q_5 implement a negative-resistance amplifier. The LM329, LF353 combination eliminates power-supply dependence.*

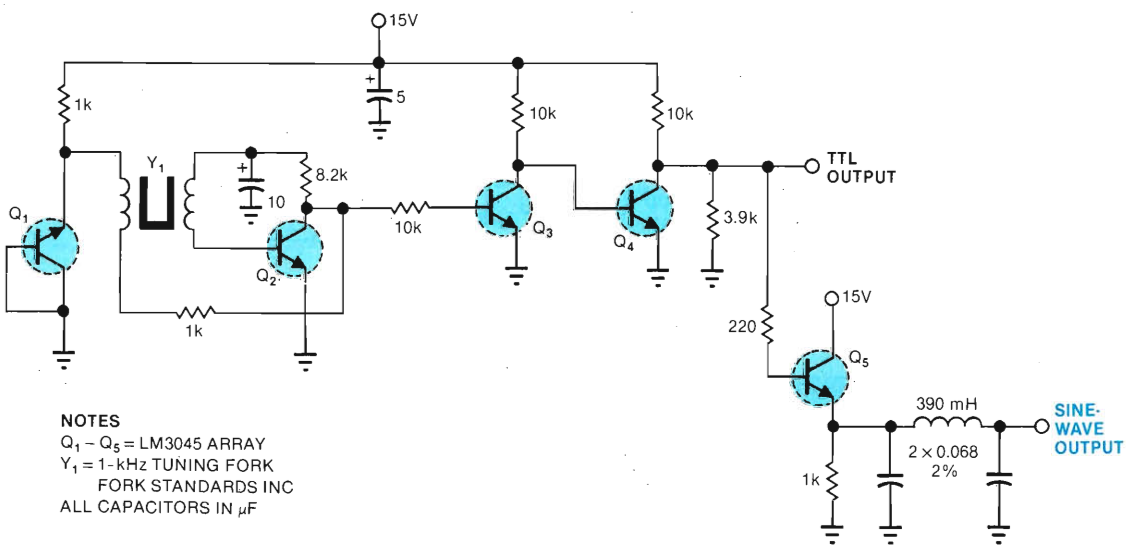


Fig 6—Tuning-fork-based oscillators *don't inherently produce sinusoidal outputs. But when you do use them for this purpose, you achieve maximum stability when the oscillator stage (Q_1, Q_2) limits. Q_3 and Q_4 provide a TTL-compatible signal, which Q_5 then converts to a sine wave.*

LM394 matched pair accomplish a voltage-to-current conversion that decreases Q_3's base current when this transistor's collector voltage rises—a process that furnishes the negative-resistance characteristic that permits oscillation.

The LC circuit in the Q_3, Q_5 collector line determines the oscillator circuit's operating frequency, and the LF353 FET amplifier provides gain and buffering. An LM329 zener diode and LF353 unity-gain follower eliminate power-supply dependence. This circuit starts quickly, and distortion remains within 1.5%.

Tuning forks offer another approach

Although oscillators for many applications can rely on combinations of passive components—whether RC or LC—to achieve resonance at the oscillation frequency, some circuits must utilize inherently resonant elements to achieve very high frequency stability. Such oscillators can generate stable low-frequency outputs under high-mechanical-shock conditions that would fracture quartz crystals.

In **Fig 6**'s circuit, for instance, a tuning fork works in a feedback loop with one of the transistors (Q_2) in an LM3045 array to achieve a stable 1-kHz output. Zener-connected Q_1 performs a combined reference and signal-limiting function. And because the oscillator is allowed to limit—a conventional technique in fork designs—it doesn't require amplitude stabilization. Q_3 and Q_4 speed up the oscillator's signal edges and furnish a TTL-compatible output level. Emitter follower Q_5 then drives an LC filter to produce a sine-wave output.

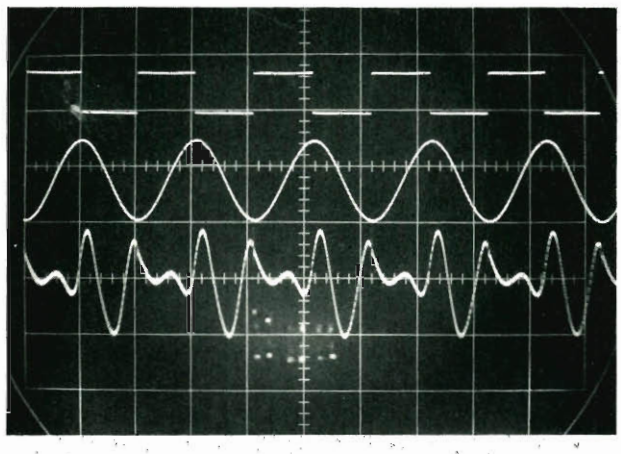
Fig 7 shows the circuit's TTL and sine-wave outputs. The 0.7% sine-wave distortion displayed in the bottom trace is a distortion analyzer's output signal.

Quartz crystals furnish high-frequency stability

If an application demands high-frequency stability—higher than a tuning-fork circuit can deliver—in the face of changing power-supply and temperature parameters, try a quartz-crystal oscillator. **Fig 8a** shows a simple example of a 100-kHz crystal oscillator—a Colpitts-class circuit that improves stability by using a JFET for low crystal loading. Voltage regulation eliminates the small effects (less than 5 ppm for a 20% shift) introduced by supply variations. And shunting the crystal with small-value capacitors allows very fine frequency trimming.

Crystals typically drift less than 1 ppm/°C, and temperature-controlled ovens can eliminate even this variation (**Fig 8b**). The RC feedback values depend upon the thermal time constants of the oven used; the values shown are typical. Set oven temperature to coincide with the crystal's zero temperature coefficient or "turning-point" temperature, which the manufacturer specifies.

An alternative to temperature control (**Fig 8c**) places a varactor diode across the crystal. The varactor receives its bias via a temperature-dependent voltage from a circuit similar to the one shown in **Fig 8b** but without the output transistor. As ambient temperature



TRACE	VERTICAL	HORIZONTAL
TOP	5V/DIV	
MIDDLE	50V/DIV	500 μSEC/DIV
BOTTOM	0.2V/DIV	

Fig 7—Various output levels *are provided by the tuning-fork oscillator shown in* ***Fig 6.*** *This design easily produces a TTL-compatible signal (top trace) because the oscillator is allowed to limit. Low-pass filtering this square wave generates a sine wave (middle). The oscillator's 0.7% distortion level is indicated (bottom) by an analyzer's output.*

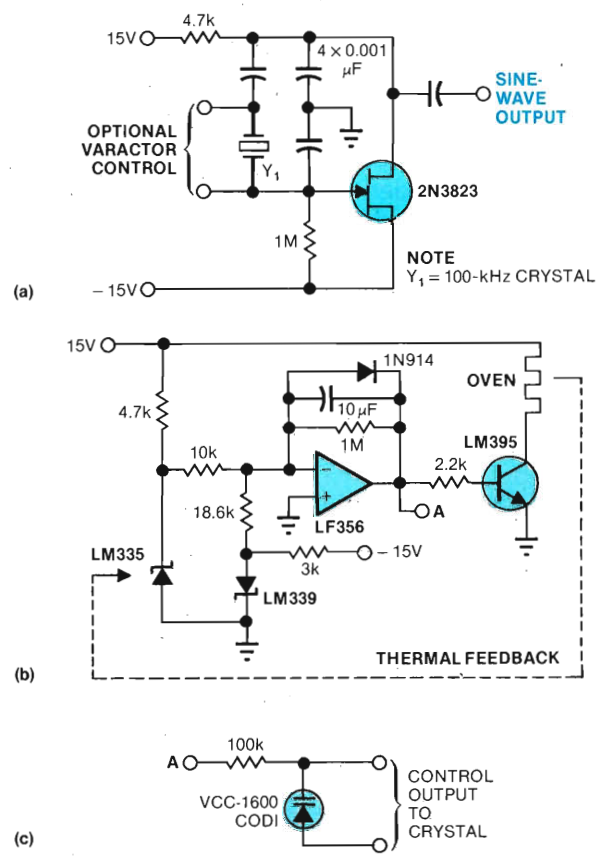


Fig 8—Stable quartz-crystal oscillators *can operate with a single active device* ***(a).*** *You can achieve maximum frequency stability by mounting the oscillator in an oven and using a temperature-controlling circuit* ***(b).*** *A varactor network* ***(c)*** *can also accomplish crystal fine tuning. Here, the varactor replaces the oven and retunes the crystal by changing its load capacitances.*

varies, the circuit changes the voltage across the varactor, which in turn changes its capacitance. This capacitance shift trims the oscillator frequency.

Approximate sine waves

With the exception of the tuning-fork design, all of the preceding circuits operate as *inherent* sine-wave generators: Their normal operating mode supports and maintains a sinusoidal characteristic. Another oscillator class consists of circuits that *approximate* the sine function using a variety of techniques—usually a more complex approach but one that offers increased versatility in controlling amplitude and oscillation frequency. The adaptability of digital controls to these circuit types has markedly increased their popularity.

As an example, **Fig 9** diagrams a circuit that shapes a 20V p-p triangle-wave input into a sine-wave output. The two amplifiers in the center of the circuit establish stable bias potentials for the diode shaping network, which operates by turning individual diodes on or off depending upon the input triangle's amplitude. This action changes the output amplifier's gain and gives the circuit its characteristic nonlinear, shaped-output response. The values of the resistors associated with the diodes determine the shaped waveform's appearance. And note that individual diodes in the dc-bias circuitry provide first-order temperature compensation for the shaper diodes.

Fig 10 depicts the circuit's performance. Trace A is the filtered output (note the 1000-pF capacitor across the **Fig 9** circuit's output amplifier), and trace B shows the waveform with no filtering. In B, you can barely detect a breakpoint at the top and bottom of the waveform, but all the breakpoints become clearly identifiable in the distortion-analyzer output (trace C). Note that in **Fig 9**'s circuit, if the amplitude or symmetry of the input triangle wave shifts, the output waveform degrades badly. Typically, you can employ a D/A converter to provide input drive. Distortion in this circuit specs below 1.5% when filtered and about 2.7% without filtering.

Log shaping yields 10,000:1 frequency range

Applications that call for a wide frequency range can make good use of the shaper circuit shown in **Fig 11,** a complete sine-wave generator that you can tune from 1 Hz to 10 kHz using one variable resistor. Amplitude stability remains within 0.02%/°C, and distortion measures 0.35%. In addition, desired frequency shifts occur instantaneously because no control-loop time constants apply.

The circuit works by placing an integrator inside a comparator's positive feedback loop to produce triangle waves for shaping into sine waves. The LM311 drives a symmetrical temperature-compensated clamp arrangement, which then biases the LF356 integrator. The LF356 integrates this current into a linear ramp. At the 311's input, this ramp is summed with the clamp's output until the ramp voltage nulls out the bound voltage. At this time, the comparator changes state and the integrator output reverses.

The resultant repetitive triangle waveform then feeds to a sine-shaper section that utilizes the nonlinear, logarithmic relationship between V_{BE} and the collector current in the transistors to smooth the triangle wave. The LM394 dual transistor handles the actual shaping, while the 2N3810 provides current drive. The LF351 allows adjustable, low-impedance output-amplitude control.

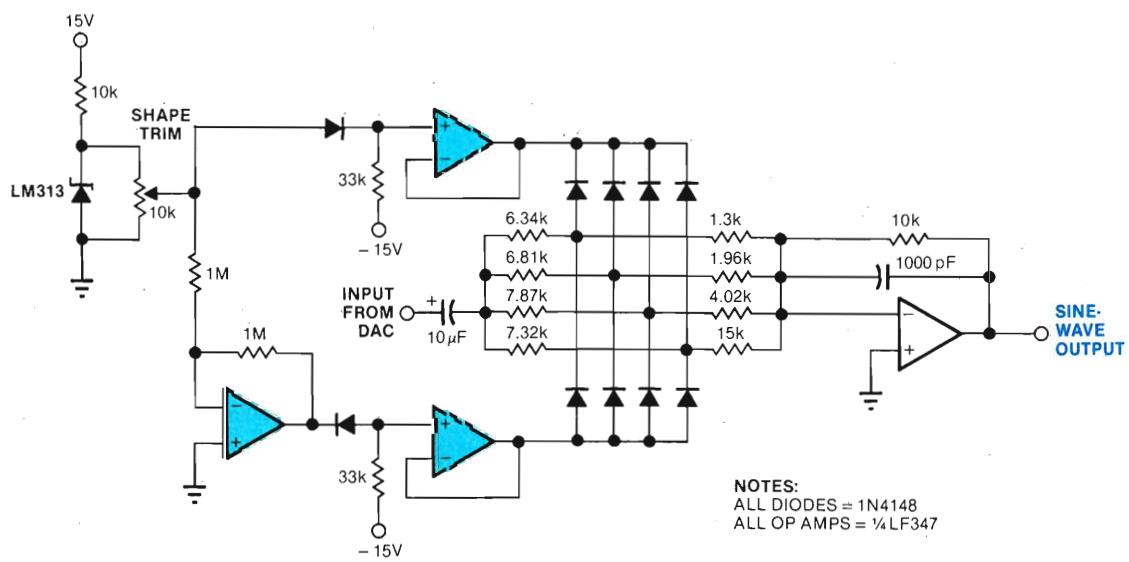
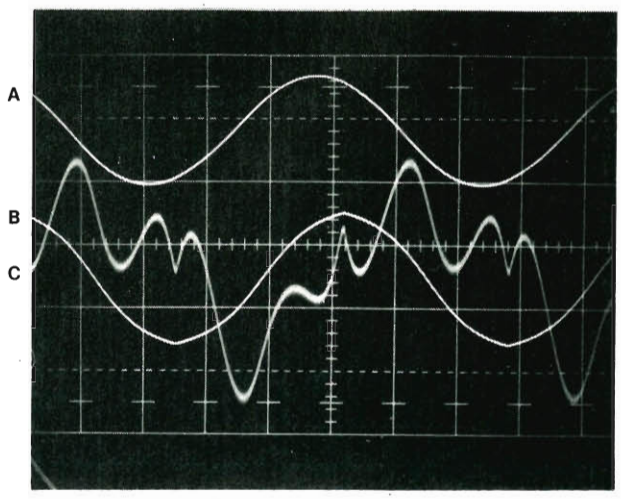
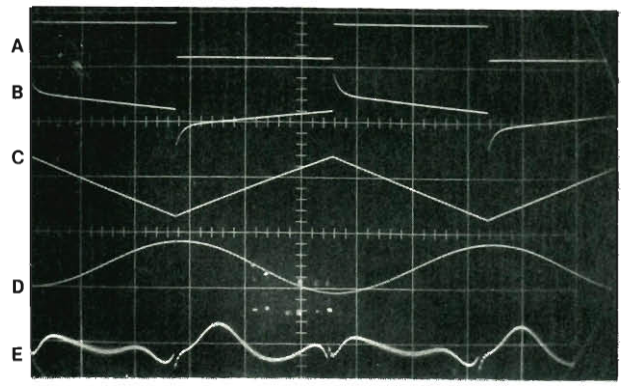


Fig 9—Breakpoint-shaping networks *employ diodes that conduct in direct proportion to an input triangle wave's amplitude. This action changes the output amplifier's gain to produce the sine function.*



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	
B	5V/DIV	20 μSEC/DIV
C	0.5V/DIV	

Fig 10—A clean sine wave results (trace A) *when* ***Fig 9****'s circuit's output includes a 1000-pF capacitor. When the capacitor isn't used, the diode network's breakpoint action becomes apparent (trace B). The distortion analyzer's output (trace C) clearly shows all the breakpoints.*



TRACE	VERTICAL	HORIZONTAL
A	20V/DIV	
B	20V/DIV	20 μSEC/DIV
C	10V/DIV	
D	10V/DIV	
E	0.5V/DIV	

Fig 12—Logarithmic shapers *can utilize a variety of circuit waveforms. The input to the LF356 integrator* ***(Fig 11)*** *appears here as trace A. The LM311's input (trace B) is the summed result of the integrator's triangle output (C) and the LM329's clamped waveform. After passing through the 2N3810/LM394 shaper stage, the resulting sine wave is amplified by the LF351 (D). A distortion analyzer's output (E) represents a 0.35% total harmonic distortion.*

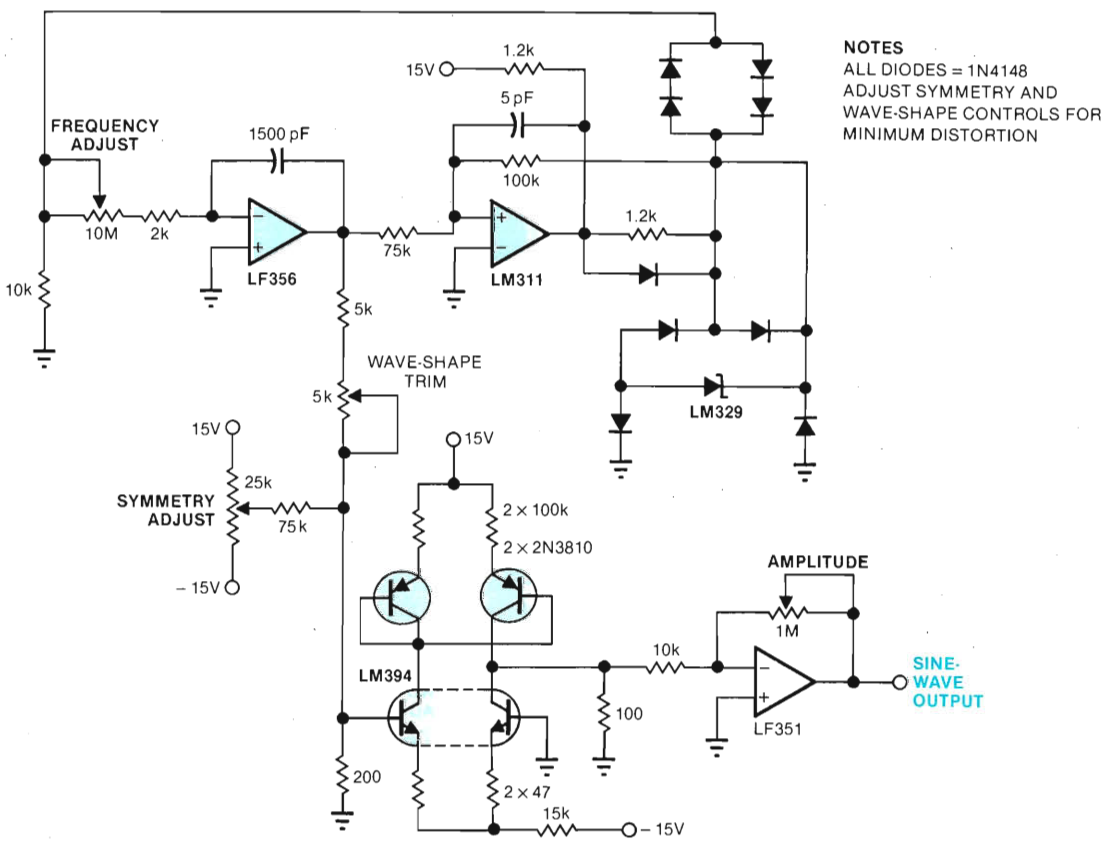


Fig 11—Logarithmic shaping schemes *produce a sine-wave oscillator that you can tune from 1 Hz to 10 kHz with a single control. Additionally, you can shift frequencies rapidly because the circuit contains no control-loop time constants.*

Digital techniques implement analog sine-wave sources

Typical circuit waveforms appear in **Fig 12.** Should you need an even wider frequency range than that provided by this circuit, bear in mind that more sophisticated versions (**references**) achieve operation from 1 Hz to 1 MHz while retaining the single-frequency-control feature.

Electronic tuning brings speed

A very-high-performance version of **Fig 11**'s log shaper design appears in **Fig 13.** Here, the LF356 integrator's input voltage is an externally supplied control voltage, rather than the zener-bridge output previously used. Inverted by the LF351, the control voltage is gated by the 2N4392 FET switches, which are in turn controlled by the LM311's output. Thus, oscillator frequency varies directly with the input control voltage. And because limiting rather than a servo-loop process determines the circuit's amplitude, an almost instantaneous frequency change occurs as the result of a step input.

A 10V input sweeps the oscillator from 1 Hz to 30 kHz with less than 0.4% distortion (**Fig 14**). Additionally, control-voltage input vs frequency-output linearity lies within 0.25%.

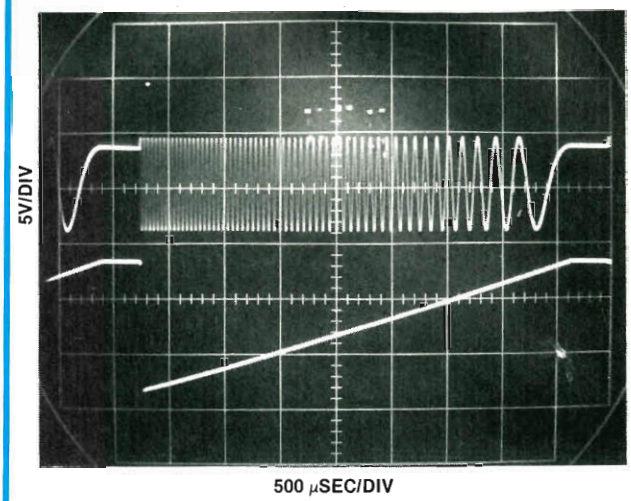


Fig 14—Rapid frequency sweeping *is an inherent feature of* ***Fig 13****'s voltage-controlled sine-wave oscillator. You can sweep this VCO from 1 Hz to 30 kHz with a 10V input signal; the output settles quickly.*

Digital techniques make analog sine waves

You can also use digital methods to approximate a sine wave. But, although they offer greater flexibility, it's only at the cost of an increase in complexity. **Fig 15,** for instance, shows a 10-bit D/A-converter IC driven by up/down counters to deliver an amplitude-stable triangle current into the LF357 FET amplifier. The LF357 then drives a shaper circuit of the type shown in **Fig 9.** The sine wave's amplitude remains stable, and its frequency depends solely on the clock speed used to drive the counters. If the clock is crystal controlled, the output sine wave reflects the crystal's high frequency stability. In this example, 10 binary bits drive the DAC, so the output frequency equals $1/1024$ of the clock frequency.

If you insert a sine-coded ROM between the counter outputs and the DAC, you can eliminate the sine shaper

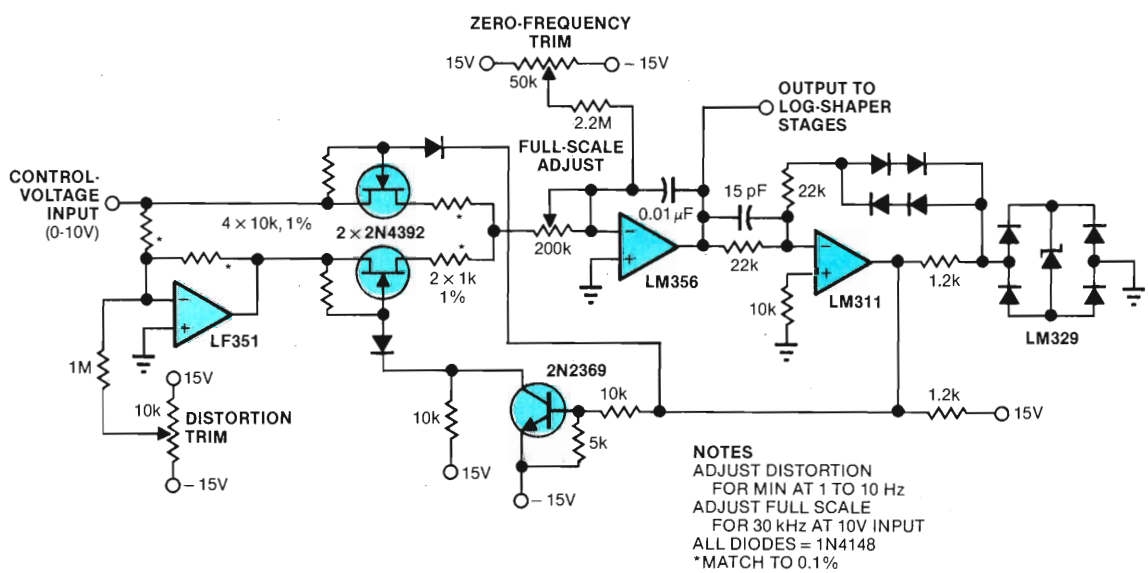


Fig 13—A voltage-tunable oscillator *results when* ***Fig 11****'s design is modified to include signal-level-controlled feedback. Here, FETs switch the integrator's input so that the resulting summing-junction current is a function of the input control voltage. This scheme realizes a frequency range of 1 Hz to 30 kHz for a 0 to 10V input.*

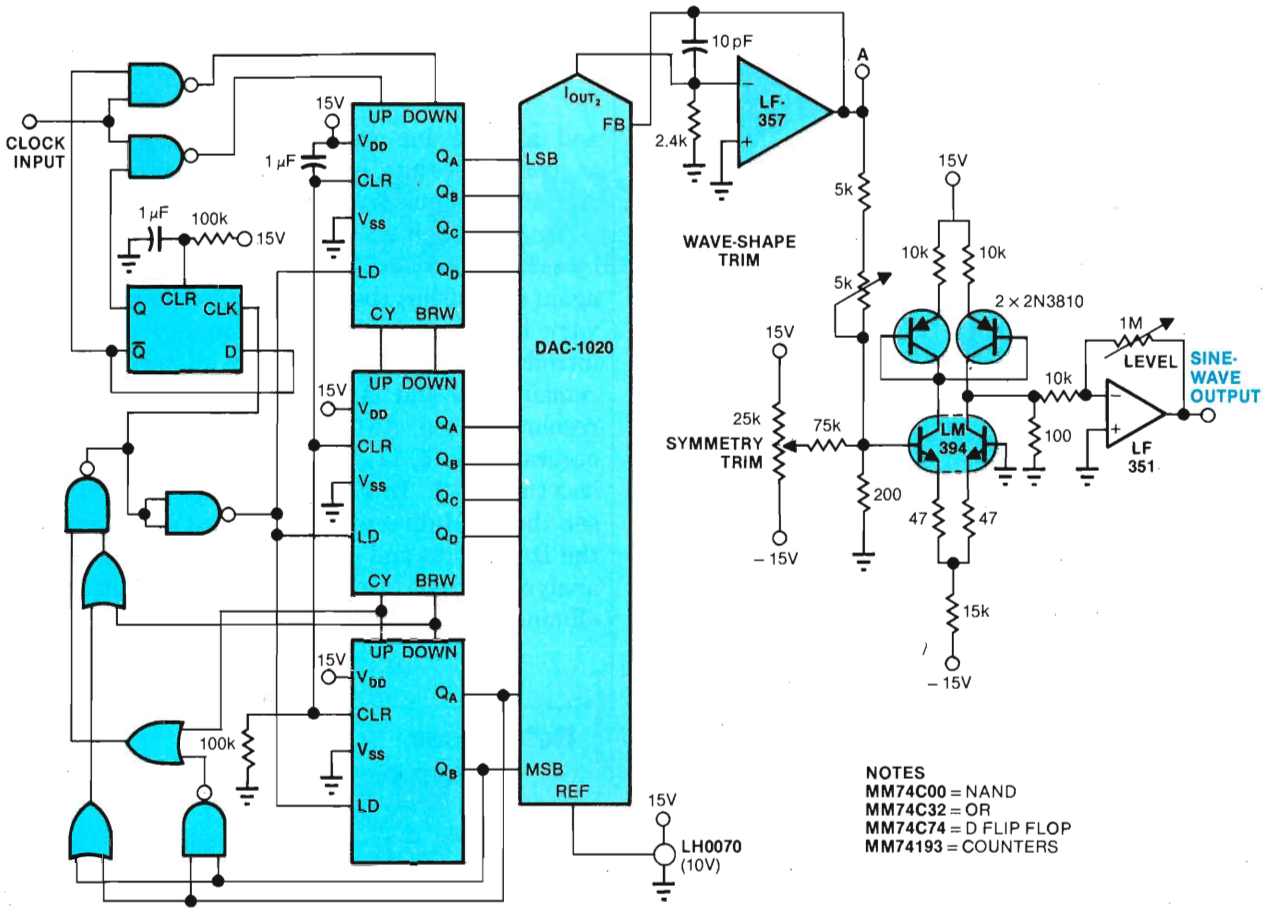
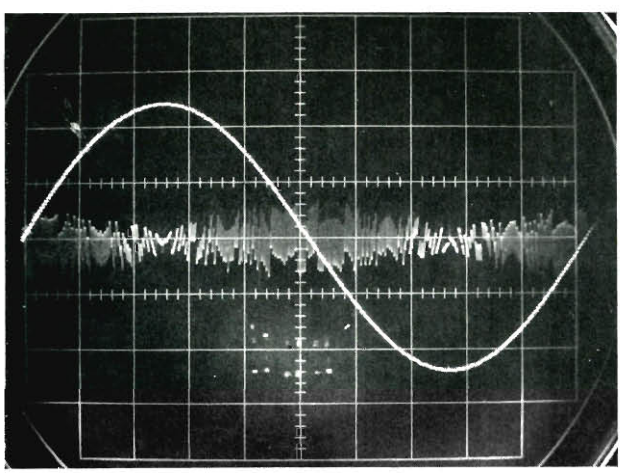


Fig 15—Digital techniques *produce triangular waveforms that methods employed in* ***Fig 11*** *can then easily convert to sine waves. This digital approach divides the input clock frequency by 1024 and uses the resultant 10 bits to drive a DAC. The DAC's triangular output—amplified by the LF357—drives the log shaper stage. You could also eliminate the log shaper and place a sine-coded ROM between the counters' outputs and the DAC, then recover the sine wave at point A.*



TRACE	VERTICAL	HORIZONTAL
SINE WAVE	1V/DIV	200 μSEC/DIV
ANALYZER	0.2V/DIV	

Fig 16—An 8-bit sine-coded-ROM version of Fig 15's circuit *produces a distortion level less than 0.5%. Filtering the sine output—shown here with a distortion analyzer's trace—can reduce the distortion to below 0.1%.*

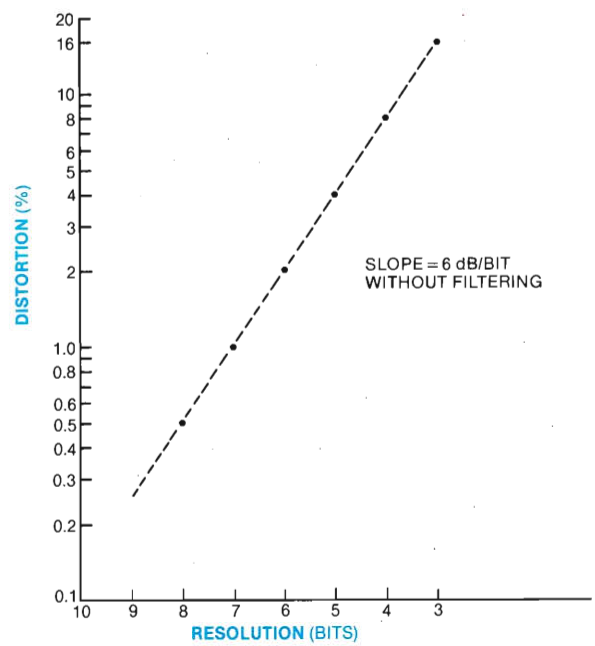


Fig 17—Distortion levels decrease *with increasing digital-word length. Although additional filtering can considerably improve the distortion levels (to 0.1% from 0.5% for the 8-bit case), you're better off using a long digital word.*

and take the sine-wave output directly from the LF357 at point A—thus employing an extremely powerful digital technique for generating sine waves.

You can amplitude-modulate **Fig 15**'s circuit's output by driving the DAC's reference input. The clock speed again establishes the operating frequency, and you can vary both amplitude and frequency quickly without introducing significant lag or distortion. Distortion remains low and is related to the number of bits of resolution used. At the 8-bit level, only 0.5% distortion occurs (**Figs 16, 17**), and filtering reduces this figure to less than 0.1%. In **Fig 16,** for example, you can clearly see the ROM-directed steps in the sine waveform, and the DAC levels and glitching show up in the distortion-analyzer output. But filtering at the output amplifier eliminates these frequency components. **EDN**

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Author's biography

Jim Williams, design engineer with National Semiconductor Corp's Linear Applications Group, Santa Clara, CA, has made a specialty of analog-circuit design and instrumentation development. Before joining NSC, he was a consultant with Arthur D Little Inc in analog systems and circuits. From 1968 to 1977, Jim directed the Instrumentation Development Lab at the Massachusetts Institute of Technology, where in addition to designing experimental biomedical instruments, he was active in course development and teaching. A former student of psychology at Wayne State University, he lists tennis, art and collecting antique scientific instruments as his leisure interests.

Use comparator ICs in new and useful ways

You can use the unique differential-input/digital-output characteristics of comparators to implement a wide range of circuit functions.

Jim Williams, National Semiconductor Corp

Perhaps the most underrated and underutilized of monolithic ICs, comparators are among the most flexible and universally applicable components in your design arsenal. With their differential linear inputs and very-fast-switching digital outputs, these devices can help you implement unusual circuit functions at favorable cost and low component count compared with other approaches. Examples ranging from a shaft-angle encoder to a V/F converter show how you can exploit comparators' unique abilities.

Variable capacitor makes shaft-angle encoder

If, for example, you need to convert a shaft angle to a digital bit stream, you can employ **Fig 1**'s comparator-

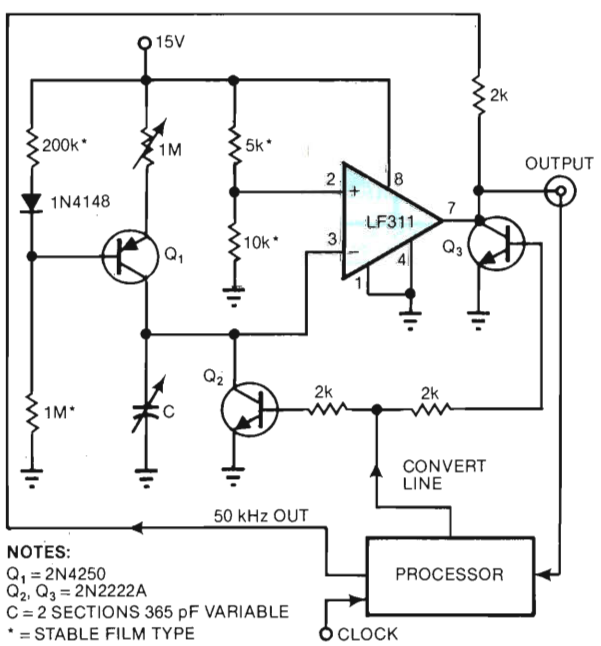
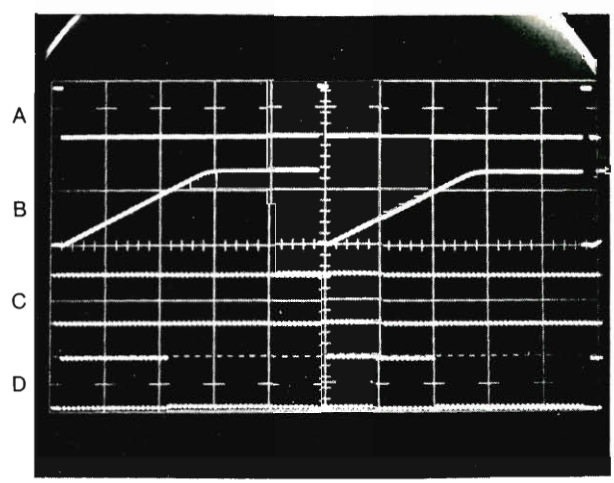


Fig 1—Employing a variable capacitor and a comparator, *a single-supply circuit yields a pulse burst—triggered by a Convert-line HIGH-to-LOW transition—whose duration is a ±0.1% linear function of the capacitor's shaft angle.*



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	200 μSEC/DIV
B	10V/DIV	200 μSEC/DIV
C	5V/DIV	200 μSEC/DIV
D	5V/DIV	200 μSEC/DIV

Fig 2—When the linear charging ramp *(trace B) of* ***Fig 1****'s variable capacitor reaches 10V, it signals a comparator to shut off the trace D output pulse burst.*

Obtain shaft-angle readings with a comparator-based circuit

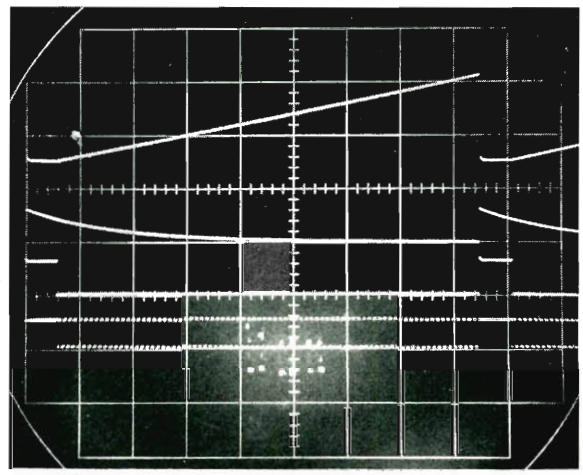
based circuit. It uses a standard AM-radio dual 365-pF variable air capacitor to generate a controlling-processor-triggered constant-frequency pulse burst. The burst's duration—or the number of pulses it contains—indicates shaft position to within a ±0.1% typ accuracy. Moreover, the capacitor has essentially infinite life—unlike potentiometers, which can wear quickly and require frequent replacement in high-usage applications such as video arcade games.

In operation, transistor Q_1 and associated components form a ground-referred current source that linearly charges the variable capacitor. When the controlling processor needs a shaft-angle conversion, it drives the Convert line HIGH (**Fig 2,** trace A), turning Q_2 on and discharging the capacitor. Concurrently, Q_3 turns on, forcing the circuit output to zero.

To continue the conversion, the processor pulls the Convert line LOW, and the constant-current-source-driven capacitor voltage begins to ramp linearly toward the 15V supply (**Fig 2,** trace B). This Convert-line HIGH-to-LOW transition simultaneously unclamps the LF311's output, thus triggering a pulse burst by causing the processor's clock (**Fig 2,** trace C) to appear as a serial bit stream at the output (**Fig 2,** trace D).

The circuit continues to transmit this bit stream until the capacitor's voltage crosses the level established by the 5-kΩ/10-kΩ resistor divider; at that point the comparator output clamps, inhibiting pulses. Note that each Convert-line HIGH-to-LOW transition initiates an updated bit-stream output.

The circuit is insensitive to supply shifts because the resistor-divider trip point and the current-source reference are ratiometrically related. The FET-input comparator does not appreciably load other circuit components, so linearity is excellent. With a standard variable air capacitor (General Radio Type 722) substi-



TRACE	VERTICAL	HORIZONTAL
A	0.5V/DIV	1 mSEC/DIV
B	0.1V/DIV	1 mSEC/DIV
C	5V/DIV	1 mSEC/DIV
D	10V/DIV	1 mSEC/DIV

Fig 4—The number of pulses *between bit-stream gaps in the* ***Fig 3*** *circuit's output (trace D) is a linear function of temperature.*

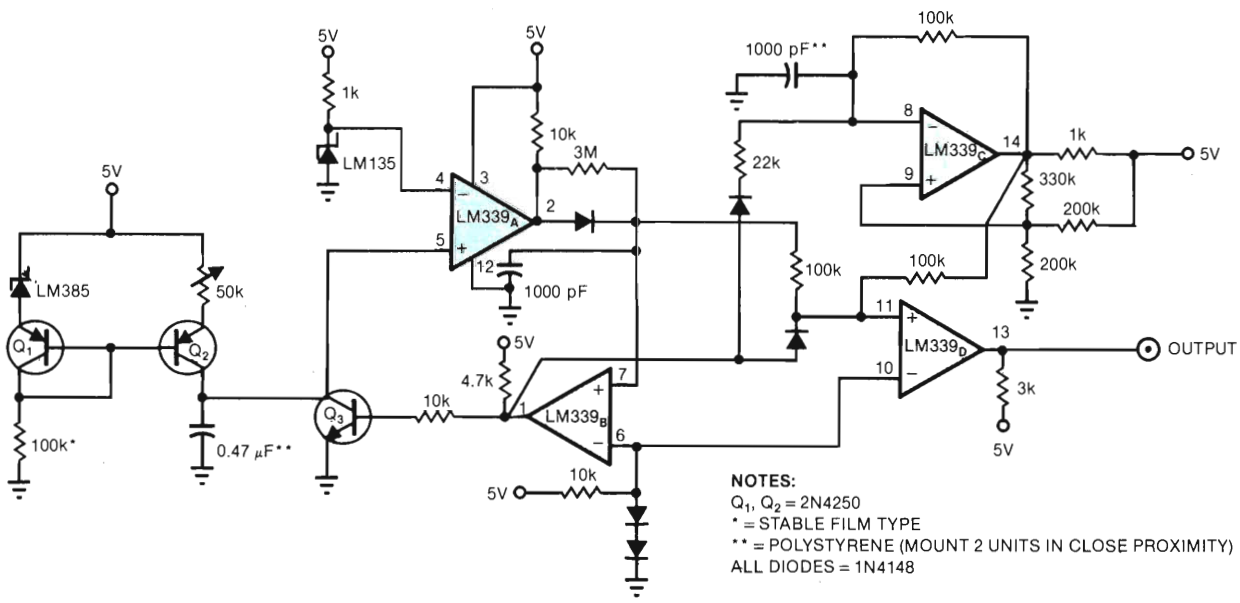


Fig 3—Furnishing an output pulse count proportional to temperature, *this LM135-sensor-based circuit requires no external clock. A gap in the output bit stream indicates the end of conversion.*

tuted for the dual 365-pF unit, linearity is well within ±0.1%. Use the 1-MΩ potentiometer to set the desired scale factor.

Convert temperatures to bit streams

Fig 3 shows another serial-output converter, one that requires only a 5V supply. Generating this circuit's output, which indicates the temperature at the LM135 sensor, doesn't require an external command—instead, the circuit clocks itself continuously and inserts gaps in the output stream to indicate the end of one conversion and the beginning of a new one.

Q_1 and Q_2 form a temperature-compensated current source whose output is referenced to the LM385. Q_2's collector current linearly charges the 0.47-μF capacitor (**Fig 4**, trace A) until the ramp voltage exceeds the LM135's voltage. Then, $LM339_A$'s output goes HIGH, dumping charge into the 1000-pF capacitor and forcing $LM339_B$'s positive input (**Fig 4**, trace B) and output (**Fig 4**, trace C) HIGH. This action turns on Q_3, resetting the ramp capacitor.

The 1000-pF capacitor can discharge only through the 3-MΩ resistor paralleling the diode at $LM339_A$'s pin 2. Therefore, the waveform at $LM339_B$'s positive input decays slowly, and the ramp capacitor stays off for an extended period of time. When the 1000-pF capacitor's

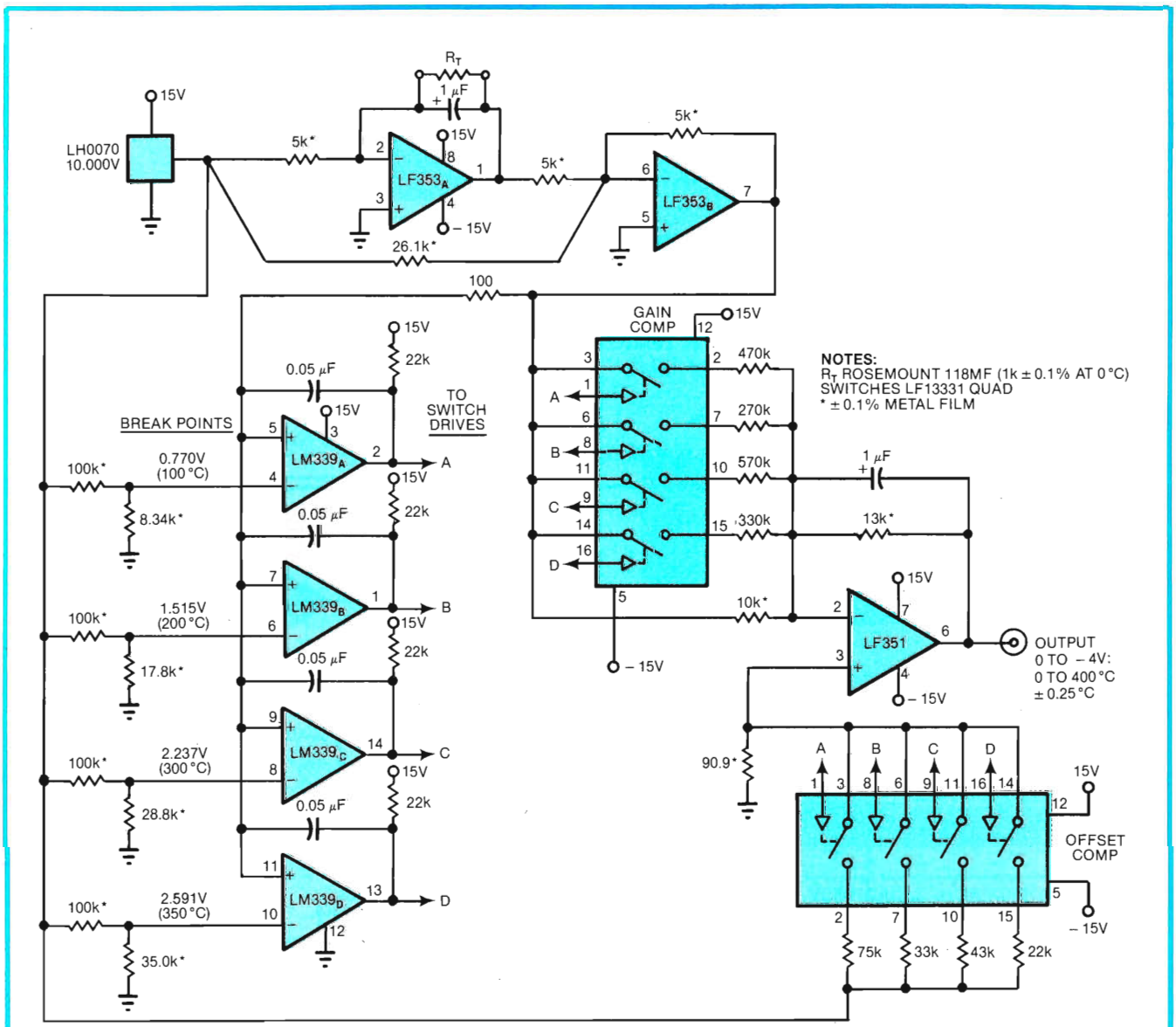


Fig 5—Using breakpoint corrections *at four temperatures and requiring no trimming, this circuit compensates for a platinum RTD sensor's nonlinearity.*

Temperature-sensing scheme uses a 4-comparator IC

voltage finally decays below the 2-diode-drop value at $LM339_B$'s negative input, Q_3 turns off, ramping begins and the cycle repeats.

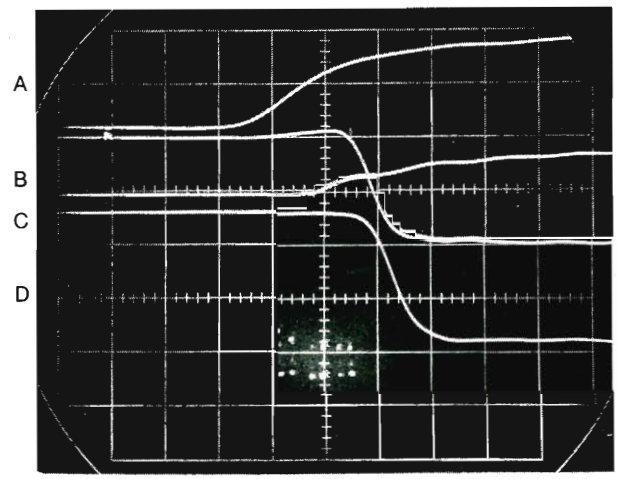
The oscillation frequency varies inversely with the LM135's output voltage. The ramping time, however, is directly—and linearly—proportional to the LM135's output. While the ramp is running, $LM339_B$'s output is LOW, and $LM339_C$, which functions as a 10-kHz clock, biases $LM339_D$, providing the circuit's output. When $LM339_A$'s output goes HIGH, the 100-kΩ resistor path from $LM339_A$ to $LM339_D$'s positive input in turn forces $LM339_D$'s output HIGH (**Fig 4**, trace D).

Reinforcing feedback results when $LM339_B$'s output goes HIGH and applies bias through the diode path to $LM339_D$'s positive input. This condition lasts until the 1000-pF-capacitor voltage decays to a value sufficiently low for the cycle to repeat. The 22-kΩ resistor/diode path from $LM339_B$'s output to $LM339_C$'s negative input synchronizes the 10-kHz clock to the circuit's ramp-reset sequence, thereby averting a ±1-count uncertainty in the output data.

A monitoring processor can use the gap in the circuit's output bit stream to synchronize itself to the temperature data. To calibrate the circuit, measure the voltage at the LM135 and adjust the 50-kΩ potentiometer so that the number of bits in each burst relates numerically to this voltage (eg, 2.98V=298 bits).

Linearize a platinum RTD with comparators

If, instead of an LM135 sensor, you're using platinum RTDs (resistance temperature detectors) to take advantage of their extremely wide operating-temperature ranges and their long-term stability under adverse environmental conditions, consider the **Fig 5** linearizing



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	10 nSEC/DIV
B	50 mA/DIV	10 nSEC/DIV
C	5V/DIV	10 nSEC/DIV
D	10V/DIV	10 nSEC/DIV

Fig 7—The fast shutdown action *of* ***Fig 6****'s circuit results in power cutoff (trace D) within 30 nsec of an overload occurrence. Note the beginning of the overload (trace B) at about four horizontal divisions from the left of the screen.*

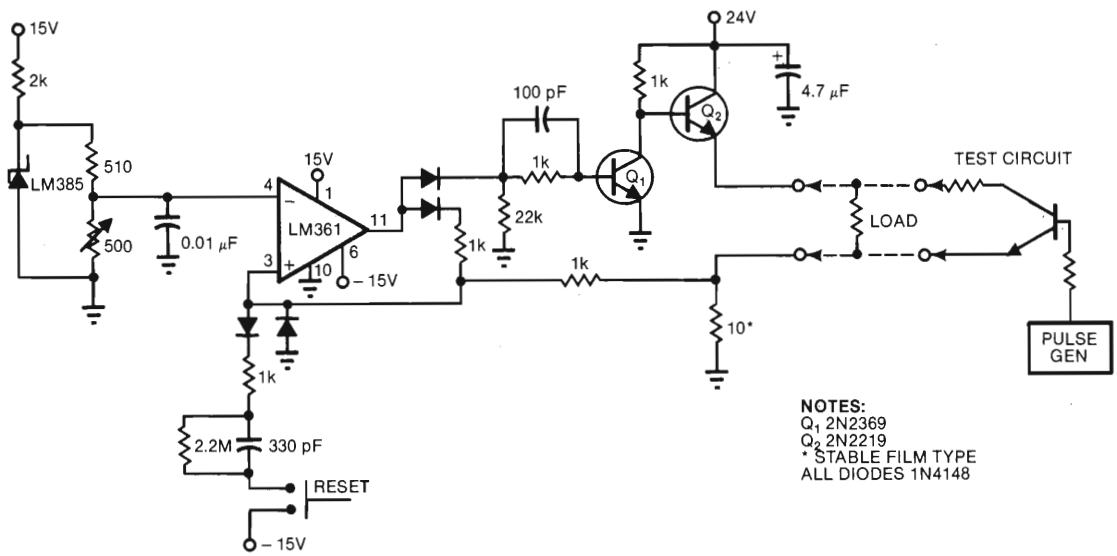


Fig 6—A fast-acting power-shutdown circuit can protect sensitive components. *The one shown here employs a comparator and a 10Ω sense resistor to establish a 100-mA trip point.*

circuit. It overcomes an RTD's inherent nonlinearity (>6° error from 0 to 400°C) by using an LM339 quad comparator to apply a 4-section breakpoint correction. In contrast to other RTD-linearizing circuits, **Fig 5**'s design needs no calibration.

Because of the RTD sensor's positive temperature coefficient, op amp $LF353_A$'s output rises with increasing temperature. Summing the output with a constant current at $LF353_B$'s negative input results in a 0V $LF353_B$ output at 0°C; this output increases as a direct but nonlinear function of the RTD's temperature.

$LF353_B$'s temperature-dependent output drives the positive inputs of the LM339 comparators and provides the input to the output gain stage, $LF351_C$. The threshold voltages at the LM339 negative inputs cause the respective comparators to switch at the $LM353_B$ voltages corresponding to 100, 200, 300 and 350°C.

When a comparator output switches HIGH, it switches in gain- and offset-changing resistors via the LF13331 JFET switches. The four slight gain adjustments compensate for the RTD's nonlinearity, and the introduced offsets ensure a monotonic increase in output as temperature rises. The 0.05-μF capacitors at the LM339 outputs prevent chattering at the trip points; the 1-μF capacitor in the LF351's feedback loop eliminates transient switching signals from the output.

If you use the **Fig 5** circuit values and RTD sensor, you can obtain ±0.15°C accuracy over 0 to 400°C with no trimming of any kind.

Do you have need to protect expensive components in a system—perhaps, for example, during the final phases of trimming and calibration? If so, consider the **Fig 6** circuit—it shuts down power within 30 nsec of an overload occurrence (in this case, for load currents greater than 100 mA).

When the current is less than or equal to 100 mA, the LM361's output is LOW, Q_1 is OFF and emitter follower

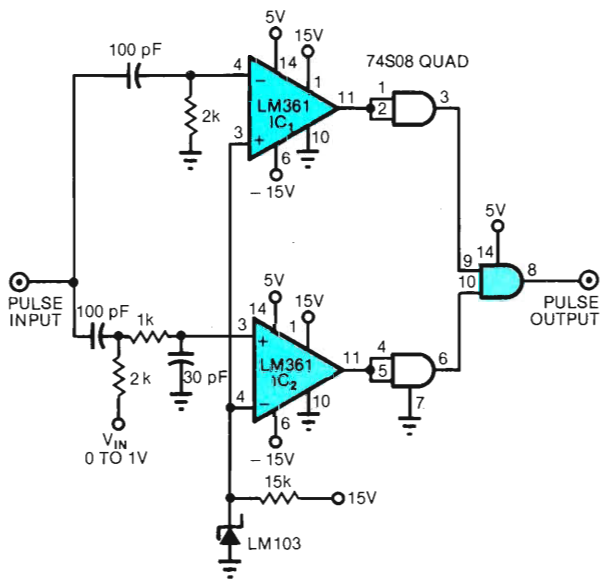
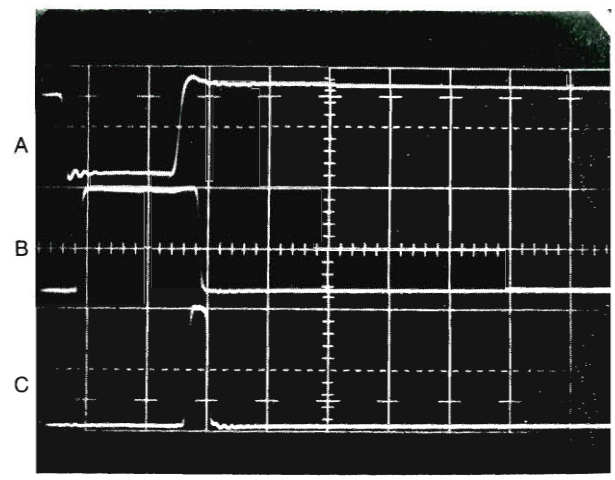
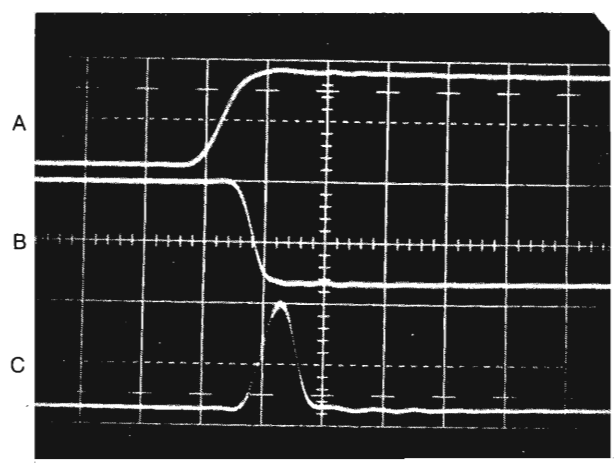


Fig 8—A circuit based on two comparators *and an AND gate can generate 6-nsec-wide pulses with 2-nsec rise and fall times. The V_{IN} level determines pulse width.*



TRACE	VERTICAL	HORIZONTAL
A	2V/DIV	200 nSEC/DIV
B	2V/DIV	200 nSEC/DIV
C	2V/DIV	200 nSEC/DIV



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	10 nSEC/DIV
B	5V/DIV	10 nSEC/DIV
C	5V/DIV	10 nSEC/DIV

Fig 9—The ANDing action *of* ***Fig 8****'s 74S08 gate yields a narrow pulse (**(a)**, trace C) because of time displacement between comparator outputs (traces A and B). The traces in **(b)** show the signals at these same circuit nodes for a 100-mV V_{IN}.*

Comparator high-speed switching eases pulse-generation tasks

Q_2 sources power to the load and the 10Ω sense resistor. When an overload occurs (in this case via the test circuit, whose output appears in **Fig 7,** trace A), the current through the 10Ω sense resistor begins to increase. (Note the slight load-current rise in **Fig 7,** trace B.)

This rise in current produces a corresponding voltage increase at the LM361's positive input. The comparator's output then rises (**Fig 7,** trace C) and drives Q_1 through a heavy feedforward network. Although this network degrades the LM361's output rise time somewhat, Q_1 responds very quickly and clamps Q_2's base to ground, causing load voltage (**Fig 7,** trace D) to immediately decay to zero.

As noted, the total elapsed time from overload onset to circuit shutdown is 30 nsec. Once the shutdown has occurred, the resistor-diode network from the LM361's pin 11 to pin 3 provides latching feedback to keep power

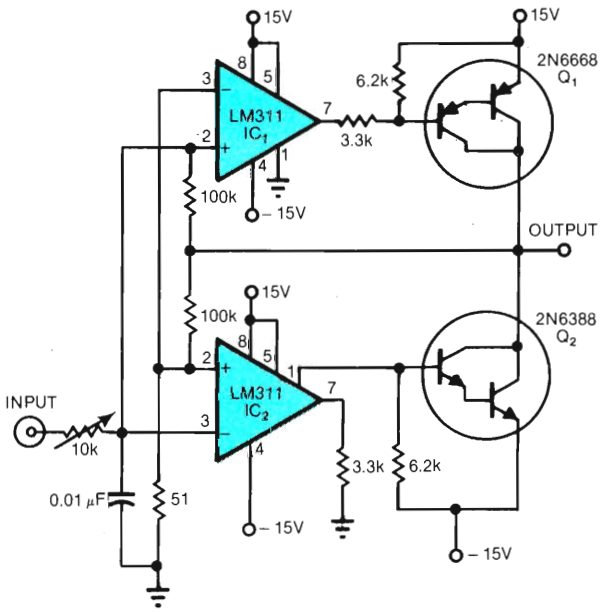


Fig 10—A comparator-based 400-Hz switching amplifier *is inexpensive, requires few components and can provide a 6A output.*

off the load. The reset pushbutton causes a negative spike to appear at the LM361's positive input, breaking the latching feedback and allowing the loop to function normally again. Use the 500Ω potentiometer to set the trip point at the desired value (for the **Fig 6** circuit, 1V=100 mA).

Comparators make 2-nsec pulse generator

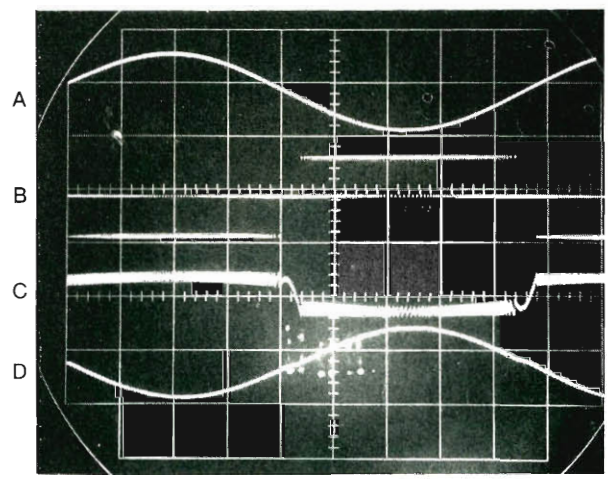
Similarly benefiting from the LM361's high-speed performance, the **Fig 8** ultra-high-speed pulse generator furnishes voltage-controllable pulse widths. Its differentiator networks generate a pair of pulses with slightly different durations; the comparators and a Schottky TTL gate extract the difference between two widths and present it as a single fast-rise-time pulse at the circuit output.

When you apply a positive input pulse, the two 100-pF/2-kΩ differentiator networks yield positive outputs. When the positive-going steps exceed the 2V threshold established by the LM103, both LM361s switch output states. For a 0V control input, the differentiator networks and the LM361s respond simultaneously, and both output transitions line up.

As you increase the control voltage, however, the spike produced by IC_2's differentiator arrives at the 2V threshold earlier than does that of IC_1. IC_2 also normally takes longer to decay through the 2V threshold, appearing to lead to a situation in which IC_2's output would remain HIGH longer and switch earlier than would IC_1's.

IC_2's 30-pF/1-kΩ network, however, provides a delay that shifts the IC_2 output so that IC_1's leading and trailing edges occur first (**Fig 9a,** traces A and B). The length of time between the comparator outputs' edges depends on the input control voltage.

For the **Fig 8** circuit, a 0 to 1V control range produces a trailing-edge timing difference of 0 to 100 nsec. The



TRACE	VERTICAL	HORIZONTAL
A	2V/DIV	200 μSEC/DIV
B	20V/DIV	200 μSEC/DIV
C	100 mV/DIV	200 μSEC/DIV
D	20V/DIV	200 μSEC/DIV

Fig 11—The power envelope *of the* ***Fig 10*** *switching amplifier's output (trace D) is sinusoidal when the circuit is driven by a sine-wave input (trace A). Note the high-frequency charging and discharging of the circuit's 0.01-μF capacitor (trace C).*

Comparator circuit handles frequency-division chores

DM74S08 ANDs the two comparators' outputs to obtain the single-pulse circuit output (**Fig 9a,** trace C).

The gate and comparator switching speeds limit the minimum pulse width to 6 nsec; rise and fall times are approximately 2 nsec. **Fig 9b** shows an example of the high-speed operation that the **Fig 8** circuit can achieve (control input=100 mV). Traces A and B represent IC_1 and IC_2 outputs, respectively; trace C is the circuit's output pulse.

If you need a simple, inexpensive 400-Hz amplifier, consider the **Fig 10** circuit. It uses ±15V supplies,

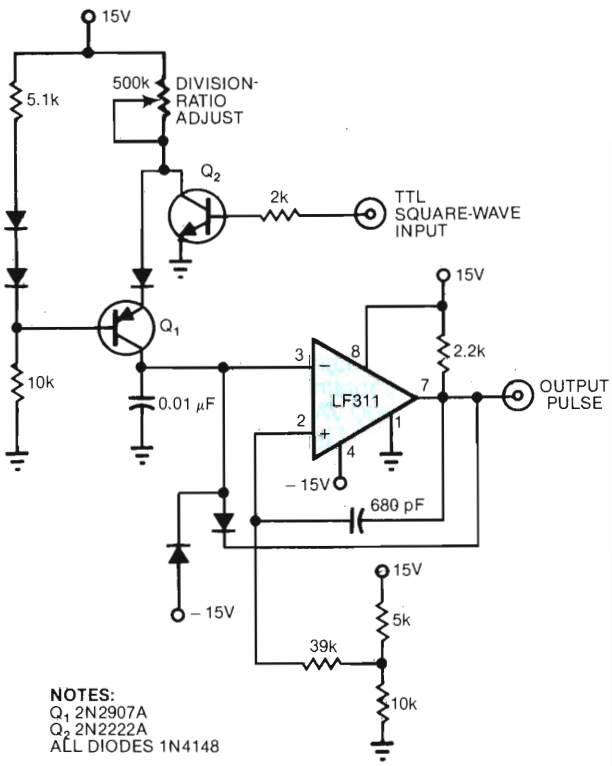


Fig 12—Divide and conquer *your frequency-reduction problems with this synchronous circuit. You can vary the division ratio over a 1:1,000,000 range.*

provides full bipolar swing and has a 1.5-kHz full-power bandwidth with a 6A pk output capability.

If the input voltage is negative, IC_2's output is LOW (note that IC_2 operates in an emitter-follower mode, so its output is in phase with its negative input), cutting Q_2 off. Concurrently, IC_1's output goes LOW, turning Q_1 on and thereby driving the load and the 100-kΩ resistors connected to the comparators' positive inputs. This feedback produces a small voltage at IC_1's negative input.

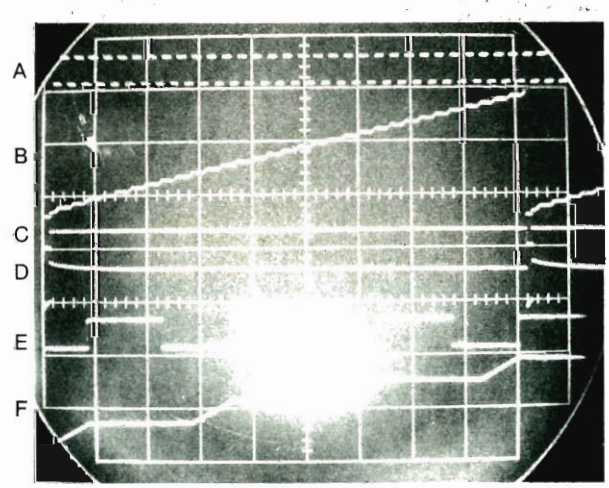
When the 0.01-μF capacitor charges to a level high enough to offset the negative input, IC_1's output changes state, turning Q_1 off. At this point, the input draws current from the capacitor, forcing IC_1's positive input to a lower state and consequently driving IC_1's output LOW again, turning Q_1 on.

The switching action occurs continuously; repetition rate depends on the input voltage. For positive inputs, IC_2 and Q_2 perform similar action. To avoid cross-current conduction in the output transistors, tie the comparators' offset-adjust terminals to the 15V supply.

Fig 11 trace B shows the circuit output resulting from the trace A input; the trace C waveform represents current flow in and out of the capacitor. (Think of the IC_2 pin 3 point as a digitally driven summing junction.) Trace D is a lightly filtered version of trace B; it clearly shows that the circuit output has a sinusoidal power envelope. You can vary the amplifier gain with the 10-kΩ input potentiometer.

Divide frequencies over a 1:1,000,000 range

Using the **Fig 12** circuit, you can divide a frequency over a $1:10^6$ range, adjustable via a single potentiometer. Moreover, the output frequency you obtain is synchronously related to the input frequency. You can use this circuit to obtain simultaneous oscilloscope observations of low-frequency signals and the fast clock



TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	100 μSEC/DIV
B	5V/DIV	100 μSEC/DIV
C	50V/DIV	100 μSEC/DIV
D	20V/DIV	100 μSEC/DIV
E	10V/DIV	10 μSEC/DIV
F	0.2V/DIV	10 μSEC/DIV

Fig 13—Using a step-charging technique *that results in the trace B capacitor voltage,* ***Fig 12****'s circuit yields an output frequency proportional to and synchronized with an input signal's frequency (trace A). In the example shown here, the output (trace C) contains a pulse after 32 input pulses.*

Manipulate pulses with comparator-based circuits

from which they're derived or to synchronously trigger an A/D converter at a variable rate.

The circuit functions by step-charging a capacitor with a switched current source and using a comparator to determine when to reset the capacitor. **Fig 13,** trace B, shows the step-charging waveform; each time the pulse input (**Fig 13,** trace A) goes LOW, a current-source pulse causes a capacitor-voltage positive step. You can control the step height—and therefore the division ratio—with the 50-kΩ potentiometer.

When the staircase waveform reaches the voltage at the LF311's positive input, the comparator output goes LOW (**Fig 13,** trace C) and stays LOW until the positive feedback through the 680-pF capacitor ceases. The delay produced by this feedback ensures a complete reset for the 0.01-μF capacitor, which discharges through the steering diode into the comparator output.

The diode connected from LF311 pin 3 to −15V provides first-order compensation for the steering diode's leakage effects during the charge cycle. **Fig 13,** trace D, shows the waveform at the LF311's positive input. Traces E and F show in an expanded time scale the relationship between the input waveforms and the step-charged ramp.

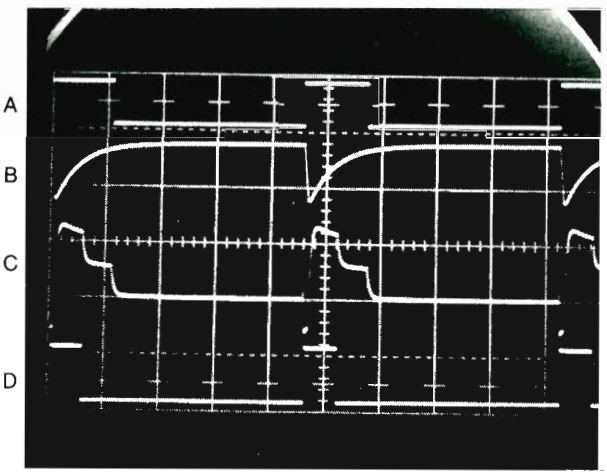
When using this circuit, remember that although the output frequency is always synchronously related to the input frequency, its absolute value can vary with time and temperature. Typically, the trip point—hence, the output frequency—moves back and forth along the horizontal portion of a step at low division ratios and changes from step to step at high ratios.

Overcome TTL multivibrators' shortcomings

If you've used TTL monostables, you've undoubtedly noticed their poor input triggering characteristics and limited dynamic range with a given timing capacitor. The **Fig 14** circuit surmounts these limitations to provide a true level-triggered input and a single-resistor-programmable 10,000:1 output-pulse range. It delivers a preprogrammed output pulse width regardless of the input pulse duration. (The minimum input trigger-pulse width is, however, 3 μsec.)

When you apply an input pulse (**Fig 15,** trace A) to the circuit, $LM393_A$'s output goes LOW (**Fig 15,** trace B), producing reinforcing feedback for its own positive input (**Fig 15,** trace C). This causes $LM393_B$'s output to go HIGH, providing additional feedback to $LM393_A$'s positive input via the 1-MΩ resistor.

When the 50-pF capacitor ceases to provide feedback



TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	200 μSEC/DIV
B	5V/DIV	200 μSEC/DIV
C	1V/DIV	200 μSEC/DIV
D	5V/DIV	200 μSEC/DIV

Fig 15—The output pulse width *(trace D) of* ***Fig 14****'s monostable circuit is insensitive to the input width (trace A).*

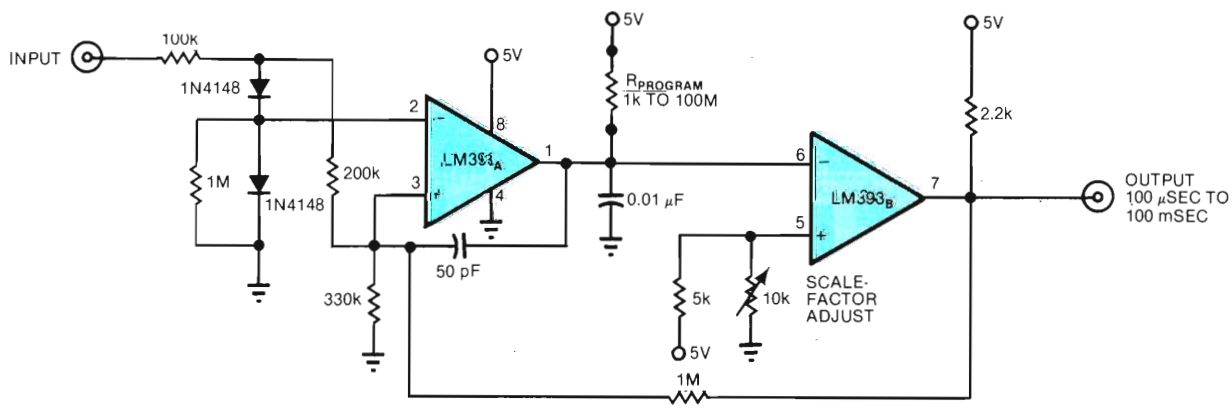


Fig 14—Better than a multivibrator, *this monostable circuit provides a true level-triggered input and a 10,000:1 output pulse range. You program the output pulse width with one resistor.*

to $LM393_A$'s positive input, this comparator's output goes HIGH, allowing the 0.01-μF timing capacitor to charge (**Fig 15,** trace B). When the capacitor voltage exceeds $LM393_B$'s positive input voltage, $LM393_B$'s output (**Fig 15,** trace D) goes LOW, terminating the output pulse.

With the 0.01-μF timing capacitor, you can obtain output pulse widths of 10 μsec to 100 msec, with a scale factor (trimmable with the 10-kΩ potentiometer) of 100Ω/μsec.

Get variable width and delay with one IC

If you need a known-width pulse that's delayed with respect to another pulse, consider the **Fig 16** circuit. It works from one 5V supply and requires only one dual-comparator IC.

When you apply a TTL input (**Fig 17,** trace A), $LM319_A$'s output stays LOW until the 1500-pF capacitor at its positive input charges beyond the negative input's 1.2V level. The resistor-diode clamp from the circuit input to $LM319_A$'s pin 5 provides immunity to input-amplitude variations.

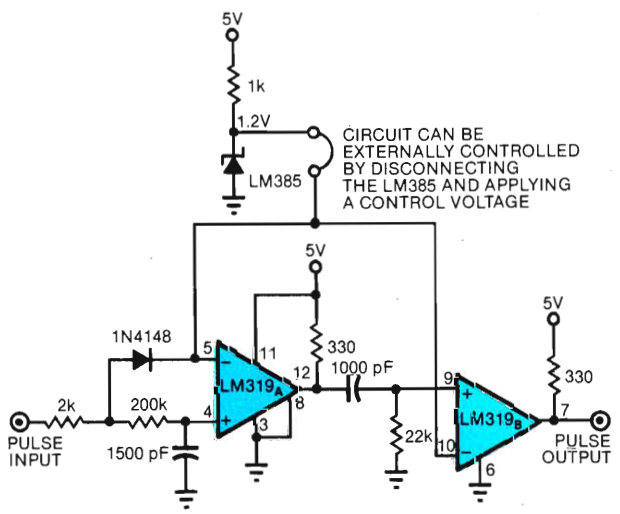


Fig 16—Form a pulse *having the parameters you need from this simple 1-IC circuit. The 1500-pF/200-kΩ network determines delay relative to a triggering pulse; the 1000-pF/22-kΩ differentiator sets the width.*

When $LM319_A$'s output goes HIGH (**Fig 17,** trace B), the transition is coupled via the 1000-pF/22-kΩ differentiator to $LM319_B$'s positive input (**Fig 17,** trace C), causing $LM319_B$'s output to rise and stay HIGH (**Fig 17,** trace D) until the differentiator output drops below the 1.2V level at $LM319_B$'s negative input.

You can tailor both the delay time and the output pulse width to your requirements by altering the values of the RC networks. Alternatively, you can control these parameters externally by applying variable voltages to the comparators' negative inputs.

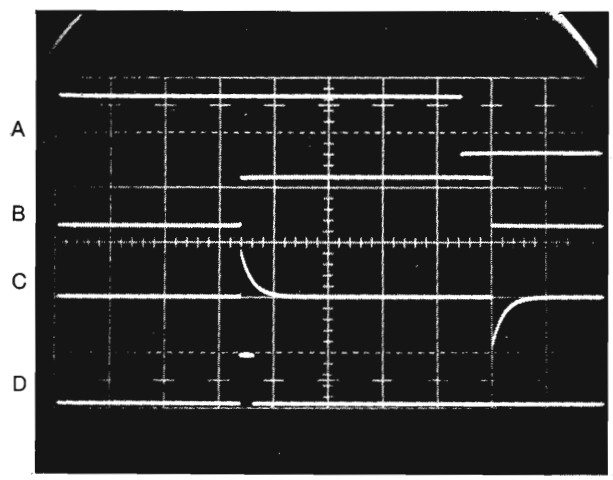
Make an ultrafast V/F converter

Using two comparator ICs, you can build a V/F converter that yields a 5-kHz to 10-MHz output, with better than ±1% linearity, from a 0 to 5V input. The LM160's 20-nsec propagation delay allows **Fig 18**'s circuit to run much faster than monolithic VFCs.

The LM160's output switches the 50-pF capacitor between a reference voltage (furnished by the LM385) and the comparator's negative input. The comparator's output pulse width is unimportant so long as it permits complete charging and discharging of the capacitor. The LM160 also drives the 5-pF/510Ω network, providing regenerative feedback to reinforce its output transitions.

When this positive feedback decays, any negative-going LM160 output is followed by a positive-going edge after an interval determined by the 5-pF/510Ω time constant (**Fig 19,** traces A and B).

The actual integration capacitor—the 0.01-μF unit—never charges beyond 100 mV because it's constantly reset by charge dispensed from the switched 50-pF capacitor (**Fig 19,** trace C). When the LM160's output goes negative, the 50-pF capacitor takes charge from



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	100 μSEC/DIV
B	5V/DIV	100 μSEC/DIV
C	5V/DIV	100 μSEC/DIV
D	5V/DIV	100 μSEC/DIV

Fig 17—A delayed narrow pulse *(trace D) from* ***Fig 16****'s 1-IC circuit specs delay and width of 340 and 30 μsec, respectively.*

Two comparator ICs yield a fast, linear VFC

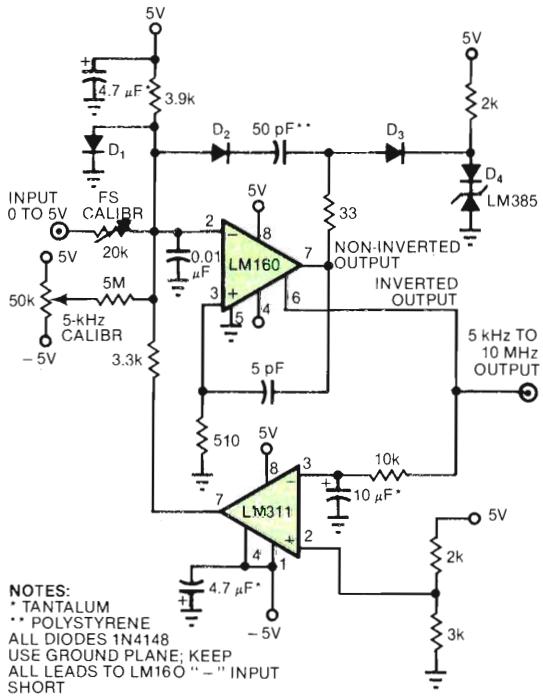
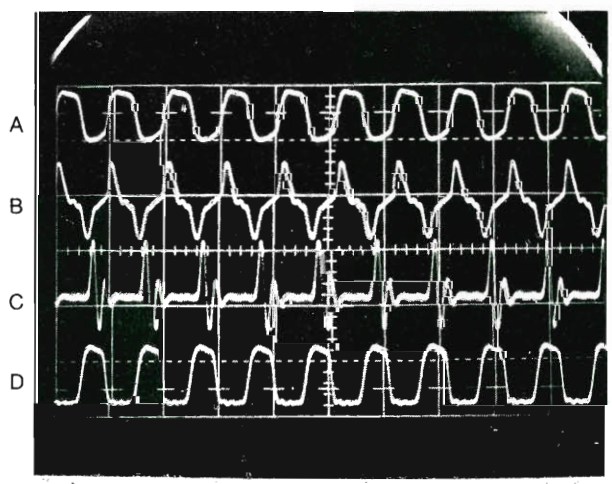


Fig 18—Producing 5-kHz to 10-MHz output, *this V/F-converter circuit uses two comparator ICs and features ±1% linearity. The LM160 is the heart of the converter; the LM311 prevents lockup.*



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	100 μSEC/DIV
B	0.5V/DIV	100 μSEC/DIV
C	10 mA/DIV	100 μSEC/DIV
D	5V/DIV	100 μSEC/DIV

Fig 19—A clean 10-MHz output *(trace D) results from an LM160's action in* **Fig 18***'s V/F converter. Trace C shows the charge-dispensing current from* **Fig 18***'s 50-pF capacitor.*

the 0.01-μF capacitor, resulting in a lower voltage.

The LM160's negative-going output also produces a short negative pulse—via the 5-pF/510Ω feedback—at its positive input. When this negative pulse decays to a point where the positive input is just higher than the negative input, the 50-pF capacitor again receives a charge, and the entire cycle repeats. Diodes D_1 and D_2 compensate for diodes D_3 and D_4, minimizing temperature drift.

The LM160's inverted output (**Fig 19,** trace D) serves as circuit output and also drives the LM311 comparator circuit to prevent LM160 lockup. Without it, any condition (such as startup and input overdrive) that allows the 0.01-μF capacitor to charge beyond its normal operating point could cause the LM160's output to go to the −5V rail and stay there.

The LM311 prevents lockup by pulling the LM160's negative input toward −5V. The 10-μF/10-kΩ network determines when the LM311 switches on. When the VFC runs normally, the 10-μF capacitor charges to a negligibly small voltage, holding the LM311 off. The LM160's inverted output stays HIGH if the VFC stops running (if lockup occurs), forcing the LM311 to turn on and restarting the circuit.

To calibrate the circuit, apply a 5V input and adjust the 20-kΩ potentiometer for a 10-MHz output. Then apply 2.5 mV and adjust the 50-kΩ potentiometer for a 5-kHz output. When building this circuit, use a ground plane and good grounding techniques and locate the components associated with the LM160 inputs as close as possible to the inputs. **EDN**

Author's biography

Jim Williams, now a consultant, was applications manager in National Semiconductor's Linear Applications Group (Santa Clara, CA), specializing in analog-circuit and instrumentation development, when this article was written. Before joining the firm, he served as a consultant at Arthur D Little Inc and directed the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art and collecting antique scientific instruments in his spare time.

Article Interest Quotient (Circle One)
High **479** ***Medium*** **480** ***Low*** **481**

Low-cost dual, quad FET op amps implement complex functions

Multiple general-purpose FET op amps in one package offer more than basic gain and control capabilities. By fully exploiting their high-performance potential, you can derive a variety of low-cost special-purpose circuits.

Jim Williams, National Semiconductor Corp

FET op amps in dual and quad packages furnish the same performance as their single-op-amp relatives, but they cost less per amplifier, occupy less board area and require fewer bypass capacitors and power-supply buses. To show you how to implement these advantages effectively, this article examines temperature-control, sine-wave-oscillator and A/D-converter circuit designs that each utilize one dual or quad FET op-amp package.

Controller maintains stable temperature

Fig 1, for example, shows a complete high-efficiency pulse-width-modulating oven-temperature controller. A single LF347 package contains the four op amps shown (A_1 through A_4).

A_1 functions as an oscillator whose output (**Fig 2,** trace A) periodically resets integrator A_2's output

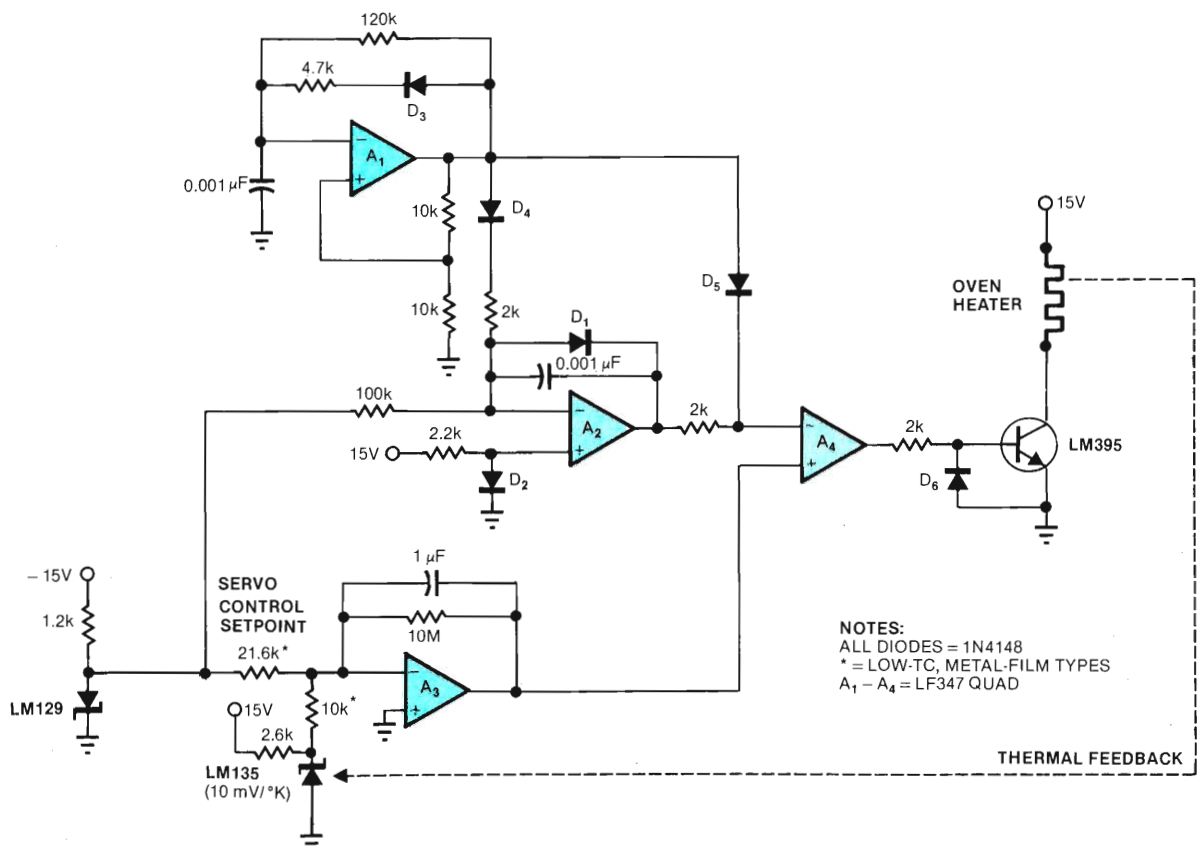


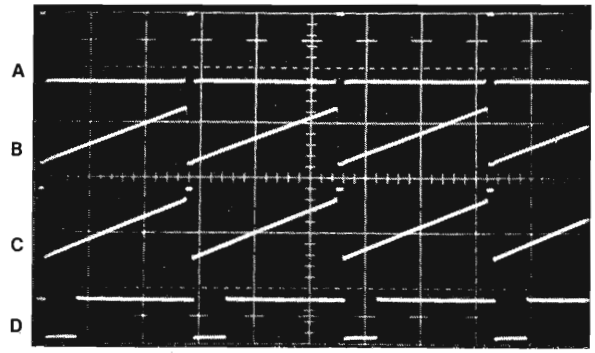
Fig 1—Connecting appropriate components *to an LF347 quad FET-op-amp IC produces a high-efficiency precision oven-temperature controller. This design can hold a temperature within 0.05°C despite wide ambient-temperature fluctuations.*

FET op amps serve efficiently in temperature-measurement circuits

(trace B) to 0V. Each time A_1's output goes high, a large positive current flows into A_2's summing junction. This current overcomes the negative current flowing through the 100-kΩ resistor into the LM329 reference. As a result, A_2's output heads negative, ultimately limited by D_1's feedback bound.

Diode D_2 provides bias at A_2's positive input to compensate for D_1. Accordingly, A_2's output settles close to 0V. When A_1's positive output pulse ends, the positive current into A_2's summing junction ceases. Then A_2's output ramps linearly until the next reset pulse.

A_3 operates as a current-summing servo amplifier that compares the currents derived from the LM135 temperature sensor and the LM329 reference. In this configuration, A_3 achieves a gain of 1000, and the 1-μF feedback capacitor permits a 0.1-Hz servo response. A_3's output represents the amplified difference between the LM135's temperature and the desired control setpoint. You can vary the setpoint by changing the



TRACE	VERTICAL	HORIZONTAL
A	20V/DIV	
B	10V/DIV	50 μSEC/DIV
C	10V/DIV	
D	20V/DIV	

Fig 2—Oven-controller waveforms *from* ***Fig 1****'s circuit show A_1's oscillator output (trace A) and A_2's integrator output (B) as the latter resets periodically to 0V. Trace C displays A_4's ramp output, and D indicates the LM395's power input to the oven heater.*

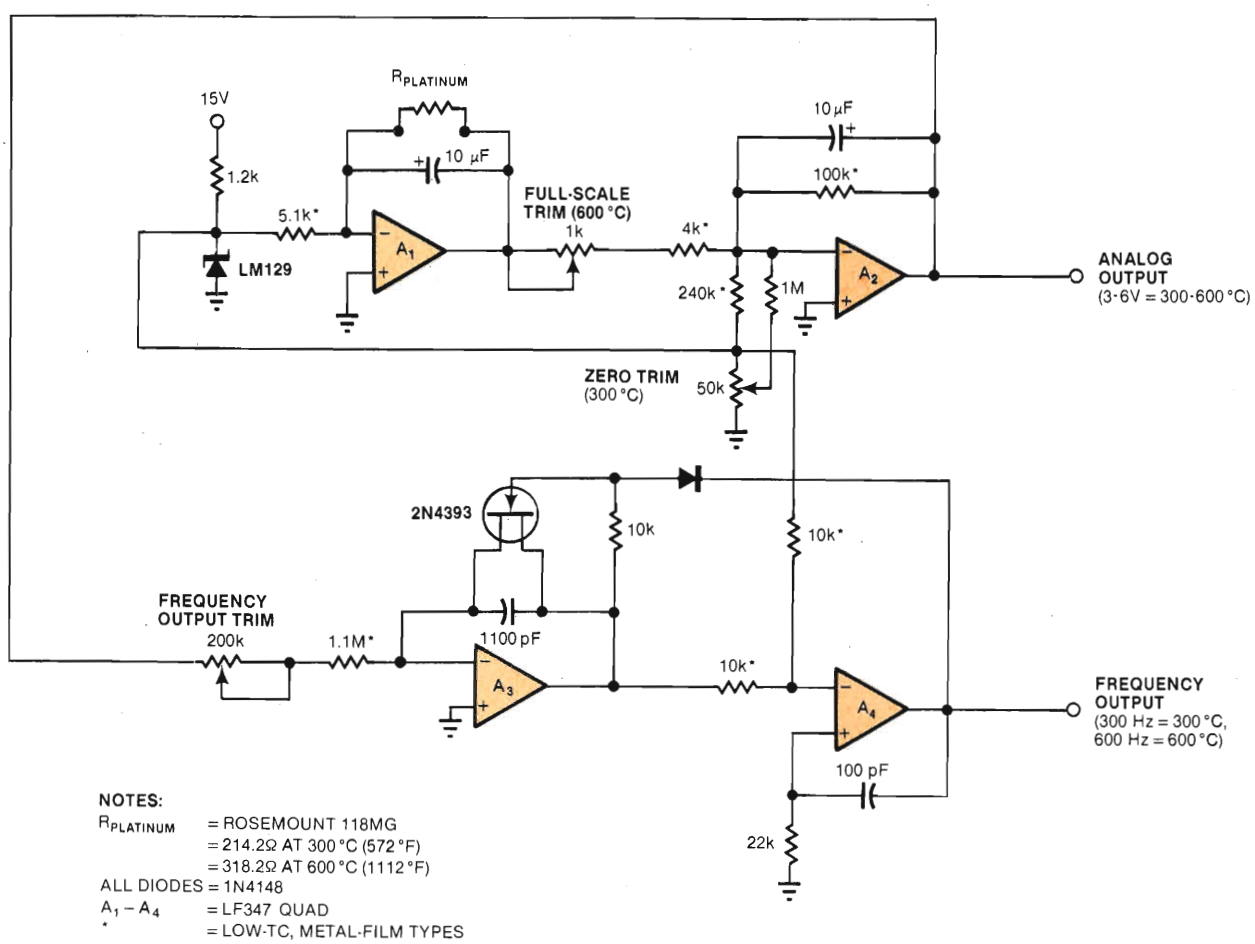


Fig 3—Generate simultaneous analog-level and frequency outputs *using one LF347 package by signal-conditioning a platinum RTD sensor. You can calibrate this high-temperature (300 to 600°C) measuring circuit to ±1°C by using three trimming pots.*

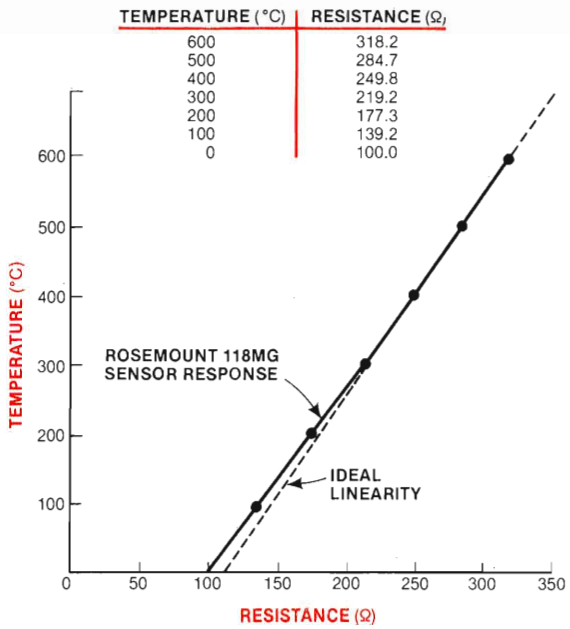


Fig 4—A platinum RTD sensor's resistance *decreases linearly from 600 to 300°C. Then, from 300 to 0°C, the sensor's resistance deviates from a straight-line slope and degrades the* ***Fig 3*** *circuit's accuracy beyond ±1°C.*

21.6-kΩ resistor's value. In **Fig 1**'s version, the 21.6-kΩ resistor provides a setpoint of 49°C (322°K).

Configured as a comparator, A_4 measures A_3's output against A_2's ramp output. Specifically, A_4's output is high only when A_3's output exceeds the ramp voltage. The ramp-reset pulse from A_1 is diode summed with the ramp output (trace C) at A_4 to prevent A_4's output from going high during the reset-pulse period.

Additionally, A_4's output biases the LM395 power transistor, which switches power (trace D) to the heater. If you tightly couple the LM135 sensor to the heater and adequately insulate the oven, this controller circuit can easily hold a setpoint within 0.05°C over wide ambient-temperature excursions.

Sensor circuit generates dual outputs

Another temperature-related circuit employing one LF347 package appears in **Fig 3.** In this design, the LF347 op amps signal-condition a platinum RTD sensor and provide simultaneous analog-level and frequency outputs. These outputs stay accurate to ±1°C over 300 to 600°C (572 to 1112°F). Although the conditioning circuit can maintain linearity over an even wider range, the sensor's nonlinear response from 0 to 300°C limits overall accuracy **(Fig 4).**

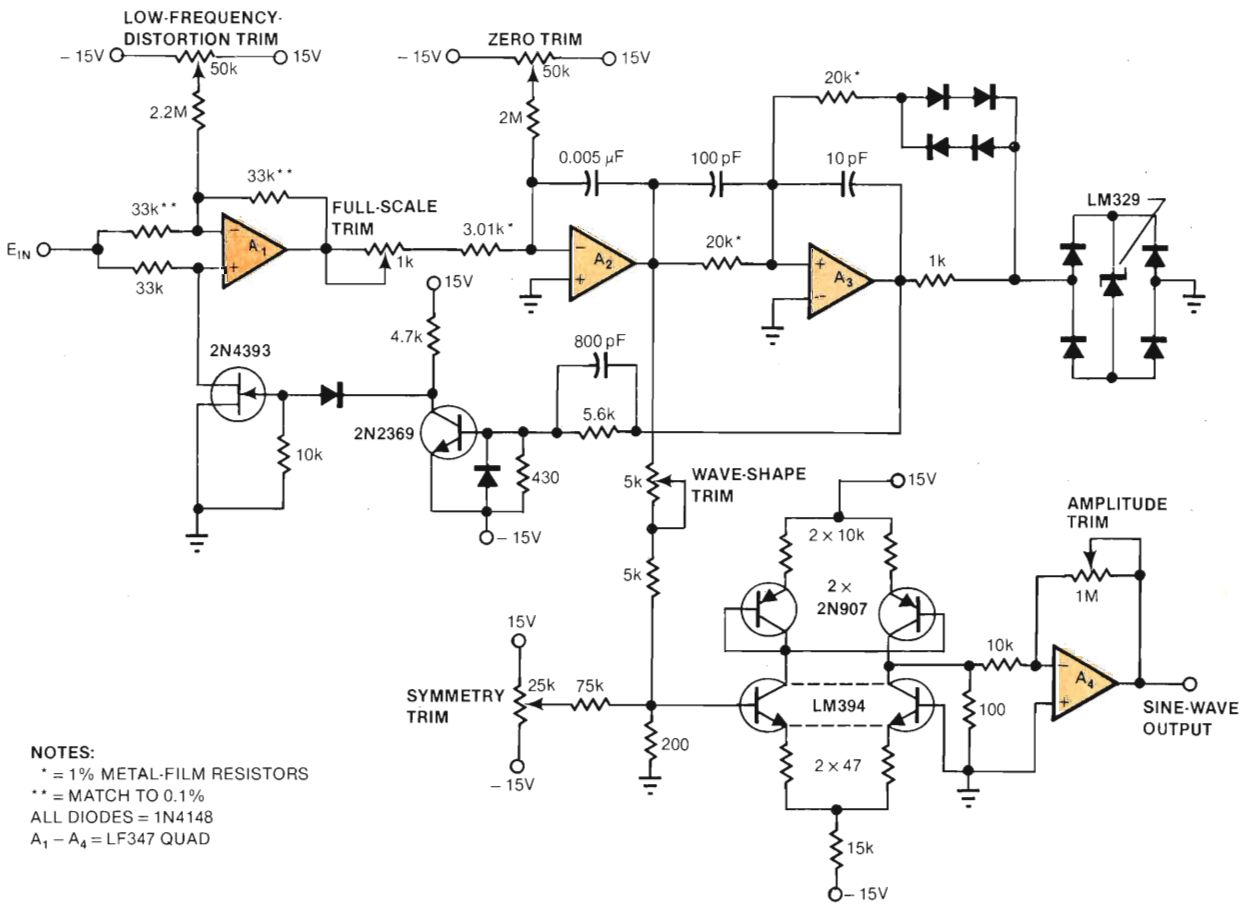


Fig 5—An LF347-based voltage-controlled sine-wave oscillator *combines high performance with versatility. For 0 to 10V inputs, this circuit generates 1-Hz to 20-kHz outputs with better than 0.2% linearity and only 0.4% distortion.*

Low-distortion oscillator generates clean sine waves

A_1 functions as a negative-gain inverter and drives a constant current through the platinum sensor. Both the LM329 and the 5.1-kΩ resistor supply the current reference. Because A_1 provides negative gain, the sensor's developed voltage remains extremely low and eliminates self-heating-induced errors.

A_1's output potential—which varies with the sensor's temperature—goes to A_2. In turn, A_2 furnishes scaled gain and offsetting to produce an analog output that ranges from 3 to 6V for a corresponding 300 to 600°C temperature swing at the sensor.

Performing as a voltage-to-frequency (V/F) converter, A_3 and A_4 generate a 300- to 600-Hz output from A_2's 3 to 6V analog output. A_3 integrates in a negative-going direction with a linear slope that depends on A_2's output voltage. Then A_4 compares A_3's negative ramp with the LM329's positive reference voltage by current-summing in the 10-kΩ resistors. When the ramp's negative potential barely exceeds the LM329's reference voltage, A_4's output goes positive. This action turns on the 2N4393 FET and resets A_3's integration process. At A_4, ac feedback causes "hang-up" in the positive state long enough to completely discharge A_3's integrator capacitor.

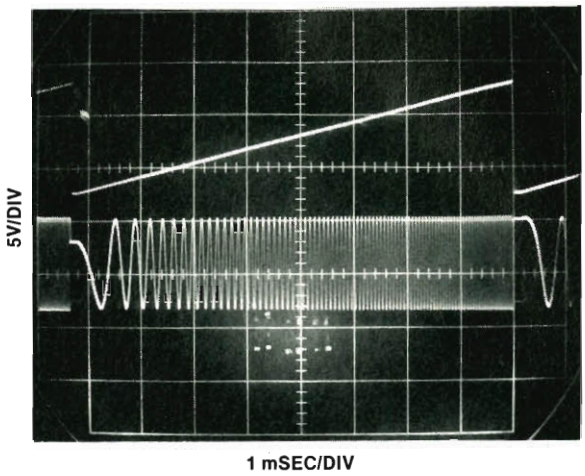
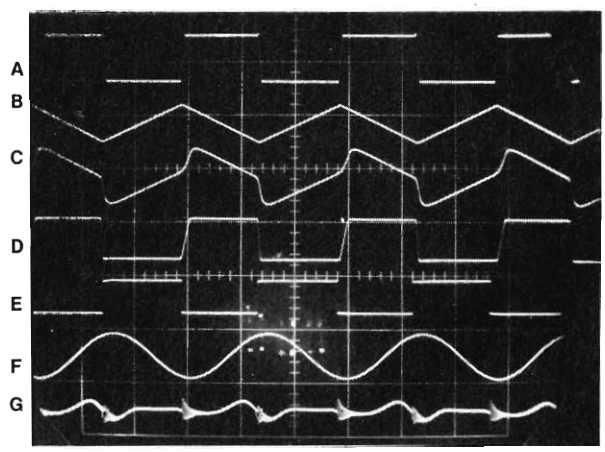


Fig 7—Applying a 10V ramp input (top trace) *to the* ***Fig 5*** *circuit's input produces an extremely clean output (bottom trace) with no glitches, ringing or overshoot, even during or after the ramp's high-speed reset.*

To calibrate this circuit, first substitute a precision decade box (eg, GenRad 1432-K) for the sensor. Next, alternately adjust the Zero (300°C) and Full Scale (600°C) trim potentiometers for the resistance values tabulated in **Fig 4** until A_2's output reaches the correct levels. Finally, adjust the 200-kΩ Frequency Output trimming pot until A_4's frequency outputs correspond to A_2's analog outputs.



TRACE	VERTICAL	HORIZONTAL
A	20V/DIV	
B	20V/DIV	
C	10V/DIV	
D	20V/DIV	20 μSEC/DIV
E	50V/DIV	
F	2V/DIV	
G	0.2V/DIV	

Fig 6—Waveforms from the oscillator shown in Fig 5 *show that upon receiving A_1's negative voltage (trace A), A_2 ramps in a positive direction (B). This ramp joins the ac feedback delivered to A_3's positive input (C); trace D depicts A_3's positive-going output. This output in turn is inverted by the 2N2369 transistor (E), which turns off the 2N4393 and drives A_1's positive input above ground. A_2's triangle output also connects to four sine-shaper transistors and A_4 and finally emerges as the circuit's sine-wave output (F). A distortion analyzer's output (G) shows the circuit's minimum distortion products after trimming.*

Generate clean sine waves

In addition to handling temperature-related tasks, a single LF347 can also find use in a high-performance voltage-controlled sine-wave oscillator **(Fig 5).** For a 0 to 10V input, this circuit produces 1-Hz to 20-kHz sine-wave outputs with better than 0.2% linearity. What's more, distortion totals only 0.4%, and the sine-wave output's frequency and amplitude settle instantaneously for a step input change. In essence, the oscillator circuit generates a sine-wave output by nonlinearly shaping a V/F converter's triangle-wave output.

To understand the circuit's operation, assume the 2N4393 FET is ON and A_1's output has just gone low. A_1's positive input is thus grounded, and A_1 functions as a unity-gain inverter. In this state, its output potential equals $-E_{IN}$ **(Fig 6,** trace A). This negative voltage goes to integrator A_2, which responds by ramping in a positive direction (trace B). A_3 then compares this positive-going ramp to the LM329's 7V reference. The reference works within a symmetrically bounded positive feedback loop, within which the parallel diodes compensate the bridge diodes.

When the positive-going ramp voltage barely nulls

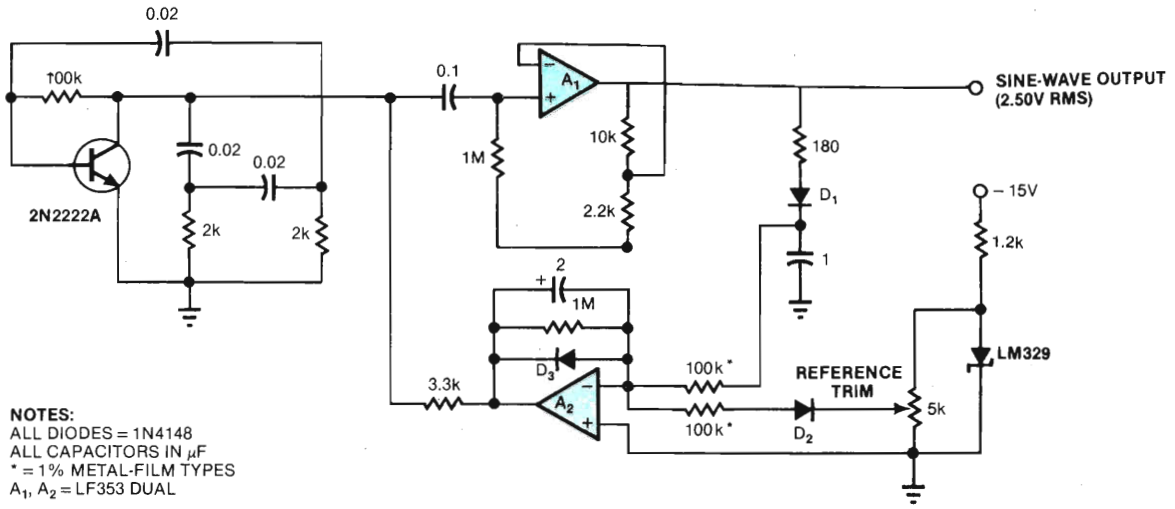


Fig 8—Reduce parts count and save money *by basing this precision sine-wave voltage reference on an LF353 dual FET-op-amp IC. This circuit generates a 1-kHz sine wave at 2.50V rms. The 2N2222A transistor functions as a phase-shift oscillator. The A_1, A_2 combination amplifies and amplitude-stabilizes the circuit's sine-wave output.*

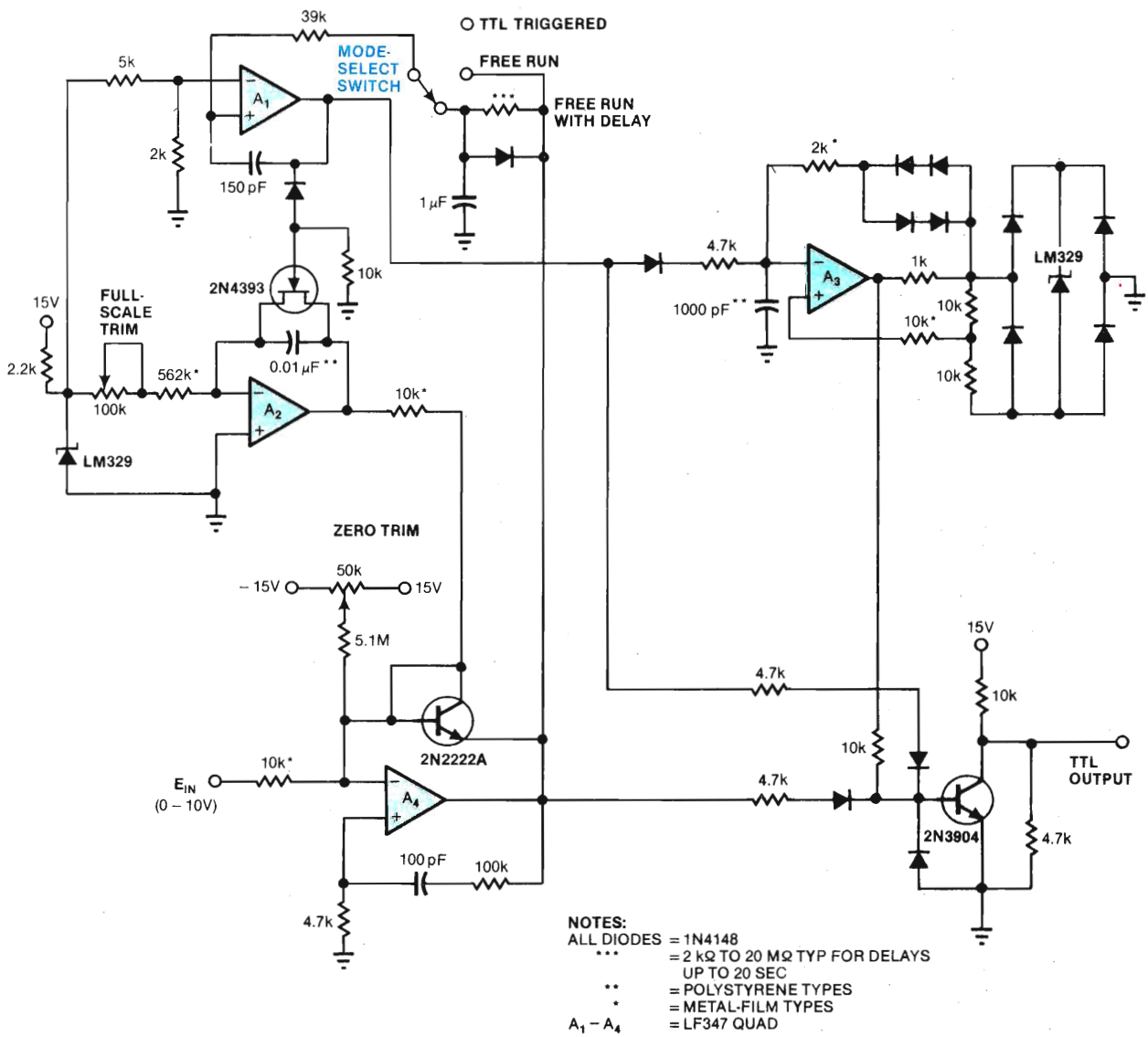


Fig 9—Three Mode Select switch positions *offer a choice of internal or external trigger conditions for this integrating A/D converter. Over 15 to 35°C, this trimmable converter provides a 10-bit serial output, converts in 10 msec and accepts 0 to 10V inputs.*

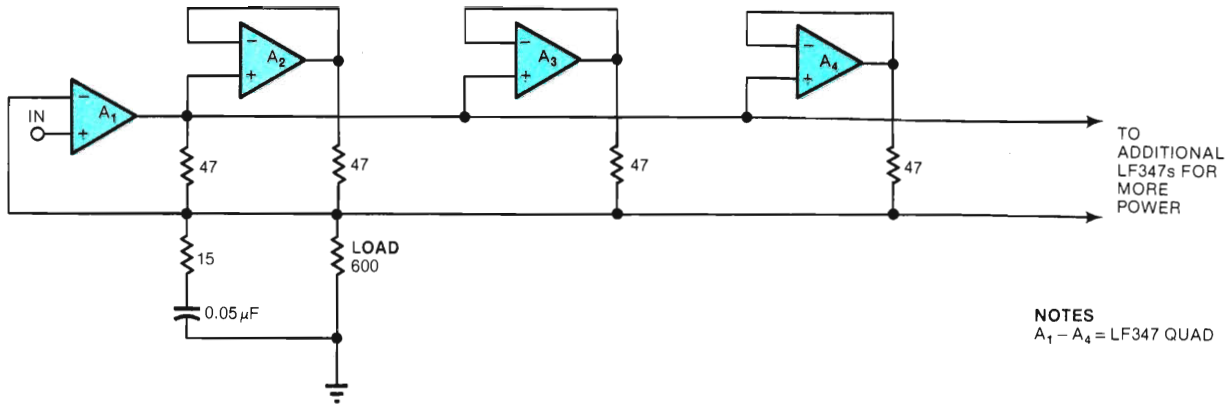


Fig 12—Utilizing current-amplifying capabilities, *one LF347 can drive a 600Ω load to ±11V. For additional power, two LF347s can supply an output current of ±40 mA.*

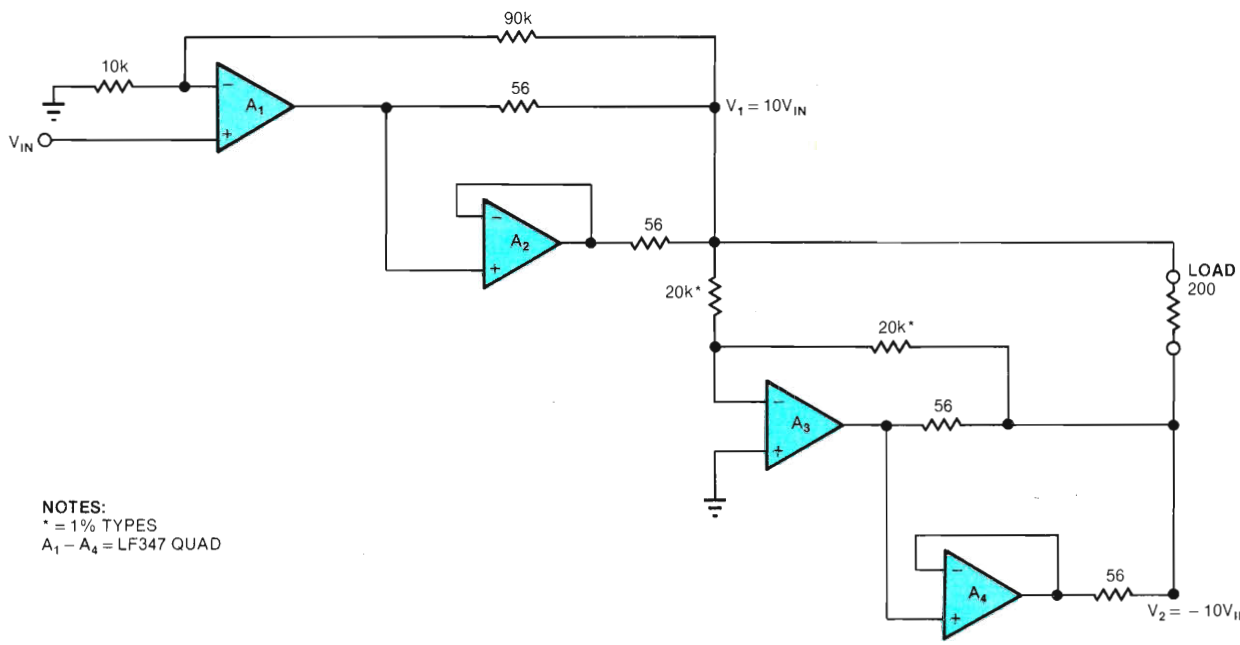


Fig 13—Configured as a high-output-current amplifier *with a gain of 10, this LF347 circuit can drive a 200Ω floating load to ±20V.*

a voltage derived from the LM329 reference. Diode D_2, located in the Reference pot's wiper arm, compensates for D_1. In A_2's feedback loop, D_3 prevents negative voltages from conducting to the transistor and the electrolytic 2-μF feedback capacitor upon start-up.

At a gain of 10, A_2 amplifies the difference between the reference and output signals. Additionally, A_2's output provides collector bias for the 2N2222A, completing an amplitude-stabilizing feedback loop around the oscillator. The electrolytic capacitor furnishes stable loop compensation.

To set the circuit's output amplitude, adjust the 5-kΩ pot until a precision voltmeter reads 2.50V rms at the sine-wave output terminal. For a ±5V variation in either power supply, the sine-wave output shifts less than 1 mV. Other key specs include 250-μV/°C typ drift and less than 1% distortion.

Versatile A/D converter employs quad op-amp IC

In addition to temperature- and oscillator-type circuits, the LF347 quad IC further demonstrates its versatility by implementing an integrating A/D converter (**Fig 9**). Either internally or externally triggered, this circuit delivers a 10-bit serial output word in 10 msec (full-scale conversion time).

To understand this circuit's operation, assume that the Mode Select switch is set to the Free Run With Delay position and the 2N4393 FET has just turned off. The A_2 integrator—biased from the LM329 reference—then begins to ramp in a negative-going direction (**Fig 10,** trace B). A_4 compares this ramp with the positive E_{IN} input voltage. When A_2's ramp potential barely

Obtain high output current using one or more quad packages

exceeds E_{IN}'s negative value, A_4's output goes high (trace C). The 2N2222A transistor provides −0.6V and +7V feedback-output limits for A_4 to keep A_4's output from saturating and aid high-speed response. The ac positive feedback also assures clean transitions.

A_3 performs as a 100-kHz oscillator. Its associated LM329 and diodes provide a temperature-compensated bipolar switching-threshold reference. When A_4 is low, the 2N3904 transistor passes A_3's output pulses to the TTL output terminal. When A_4 goes high, the 2N3904 is biased ON, and the transistor shuts off the output pulses (trace D).

Because A_2 generates a linear output ramp, the time A_4 spends low is directly proportional to E_{IN}'s value. The number of pulses appearing at the 2N3904's output digitally indicates this information. A_2's ramp continues to run after A_4 goes high and, finally, the actual conversion process ends.

When the time-constant capacitor associated with the Free Run With Delay mode charges to 2V, A_1's output goes high (trace A). This transition turns on the 2N4393 FET, which in turn resets integrator A_2. A_1 stays high until the ac feedback provided by the 150-pF capacitor decays below 2V. Then A_1 goes low, A_2 begins to ramp and a new conversion cycle starts.

Resistor/diode gating at the 2N3904's base prevents false data from occurring at the converter's TTL output while A_1 remains high. Additional gating also prevents a ±1-count uncertainty arising from the 100-kHz clock, which runs asynchronously with the conversion cycle. The 1N4148 diode and 4.7-kΩ resistor (connected between A_1's output and A_3's negative input) prevent this error. These components force the oscillator to synchronize to the conversion cycle at each falling edge of A_1's output.

You can adjust the time between conversions in Free Run With Delay mode by changing the RC components connected to this selection-switch position. Moreover, you can trigger the converter externally using a 2V source.

In Free Run mode, the converter self-triggers immediately after A_4 goes high. The conversion time thus varies with the input voltage. Here, a positively biased sine wave (**Fig 11,** trace B) feeds to the converter's input. Because the converter resets and self triggers immediately after converting, A_2's ramp output shapes a ramp-constructed envelope of the input signal (trace C); trace A shows this envelope in a time-expanded form.

In the integrator and oscillator, note that the polystyrene capacitors' −120-ppm/°C temperature coefficients tend to track in the same direction, minimizing the circuit's drift. From 15 to 35°C, the converter achieves 10-bit absolute accuracy.

To calibrate this circuit, apply 10.00V to the input. Then adjust the Full Scale trimming pot for a 1000-pulse output in each conversion cycle. Next, apply 0.05V and adjust the Zero trimming pot for a 5-pulse output in each conversion cycle. Repeat this procedure until the adjustments converge.

Amplifiers supply high output current

Yet another role the LF347 quad can play is as an element in high-output-current amplifiers. **Fig 12** shows a scheme for delivering a large current flow into a load by using all four LF347 amplifiers to supply output power. In this design, A_2, A_3 and A_4 supply the same current as A_1—positive, negative or even zero. As a result, one LF347 can drive a 600Ω load to ±11V, and two LF347s can furnish a ±40-mA output current. The series RC dampers help prevent oscillations.

Similarly, **Fig 13**'s circuit features a gain of 10 and an output to a floating load. A_1 amplifies the input signal, and A_2 helps to drive the 200Ω load. Likewise, A_3 operates as a unity-gain inverter, and A_4 helps A_3 drive the same load. This circuit easily drives the 200Ω floating load to ±20V. **EDN**

Author's biography

Jim Williams is a design engineer with National Semiconductor Corp's Linear Applications Group, Santa Clara, CA, specializing in analog-circuit and instrumentation development. Previously, he worked as an analog systems and circuit consultant at Arthur D Little Inc and directed the Instrumentation Development Lab at the Massachusetts Institute of Technology. Jim studied psychology at Wayne State University. In his spare time, he enjoys tennis, skiing, art and collecting antique scientific instruments.

Article Interest Quotient (Circle One)
High **470** ***Medium*** **471** ***Low*** **472**

Low-cost instrument measures 4-decade power

Using standard parts, a watt/watt-hour meter calculates power consumption for line-powered devices over an extremely wide measurement range—2W to 2 kW FS. And its multiple analog and digital outputs allow both direct and time-related power readings.

Jim Williams, National Semiconductor Corp

If you must monitor the usage of costly electricity in commercial, industrial or consumer equipment designs, build the inexpensive but versatile watt/watt-hour meter described in this article. It resolves power measurements to as low as 0.1W, achieving 2% accuracy over 25±5°C. And it can determine the power consumption of any 115V ac unit, from large factory machines to small hand-held tools. The instrument requires only about $175 worth of off-the-shelf parts, whereas many conventional power meters cost much more and provide lower performance.

To handle a wide variety of power measurements, mostly in cases where energy conservation has high priority, the instrument provides three analog and two digital power-related outputs. One analog output—serving a 200-μA FS meter—displays power values in watts. Another furnishes 0 to 5V for driving strip-chart recorders, while the third supplies instantaneous-power-output levels for use in external-tracking applications. One of the digital outputs—a readout—indicates time-based or watt-hour readings; the second supplies watt-hour data for use by external equipment.

A look at the overall approach

The watt/watt-hour meter's design is straightforward (**Fig 1**). The device under measurement plugs into a standard 115V ac outlet mounted on the instrument's front panel. With line power applied, the ac voltage across the monitored load passes through a resistor divider and feeds (via an op amp) to an analog

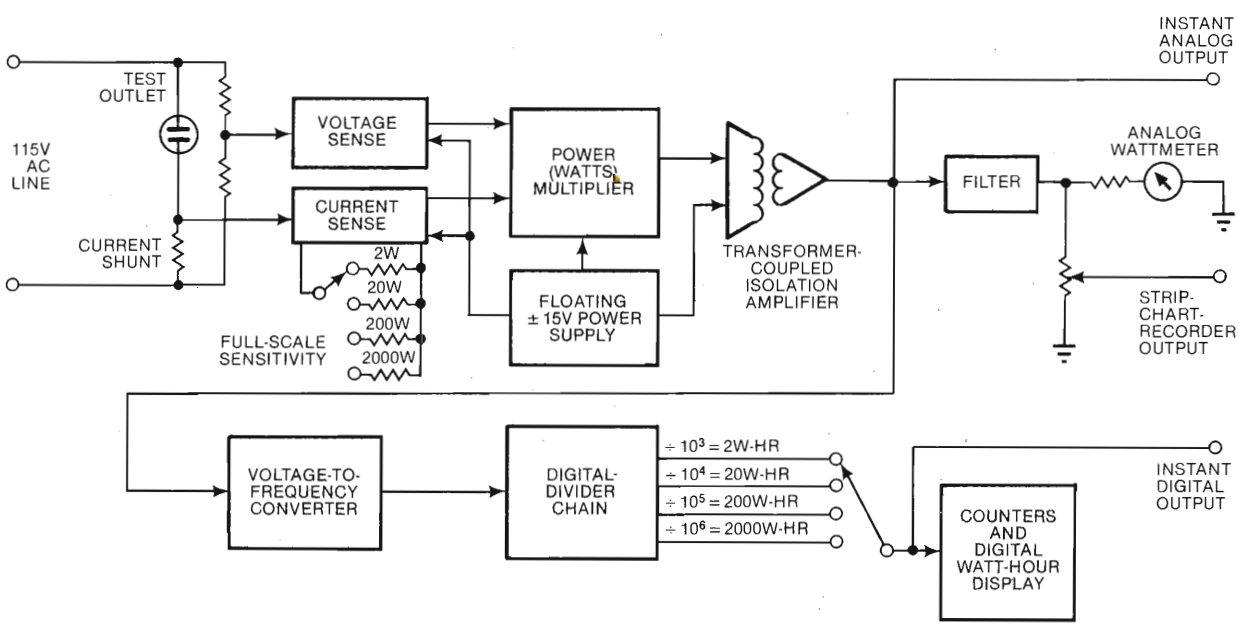


Fig 1—An inexpensive watt/watt-hour meter *incorporates (in series) a current shunt, voltage- and current-sense amplifiers, a power multiplier and a transformer-coupled isolation amplifier. These circuits generate amplitude-modulated pulses that represent the monitored device's instantaneous power consumption, measured in watts. Voltage-to-frequency conversion precedes a counter and a digital display of power levels in watt-hours.*

Single low-resistance shunt handles all four power ranges

power multiplier.

The voltage across a low-resistance shunt represents the current through the load. Even when measuring a 20A max flow, this shunt needs only 133 mV—a feature that eliminates high-resistance-current-shunt inaccuracies. Additionally, by accommodating all four power ranges—2, 20, 200 and 2000W FS—the single shunt eliminates the need to switch-in high-impedance shunts for high-sensitivity scales.

The instrument's measurement technique utilizes the low input error in a current-sense amplifier, whose output also goes to a power multiplier. Switchable gain within the amplifier makes possible the 4-decade sensitivity setting. A 4-quadrant configuration, the power multiplier produces an output representing the test load's true instantaneous-power product (E×I), regardless of the load's relative voltage and current phases.

Because the multiplier and its associated voltage- and current-sense amplifiers connect directly to the ac line, though, they require a floating ±15V power supply. Consequently, you can't safely monitor their outputs with grounded test equipment, such as strip-chart recorders. To deal with this problem, the multiplier's output drives an isolation amplifier that operates at unity gain but has no galvanic connection between its input and output terminals. The amplifier employs pulse-amplitude-modulation techniques in conjunction with a small transformer. By grounding its output, you can safely connect test equipment to all circuits following the transformer.

In addition to driving an analog meter and a strip-chart recorder, the isolation amplifier's output also biases a voltage-to-frequency (V/F) converter, which in turn combines with digital counters to form a digital integrator. This circuit translates the amplifier's analog outputs into time-related power levels. Varying the counters' divide ratio (and thus the power levels) produces the instrument's four watt-hour ranges.

Multiplier portrays instant power

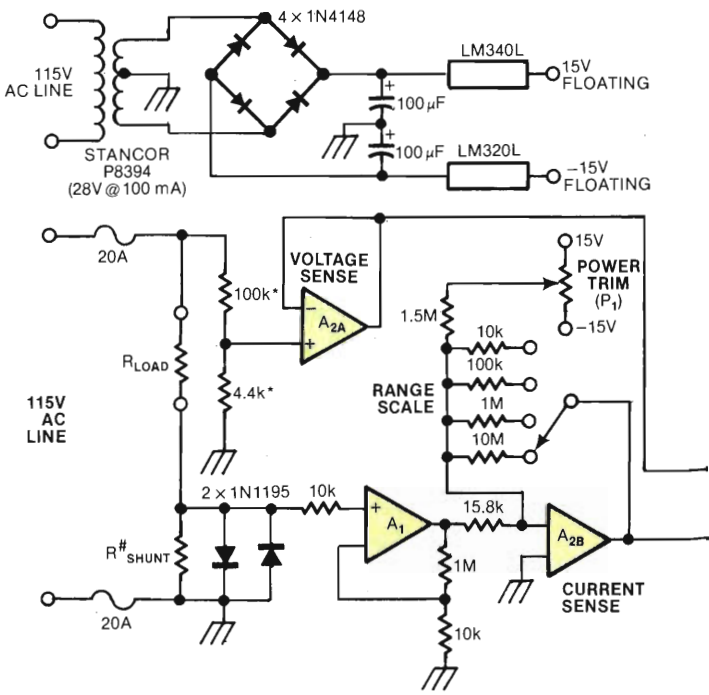
The hardware implementation of this overview appears in **Fig 2.** At the ac-line input, voltage division occurs in the 100- and 4.4-kΩ resistor string. Connected to this string, A_{2A} serves as a buffer amplifier and feeds the voltage-sense input to the power multiplier. Also working off the line input, A_1 monitors the voltage across the current shunt at a fixed gain of 100. Two 1N1195 diodes and two 20A fuses protect A_1 and the current shunt from shorts across the load's test socket. Receiving A_1's output, amplifier A_{2B} provides gain, calibrated wattage switching from 2 to 2000W FS and the power multiplier's current-sense input.

Composed of amplifiers A_{3C} and A_{3D} and an LM394 IC's dual transistors, the multiplier—a variable transconductance type—uses its current-sense input to vary a 2N2222 transistor amplifier's gain. This amplifier receives A_{2A}'s voltage-sense output as its input.

At the multiplier's output, A_{3C} produces an output representing the load's instantaneous power consumption (**Fig 3,** trace A). This output in turn biases a pulse-amplitude-modulating isolation amplifier (A_{3A} and A_{3B}) and three transistors (Q_1 to Q_3).

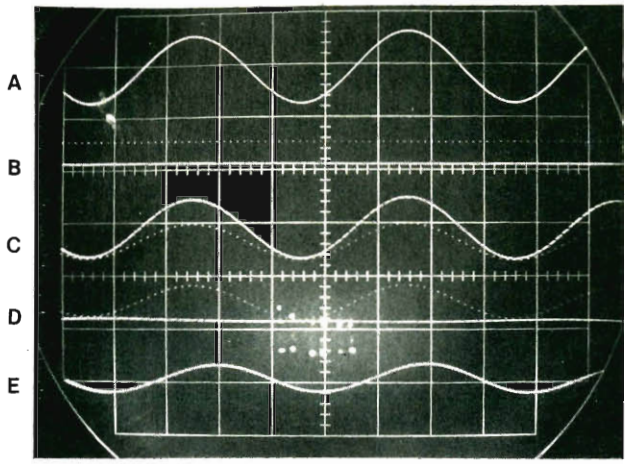
Generating an oscillator output (trace B), A_{3A} biases the Q_1/Q_2 switch connected across the transformer's primary. Meanwhile, A_{3B}'s negative input measures the pulses' amplitude at the transformer's primary. A_{3B} then servo-controls the pulses to the same amplitude as those received at its positive input (biased by the multiplier's output). Transistor Q_3 provides current-drive capability and completes A_{3B}'s feedback path.

Trace C in **Fig 3** illustrates how Q_3's emitter voltage changes to meet the servo-loop requirements. Trace D shows the pulses applied to the transformer. Note that these pulses' amplitudes form an envelope whose amplitude equals the multiplier's output.



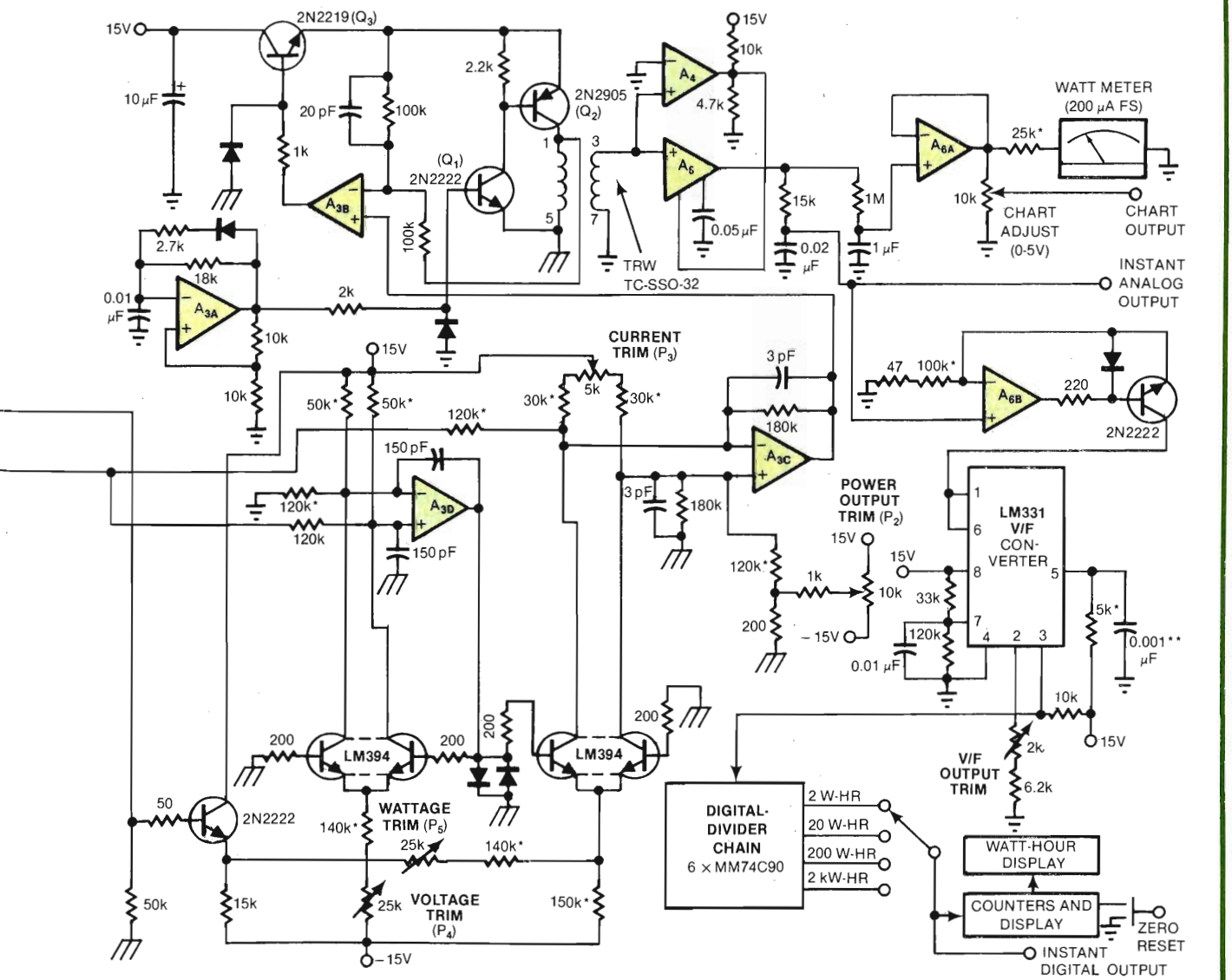
NOTES:
ALL DIODES 1N4148
⏚ = FLOATING CHASSIS GROUND
⏚ = CIRCUIT (EARTH) GROUND
* = 1% FILM TYPES
** = POLYSTYRENE TYPE
\# = GE 50-140034NDAA
A_1 = LM11
A_2 = LF353 DUAL
A_3 = LF347 QUAD
A_4 = LM311
A_5 = LF398
A_6 = LF353 DUAL

Fig 2—Careful parts selection and skillful circuit design *produce a test instrument that measures the power consumption of any 115V ac-powered device. The instrument provides a 4-decade power-measuring range—2, 20, 200 and 2000W FS—at 2% accuracy and over 25±5°C. Three analog and two digital outputs accommodate a wide variety of internal and external power-measurement applications.*



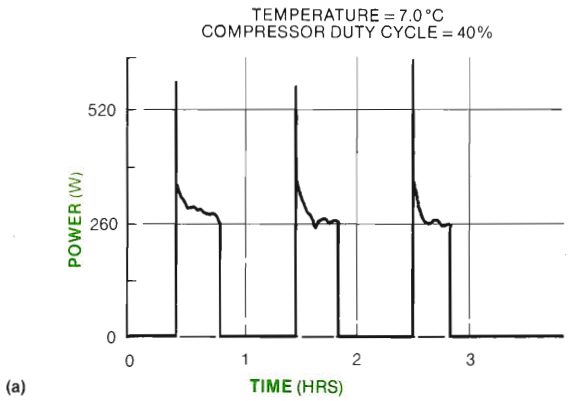
TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	
B	50V/DIV	
C	5V/DIV	2 mSEC/DIV
D	10V/DIV	
E	10V/DIV	

Fig 3—During instrument operation, the power multiplier's output *(trace A) represents the monitored device's instantaneous power consumption. Biased by this output, A_{3A}'s oscillator output (refer to* **Fig 2***) biases the Q_1/Q_2 switch (trace B). Completing the feedback path to A_{3B}, Q_3 changes its emitter voltage to maintain servo-loop needs. Via Q_1, Q_2, Q_3, A_{3A} and A_{3B}, amplitude-modulated pulses arrive at the isolation transformer's primary (trace D). Connected to this transformer's secondary, A_5's output represents a sampled version of the monitored device's power consumption (E).*

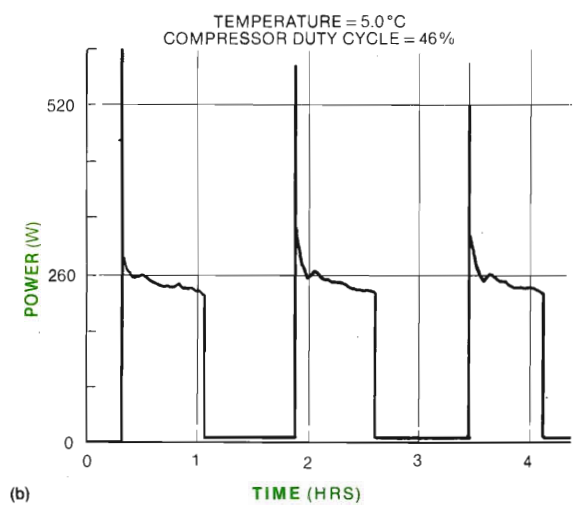


Pulse sampling and filtering smooth out power-signal levels

The amplitude-modulated pulses appear at the transformer's secondary, which is referenced to the instrument's earth ground. Each pulse's amplitude gets measured by a sample/hold amplifier (A_5) whenever A_4 generates a Sample command. Lightly filtered by the 15-kΩ, 0.02-μF network, A_5's output provides a sampled version of the load's instantaneous power consumption (trace E). Heavy filtering by the 1-MΩ, 1-μF network's time constant produces a smoother version of the sampled power signal. This signal drives the watts analog-meter and strip-chart-recorder outputs via the A_{6A} buffer.



(a)

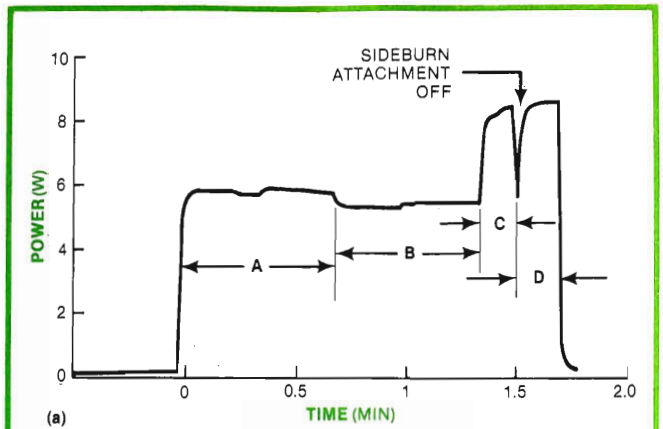


(b)

TEMPERATURE (°C)	POWER CONSUMED (W)	kW-HR PER CYCLE	COST PER DAY	COST PER YEAR
7	260	0.104	$0.0998	$36.44
5	260	0.119	$0.1147	$41.89

(c)

Fig 4—Connected to the instrument's Chart Output terminal, *a strip-chart recorder logs a refrigerator compressor's power consumption at 260W for several hours. At a 7°C temperature setpoint, the compressor functions at a 40% duty cycle* ***(a);*** *lowering the temperature to 5°C increases this duty cycle to 46%* ***(b).*** *Extrapolated data* ***(c)*** *shows that the lower temperature results in increased kilowatt-hour consumption per cycle and therefore in higher operating cost.*



(a)

FACIAL AREA	POWER CONSUMED (W)	WATT-HOURS	COST PER SHAVE* (CENTS)
CHEEKS (A)	5.8	0.173	0.00692
UPPER & LOWER LIPS (B)	5.4	0.123	0.00492
RIGHT SIDEBURN (C)	8.4	0.063	0.00252
LEFT SIDEBURN (D)	8.4	0.061	0.00244

*BASED ON $0.04 PER kW-HR

(b)

Fig 5—Monitoring the power consumption *of a small electric razor via a strip-chart recorder, the watt/watt-hour meter generates instantaneous readings over short intervals* ***(a).*** *With this accumulated data, you can make detailed power-cost calculations* ***(b).***

In conjunction with a digital-divider chain, an LM331 V/F converter forms a digital time integrator. To bias the V/F converter, A_5's lightly filtered output goes to A_{6B}. Driven by the V/F converter's output, the divider chain sets the integrator's time constant and switches the scale factor for watt-hour measurements. Additional counters drive a digital readout that shows the actual measurements. Pressing the Zero Reset pushbutton resets the watt-hour readout.

Use this procedure for calibration

To calibrate the watt/watt-hour meter, shut off the instrument's ac line power and remove the two 20A fuses. Set the Range Scale switch to 2. Then apply power and adjust the Power Trim pot (P_1) so 0.00V appears at A_{2B}'s output.

Turn off the ac line power. Then disconnect the power multiplier's two input lines and connect them to the instrument's floating ground. Turn on line power and adjust the Power Output Trim pot (P_2) for 0.00V at A_{6A}'s output.

Once more, turn off ac line power. Unground the multiplier's current-sense input but leave the voltage-sense input grounded. Then turn on line power and apply a 10V p-p 60-Hz signal to the multiplier's current-sense input lead. Adjust the Current Trim pot (P_3) for 0.00V at A_{6A}'s output.

Now turn off ac line power yet again, ground the multiplier's current-sense input and unground the voltage-sense input. Turn on the power and adjust P_4 (the Voltage Trim pot) for 0.00V at A_{6A}'s output. Then turn off the power and reconnect the multiplier's current-sense input into the circuit.

Next, turn on the line power and read ac line voltage with a precision digital voltmeter. Plug a known load

V/F converter and divider chain form a digital integrator circuit

(eg, a 1% power resistor) into the instrument's test outlet. Adjust the Wattage Trim pot (P_5) until the analog meter reads the correct wattage (watts equals line voltage times load resistance).

Finally, turn off line power and disconnect A_{6B}'s positive input line. Then turn on the power and apply 5.00V to A_{6B}'s positive line. Adjust the V/F Output Trim pot (P_6) until the LM331's output at pin 3 runs at 27.77 kHz. Then turn off line power and reconnect A_{6B}'s positive input line.

A watt/watt-hour meter calibrated in this manner can accurately measure the power consumption of any 115V ac-powered device, large or small. Connecting the instrument to a home refrigerator demonstrates its prowess with large equipment: In one test, the refrigerator operated for 3½ hrs at a temperature setpoint of 7°C (**Fig 4**), and each time its compressor turned on, it consumed approximately 260W. As the compressor warmed up, power consumption actually decreased slightly. Changing the refrigerator's temperature control to 5°C increased the compressor's duty cycle by 15%. This power change reflects directly in the unit's per-cycle kilowatt-hour consumption.

Connecting the watt/watt-hour meter to an electric razor demonstrates its ability to monitor small equipment. In this setup, the meter recorded the electric razor's power consumption during a face-shaving exercise (**Fig 5**). Note that various facial areas cost more to shave than others.

Time-related power computations revealed that a complete daily shave costs about $0.09 per year. If this is excessive, a user could economize by growing a beard. **EDN**

Author's biography

Jim Williams is a design engineer with National Semiconductor Corp's Linear Applications Group, Santa Clara, CA, specializing in analog-circuit and instrumentation development. Previously, he worked as an analog-systems and -circuit consultant at Arthur D Little Inc and directed the Instrumentation Development Lab at the Massachusetts Institute of Technology. Jim studied psychology at Wayne State University and in his spare time enjoys skiing, art and collecting antique scientific instruments.

Article Interest Quotient (Circle One)
High **479** ***Medium*** **480** ***Low*** **481**

Apply sample-and-hold techniques for elegant design solutions

More than just a data-acquisition device, a S/H amplifier can also simplify—indeed, make possible—other circuit designs. The applications presented here provide a sampling of ideas ranging from data-link eavesdropping to oven control.

Jim Williams, National Semiconductor Corp

Most designers regard sample/hold amplifiers merely as system components utilized in high-speed data-acquisition work. But they should also consider S/H devices' possibilities as circuit-oriented building blocks.

Sampling techniques can implement circuit functions that are sophisticated in performance, low in cost and not easily realized with other approaches. The designs presented here illustrate a few of the many application possibilities for S/H amplifiers as circuit elements.

Stop fiber-optic eavesdropping

Fig 1 depicts a design that detects attempts to tap a fiber-optic data link. Because the circuit works with pulse-encoded data formats, it detects only short-term changes in the fiber-optic cable's loss characteristics. Thus, long-term changes arising from temperature variations or component aging won't trigger the alarm, but any unauthorized data extraction—a short-term phenomenon—will.

Under normal operating conditions, because the input light pulse's amplitude is constant, so is the level detected by photodiode D_1 and amplified by A_6. A_6's constant-amplitude output pulses are sampled by the S/H amplifier, A_3, which is driven by a delayed S/H pulse generated by A_1 and A_2. (Delaying the sampling ensures that A_6's output settles completely.) Unless

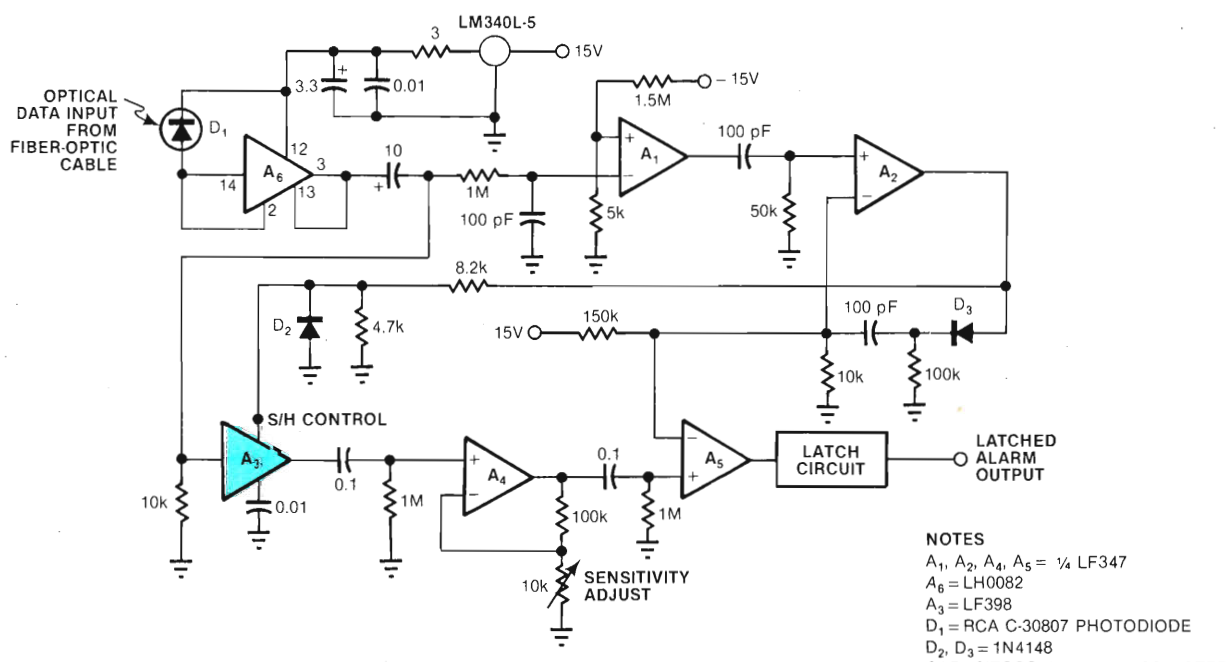


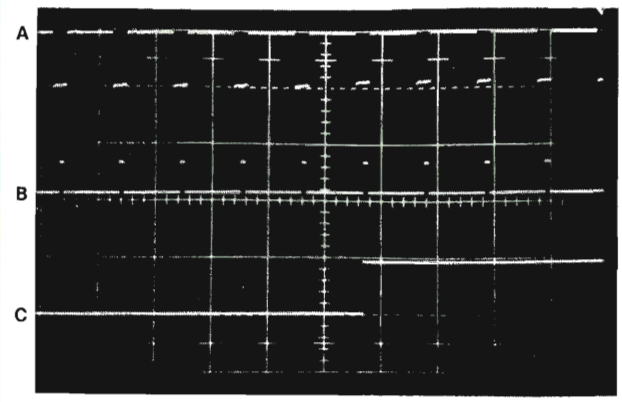
Fig 1—Fiber-optic-link eavesdropping attempts *are immediately detected by this design. Working on a pulse-by-pulse comparison basis, A_3 samples each input pulse and holds its amplitude value as a dc level. Anything that disturbs the next input's amplitude causes a jump in this level; because A_4 is an ac-coupled amplifier, the comparator and latch then activate.*

Sample/hold techniques benefit fiber-optics usage

something changes the input light pulse's amplitude, A_3's output is a dc voltage; because A_4 is ac coupled, its output is 0V.

A link-intrusion attempt disturbs the input pulse's amplitude, causing A_6's output to shift. A_4 ac-amplifies this shift, trips comparator A_5 and activates the alarm latch.

This sequence is represented in **Fig 2,** where trace A is A_6's output, B tracks A_3's S/H control pin and C is the alarm's output. An input disturbance occurs slightly past trace A's midpoint, indicated by A_6's reduced output. The alarm's output latches HIGH just after the Sample command rises—a result of the S/H amplifier's level jumping to A_6's changed output. **Fig 2** shows a large disturbance (10%) for demonstration purposes, but in practice, the design can detect an energy loss of as little as 0.1%.



TRACE	VERTICAL	HORIZONTAL
A	0.1V/DIV	500 μSEC/DIV
B	10V/DIV	500 μSEC/DIV
C	5V/DIV	500 μSEC/DIV

Fig 2—An intrusion attempt *occurring just past the midpoint of trace A is immediately detected by* **Fig 1***'s circuit. The photodetector's amplifier output (A) shows a slight amplitude drop. The next time the S/H amplifier samples this signal (B), the alarm latch sets (C).*

Stretching pulses proportionally

You can measure short-duration pulses with another S/H circuit, shown in **Fig 3.** The design works for either single-shot or repetitive events.

Assume that you must measure a 1-μsec-wide pulse to an accuracy of 1%. With digital techniques, this task would require use of a 100-MHz clock (1% of 1 μsec). **Fig 3**'s design avoids this requirement by linearly amplifying the pulse's width by a factor of 1000 or more. Thus, a 1-μsec input pulse becomes a 1-msec output pulse—a somewhat easier time duration to measure to 1% accuracy.

Fig 4 shows how this design responds to an even shorter (350 nsec) input pulse (trace A). Comparator A_1's output goes LOW (B), and the 74121-one-shot/Q_1 combination discharges the associated 100-pF capacitor via a 50-nsec pulse (D). Concurrently, Q_2 turns off, allowing current source Q_3 to start linearly recharging

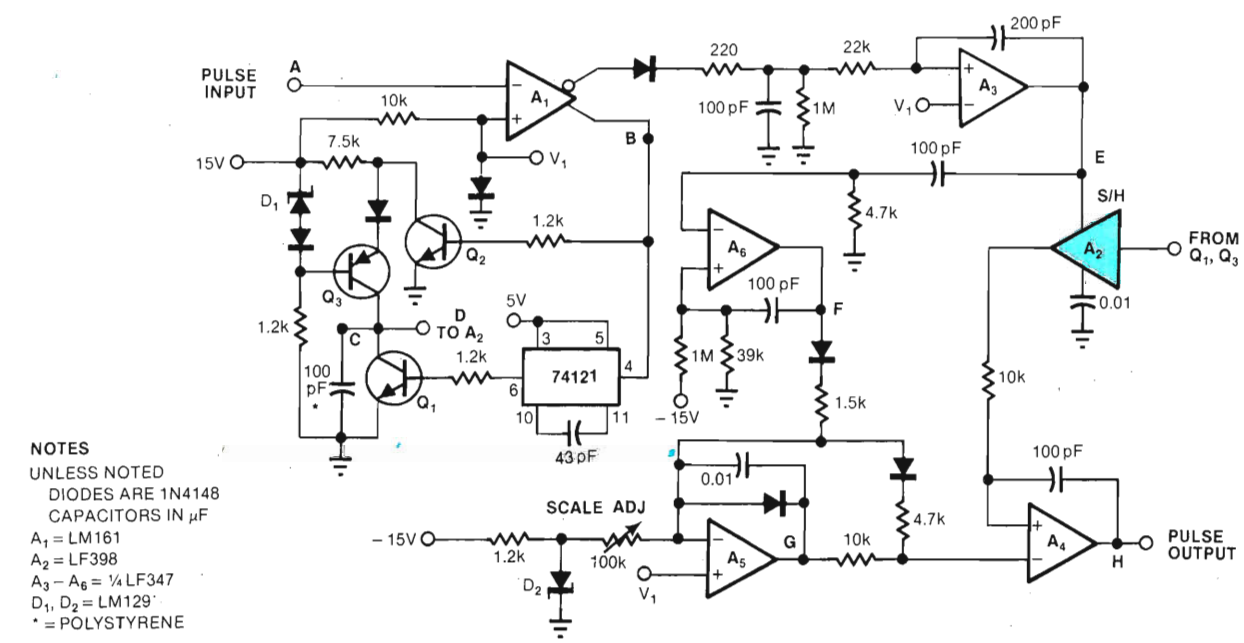
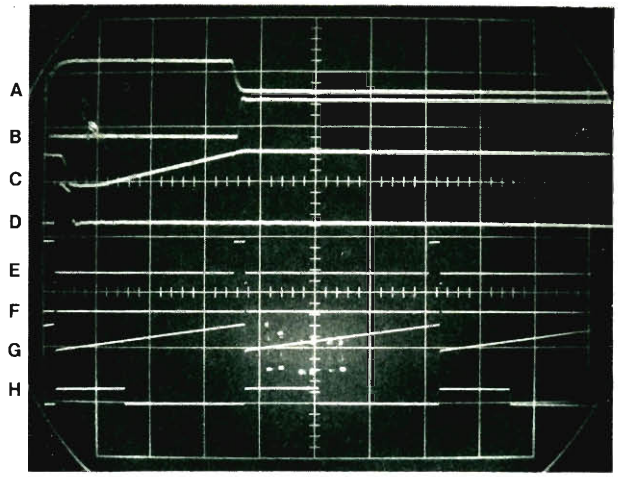


Fig 3—Pulse-width-measurement accuracy *is enhanced by this pulse-stretching circuit. A short input pulse triggers the 74121 one-shot and (via Q_1) discharges the 100-pF capacitor while concurrently turning on the recharging current source, Q_3. So long as the input pulse is present, the capacitor charges; when the pulse ends, the capacitor's voltage is proportional to the pulse's width. S/H amplifier A_2 samples this voltage, and the resultant dc level controls the ON duration of the A_4/A_5 pulse-width modulator. (Letters at key points in the circuit refer to waveforms shown in* **Fig 4.**)

the 100-pF capacitor (C). Charging continues until the input pulse terminates, which causes A_1's output to again go HIGH and cut off the current source. The voltage across the capacitor is then directly proportional to the input pulse width; S/H amplifier A_2 samples this voltage when A_3 generates the command shown by trace E. (Note the horizontal scale's change.) A_3's input derives via a delay network from A_1's inverting output, completing the sampling cycle.

A_2's dc output voltage represents the most recently applied input pulse's width. This voltage feeds to A_4, which works with A_5 as a voltage-controlled pulse-width modulator. A_5's output ramps positive (G) until reset by a pulse from A_6. (A_6 goes HIGH briefly (F) each time A_3's output (E) goes LOW.) To generate the circuit's final output, A_4 compares A_6's output with A_2's and produces a HIGH level (H) for a time linearly dependent upon A_2's output.

With the component values shown in **Fig 3**, the input-to-output time-amplification factor equals approximately 2000. Thus, a 1-μsec input yields a 1.4-msec output. Absolute accuracy is 1% (10 nsec) referred to the input, and the measurement's resolution extends down to 2 nsec. The 74121 one-shot's 50-nsec pulse limits the minimum measurable pulse width.



TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	100 nSEC/DIV
B	5V/DIV	100 nSEC/DIV
C	5V/DIV	100 nSEC/DIV
D	5V/DIV	100 μSEC/DIV
E	50V/DIV	500 μSEC/DIV
F	50V/DIV	500 μSEC/DIV
G	20V/DIV	500 μSEC/DIV
H	100V/DIV	500 μSEC/DIV

Fig 4—A sequence of events *in* ***Fig 3****'s circuit stretches a 350-nsec input pulse (A) by a factor of 2000. When triggered, comparator A_1 goes LOW (B). This action starts the recharging of a capacitor (C) after its previously stored charge has been dumped (D). When the input pulse ends, the capacitor's voltage is sampled under control of a delayed pulse (E) derived from the input amplifier's inverting output (F). The sampled and held voltage then turns off a voltage-controlled pulse-width modulator (G), and a stretched output pulse results (H).*

Control a pulse's amplitude

S/H amplifiers also make possible the amplitude-stabilized pulse generator shown in **Fig 5;** this circuit drives 20Ω loads at levels as high as 10V pk. The pulse's adjustable amplitude remains stable over time, temperature and load changes.

The circuit functions by sampling the output pulse's amplitude and holding this value as a dc voltage. This voltage then connects to a feedback loop that controls the output switching devices' supply voltage.

Specifically, an input TTL-level pulse turns on output drivers Q_2 and Q_3 and simultaneously places S/H amplifier A_1 in Sample mode. When the input pulse ends, A_1 outputs a dc voltage that represents the output pulse's amplitude. A_2 compares this level with the one

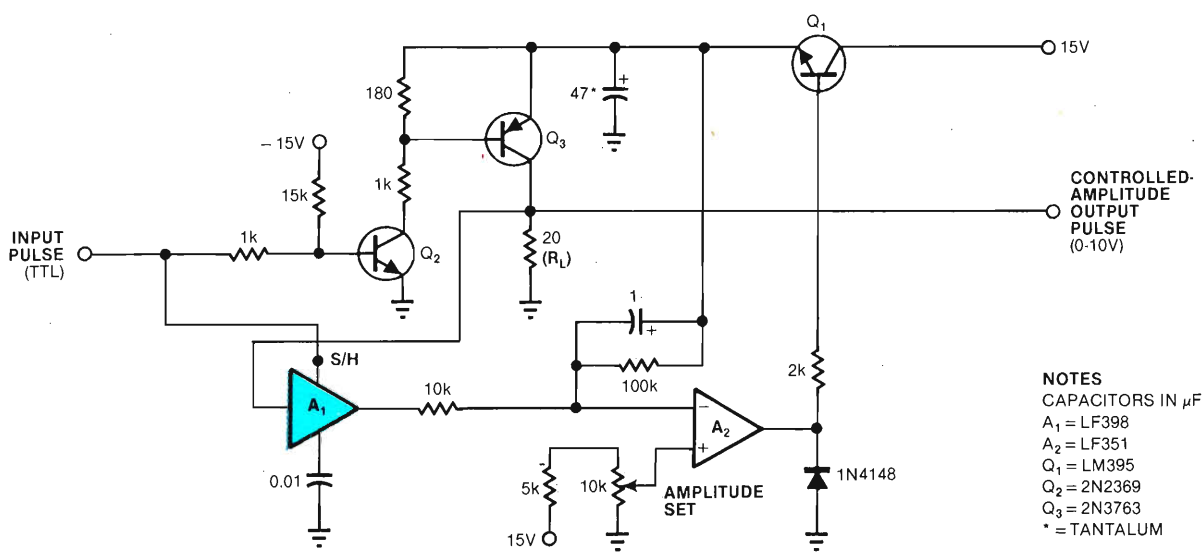
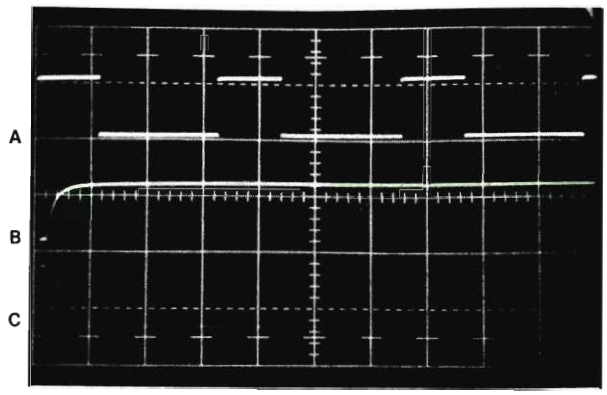


Fig 5—Pulse-amplitude control *results when this circuit samples an output pulse's amplitude and compares it with a preset reference level. When the output exceeds this reference, A_2 readjusts switching transistor Q_3's supply voltage to the correct level.*

established by the Amplitude Set adjustment; A_2 drives emitter follower Q_1, which provides the dc supply voltage to output switches Q_2 and Q_3. This servo action forces the output pulses' peak amplitude to equal the "set" value, regardless of Q_3's losses or output loading.

Fig 6's trace A shows the pulser's overall output wave shape, and traces B and C detail the clean 50-nsec rise and fall times. (Note the horizontal scale change.)



TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	1 mSEC/DIV
B	10V/DIV	100 nSEC/DIV
C	10V/DIV	100 nSEC/DIV

Fig 6—A 10V, 0.5A pulse (A) *is amplitude-stabilized by the S/H technique depicted in* **Fig 5.** *Note the clean 50-nsec rise (B) and fall (C) times.*

Input isolation made easy

Fig 7 shows a powerful extension of the pulse-amplitude-control scheme that permits you to measure low-level signals (eg, thermocouple outputs) in the presence of common-mode noise or voltages as high as 500V. Despite the input terminals' complete galvanic isolation from the output, you can expect a 0.1% transfer accuracy. And by using the optional low-level preamp (A_1), you can measure inputs as low as 10 mV FS.

The circuit works by generating a pulse train whose amplitude is linearly related to the input signal's amplitude. This pulse train drives the input-to-output isolating transformer, T_1. T_1's output, demodulated to a dc level, provides the circuit's system-ground-referenced output. The pulse train's amplitude is controlled by a loop similar to the one employed in the pulse-amplitude-servo design. Here, however, the Amplitude Set doesn't appear, and the servo amplifier's + input becomes the signal input.

Set up as an oscillator, A_2 generates both the sample pulse for S/H amplifier A_3 and the drive for switches Q_2 and Q_3 (**Fig 8**, trace A). The feedback to the pulse-amplitude stabilizing loop comes from T_1's isolated secondary—a trick that ensures highly accurate amplitude-information transfer despite T_1's or Q_2's losses.

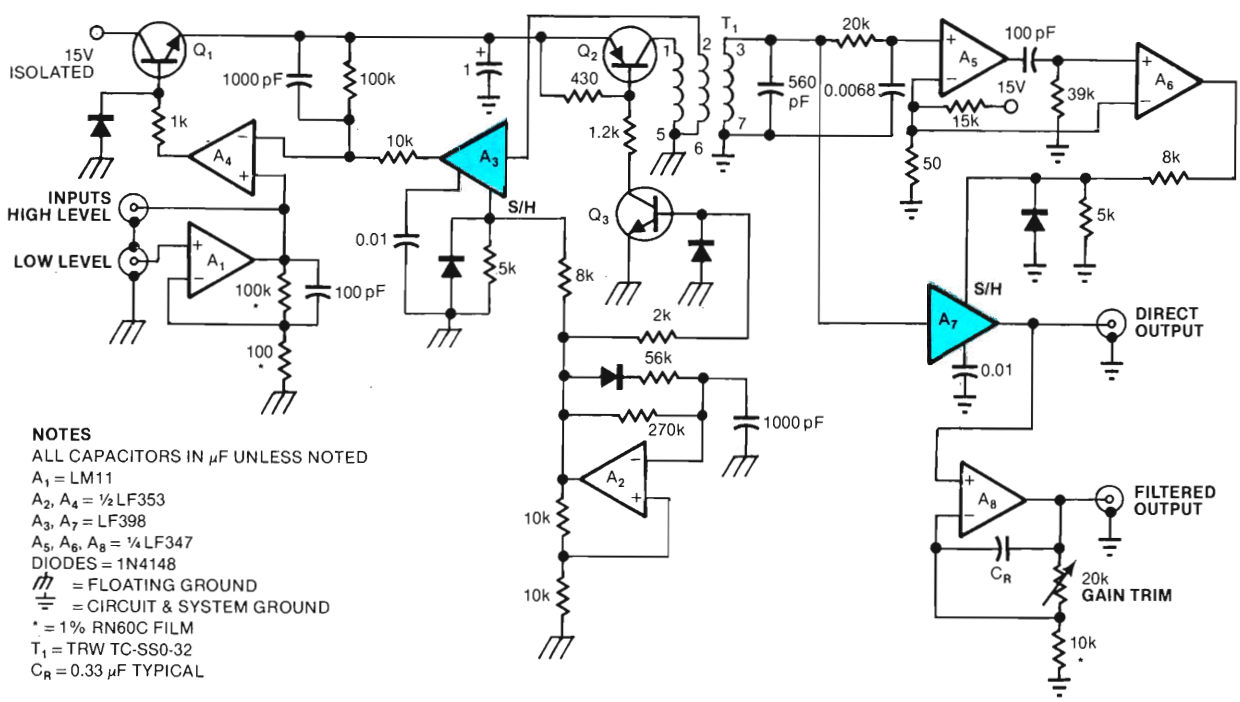
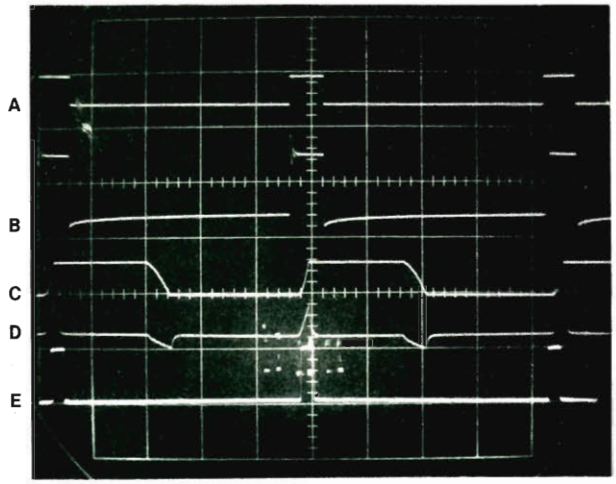
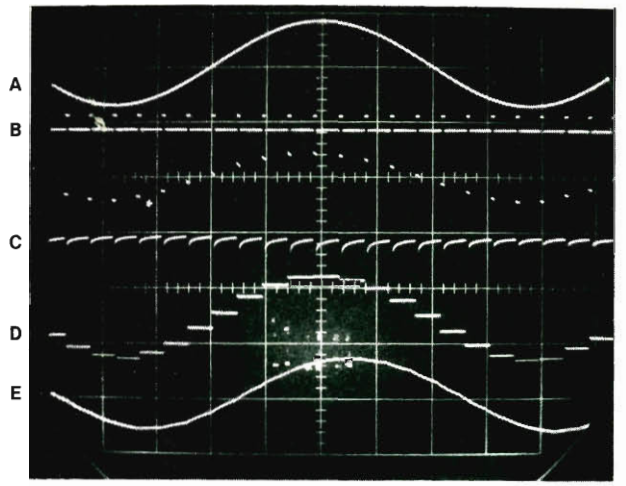


Fig 7—Obtain input-signal isolation *using this circuit's dual-S/H scheme. Analog input signals amplitude-modulate a pulse train using a technique similar to that employed in* **Fig 5**'s *design. This modulated data is transformer coupled—and thereby isolated—to a dc filter stage, where it's resampled and reconstructed.*



TRACE	VERTICAL	HORIZONTAL
A	50V/DIV	100 μSEC/DIV
B	1V/DIV	100 μSEC/DIV
C	50V/DIV	100 μSEC/DIV
D	10V/DIV	100 μSEC/DIV
E	5V/DIV	100 μSEC/DIV

Fig 8—Fig 7's in-circuit oscillator (A_2) *generates both the sampling pulse (A) and the switching transistors' drive. Modulated by the analog input signal, Q_2's (and therefore T_1's) output (B) is demodulated by S/H amplifier A_7. A_5's output (C) and A_6's input (D) and output (E) provide a delayed Sample command.*



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	100 mSEC/DIV
B	100V/DIV	
C	5V/DIV	
D	5V/DIV	
E	5V/DIV	

Fig 9—Completely input-to-output isolated, ***Fig 7's*** *circuit's analog input signal (A) is sampled by a clock pulse (B) and converted to a pulse-amplitude-modulated format (C). After filtering and resampling, the reconstructed signal (D) is available smoothed (E).*

S/H amplifier A_7 demodulates the amplitude-encoded signal at T_1's output (B) back to a dc level. A_5's output (C) and A_6's + input (D) and output (E) provide A_7's delayed Sample command. A_8 furnishes an optional gain-trimmed and filtered output.

Fig 9 illustrates the design at work. Here, the input signal (trace A) is a dc-biased sine wave. Trace B shows A_2's output clock pulse, and A_7's Sample command

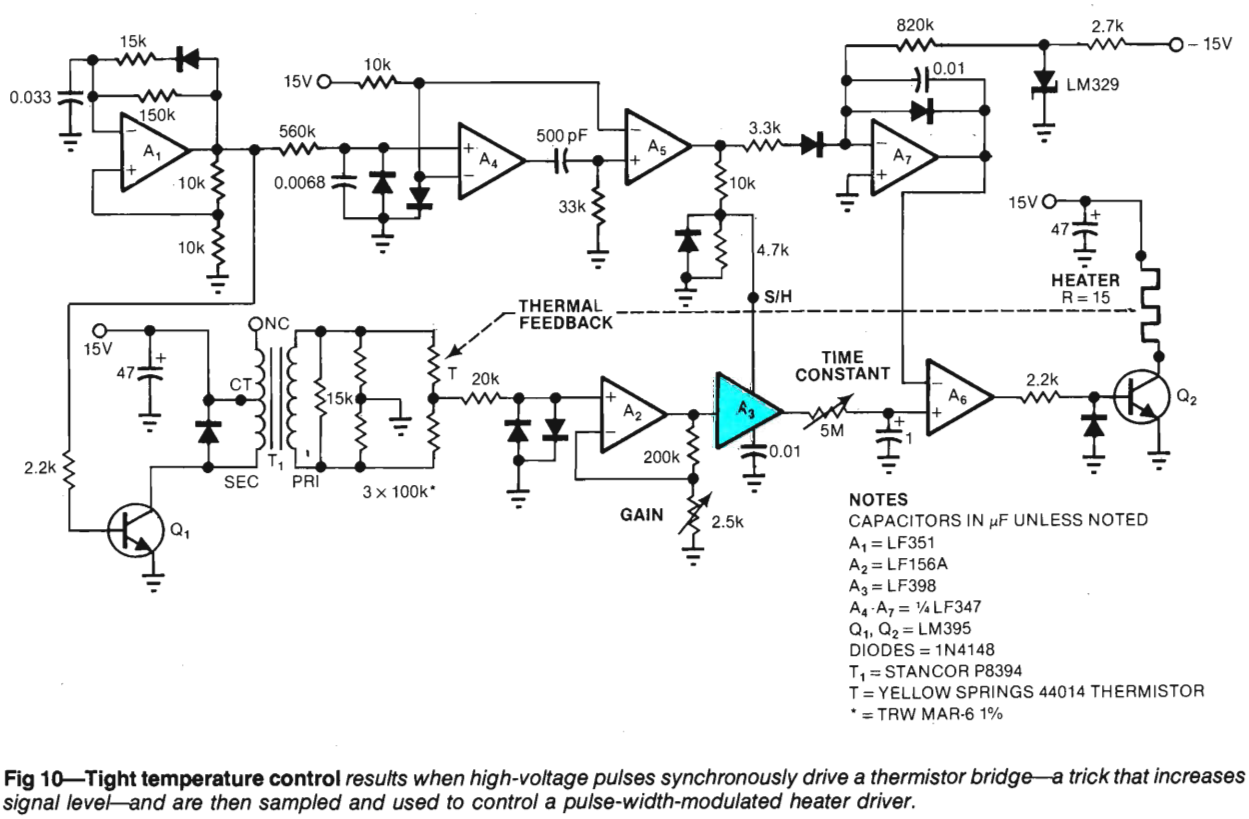


Fig 10—Tight temperature control *results when high-voltage pulses synchronously drive a thermistor bridge—a trick that increases signal level—and are then sampled and used to control a pulse-width-modulated heater driver.*

Sampling oven temperature tightens stability

appears as trace C. A_7's reconstructed output is shown as trace D and A_8's filtered output as trace E.

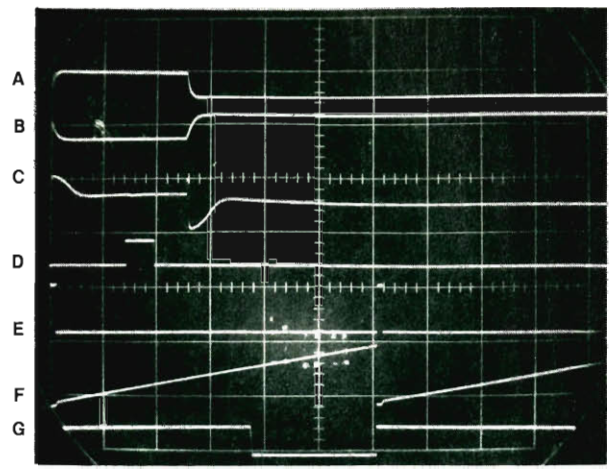
Sampling holds the temperature

The S/H-based high-stability oven-temperature controller shown in **Fig 10** embodies two unusual concepts:

- High-voltage, low-duty-cycle pulses drive the circuit's bridge and thus provide low power dissipation and high output levels. (In contrast, the power-dissipation limits of the resistors and thermistors in standard thermistor-bridge designs define the maximum dc bias level and therefore the maximum recoverable signal.)
- A S/H amplifier performs as a synchronous detector in the circuit's servo feedback loop. And because the sampling pulse establishes the design's reference level as well as the sampling interval, even the usual drift problems don't arise.

The circuit generates pulses via the oscillator-A_1/amplifier-Q_1 combination, driving a standard 24V transformer (T_1) "backwards." The transformer applies a floating 100V pulse across the thermistor bridge. Because one side of the bridge's output is grounded, this signal becomes the pair of complementary 50V pulses shown in **Fig 11** (traces A and B).

Amplified by A_2 (**Fig 11**, trace C), the bridge's output feeds to S/H amplifier A_3, whose dc output level equals A_2's peak output. (The A_4 and A_5 stages and their associated RC networks control the timing of A_3's Sample command (D).) After low-pass filtering, A_3's output (E) connects to a pulse-width modulator consisting of A_6 and A_7. A_5's output periodically resets A_7's output ramp (F). A_6's output pulse (G) results from the comparison of A_5's and A_3's outputs and serves as the drive pulse for the heater control switch (Q_2). Thus, heater ON time is directly proportional to the thermistor bridge's temperature-induced unbalance.



TRACE	VERTICAL	HORIZONTAL
A	100V/DIV	200 μSEC/DIV
B	100V/DIV	200 μSEC/DIV
C	5V/DIV	200 μSEC/DIV
D	10V/DIV	200 μSEC/DIV
E	5V/DIV	1 mSEC/DIV
F	10V/DIV	1 mSEC/DIV
G	50V/DIV	1 mSEC/DIV

Fig 11—Driving a thermistor bridge *with complementary high-voltage pulses (A and B) permits high-gain amplification without drift problems (C). Driven by a delayed Sample command (D), a S/H amplifier converts the bridge's error signal to a dc level (E) that controls a pulse-width-modulated heater driver (F and G).*

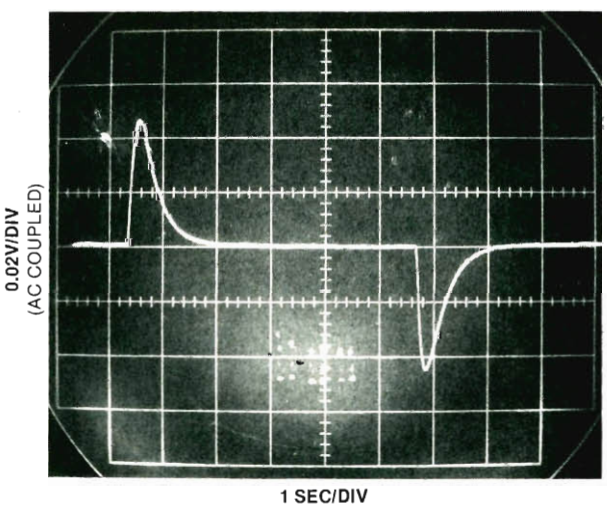


Fig 12—Tight heater-to-thermistor coupling *and careful calibration can provide rapid temperature restabilization. Here the controlled oven recovers within 2 sec after ±0.002°C steps.*

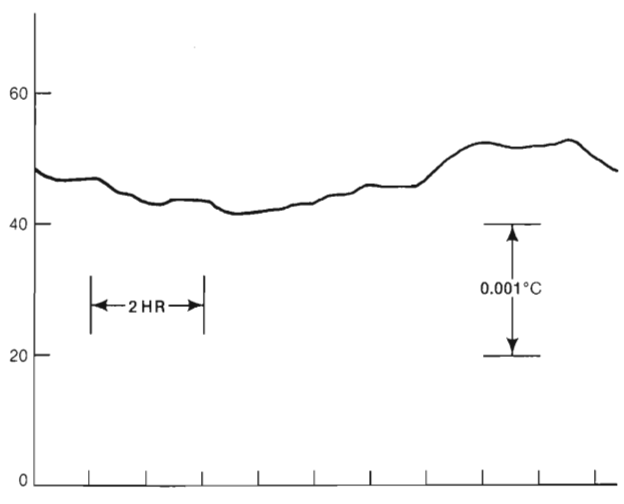


Fig 13—The long-term stability *possible with* ***Fig 10****'s circuit is demonstrated by this recording of the oven's temperature. Set at 50°C, the internal temperature stays within 0.001°C even though the exterior temperature varies by 6°C.*

Oven temperature stabilizes within 2 sec

Heater-to-thermistor thermal feedback completes the servo loop.

To adjust the loop's performance characteristics, apply small step changes in the temperature setpoint by switching a 100Ω resistor in series with one of the bridge's resistors. (For the thermistor shown in **Fig 10,** this modification produces a 0.02°C change.) While monitoring the loop's response at A_3's output, adjust the Gain and Time Constant potentiometers for minimum settling time.

Fig 12 shows how the system stabilizes within 2 sec for both positive and negative steps. And **Fig 13** demonstrates the design's very tight temperature-control capability. Set at 50°C, the oven's interior temperature varies by less than 0.001°C even when the ambient temperature changes by 6°C. Although **Fig 13** shows only a a few hours of operation, the circuit continued this performance over a 48-hr test period. **EDN**

Author's biography

Jim Williams, design engineer with National Semiconductor Corp's Linear Applications Group, Santa Clara, CA, has made a specialty of analog-circuit design and instrumentation development. Before joining National, he was a consultant with Arthur D Little Inc in analog systems and circuits. From 1968 to 1977, Jim directed the Instrumentation Development Lab at the Massachusetts Institute of Technology, where in addition to designing experimental biomedical instruments, he was active in course development and teaching. A former student of psychology at Wayne State University, he lists tennis, art and collecting antique scientific instruments as his leisure interests.

Article Interest Quotient (Circle One)
High **476** ***Medium*** **477** ***Low*** **478**

Signals & Noise

Almost the same, but...

Dear Editor:

The two circuits described in **Figs 12** and **13** in Jim Williams's article on quad op amps (EDN, January 7, pg 159) were indeed practical—I've recently been using similar designs.

My approach, however, substitutes 791-type power op amps for the LF347s. This process enables me to eliminate the power-splitting resistors and substitute instead the 791's internal current-sensing resistors.

Sincerely yours,
Art Delagrange
Naval Surface Weapons Center
Dahlgren, VA

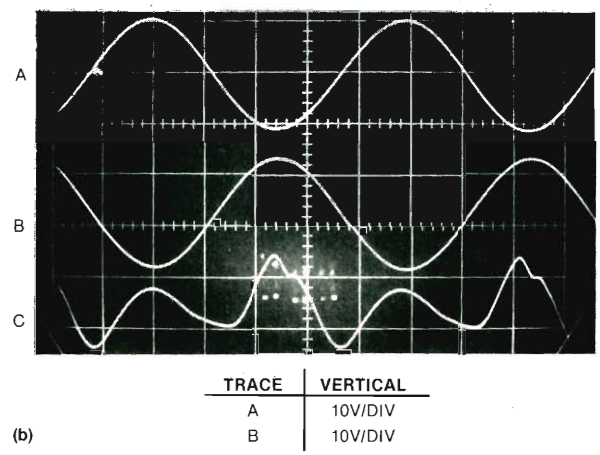
High-powered booster circuits enhance op-amp output

Although modern IC op amps simplify linear-circuit design, their output power is limited. Well-designed booster stages can solve this problem without sacrificing amplifier performance.

Jim Williams, National Semiconductor Corp

You can use the circuits presented here to substantially increase an IC amplifier's voltage and/or current output drive. Although the circuits were developed to solve specific problems, they are general enough to satisfy a variety of applications.

A booster is a gain stage with its own inherent ac characteristics. Therefore, in applying these circuits, you can't ignore such parameters as phase shift, oscillation and frequency response if you want the booster and amplifier to work well together. Designing booster stages that maintain good dynamic performance is a difficult challenge, especially because the booster circuitry changes with the application.



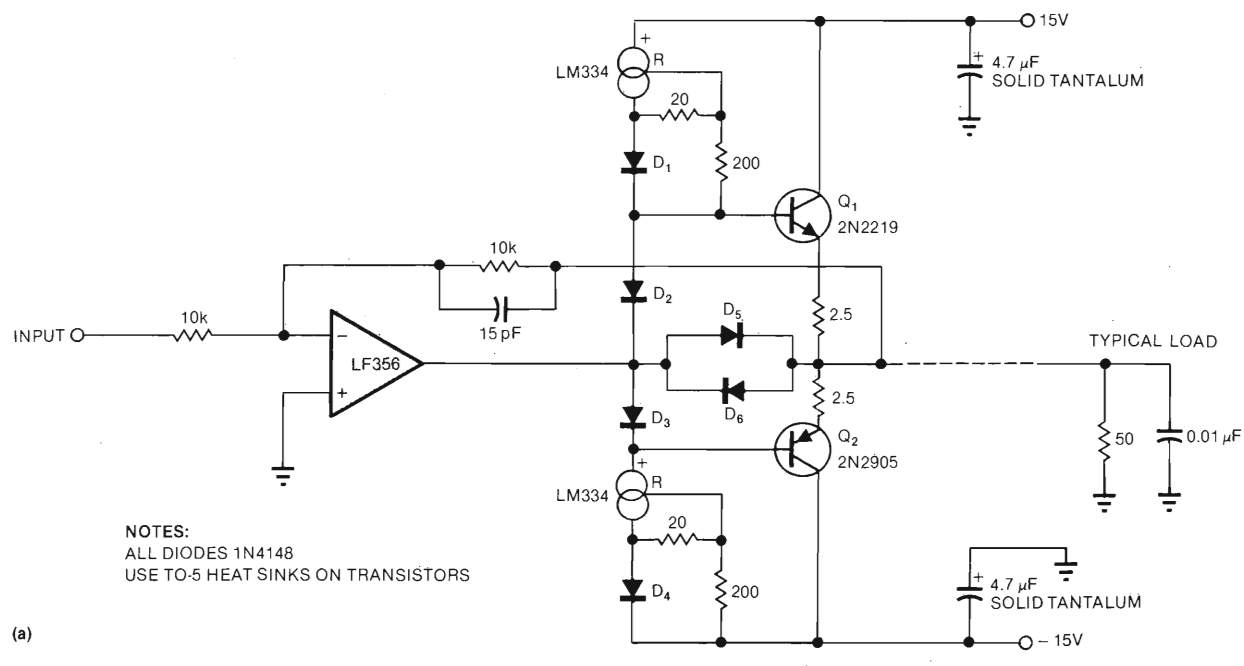


Fig 1—Complete with short-circuit protection *and fully temperature compensated, a booster circuit* ***(a)*** *develops a ±200-mA output current. Even with a heavy load (50Ω in parallel with 10,000 pF), response is quick and clean* ***(b);*** *overall circuit distortion measures less than 0.05% (trace C).*

Feedforward design technique increases current-booster speed

Start with some current-gain stages

The circuit shown in **Fig 1a** boosts the output-current level of an LF356 (a unity-gain inverting amplifier) to ±200 mA while maintaining a full ±12V output swing. In it, LM334 current sources, set for a 3.5-mA output by the 20Ω resistors, bias the complementary emitter followers, which provide drive and sink functions for the LF356 output. The RC feedback network creates a gain roll-off above 2 MHz.

The circuit's diodes satisfy several needs. D_1 and D_4, along with their associated 200Ω resistors, temperature-compensate the current sources. D_2 and D_3 eliminate crossover distortion in the output stage, while D_5 and D_6 provide short-circuit protection by shunting the drive to Q_1 and Q_2 when the output current exceeds 275 mA. For best results, thermally couple D_2 and D_3 to the transistors' heat sinks.

Circuit response (**Fig 1b**) is quick and clean. When you drive a 20V p-p sine wave into a heavy load (50Ω in parallel with 0.01 μF), output distortion measures less than 0.05%.

The circuit depicted in **Fig 2** accommodates higher current applications; it drives 3A (±25V pk) into an 8Ω load. As in **Fig 1a**'s design, the booster network—LM391-80 driver and associated power transistors—lies within the op amp's feedback loop. Booster-network bandwidth, set by the 5-pF capacitor at pin 3 of the LM391-80, is greater than 250 kHz.

Feedback resistors set the loop gain at 10, with the 100-pF capacitor introducing a roll-off at 100 kHz to ensure stability for the amplifier/booster combination. The output RC network, along with the 4-μH inductor, prevents circuit oscillations. You set the output-stage quiescent current at 25 mA by monitoring the voltage drop across the 0.22Ω resistors while adjusting the 10-kΩ pot at pins 6 and 7 of the 391.

How to increase speed

These first two circuit designs stress stability at the expense of speed. For example, **Fig 1a**'s booster network has a much wider bandwidth than the LF356 op amp. Unfortunately, the network's presence within the amplifier's feedback loop means that the LF356 dictates overall circuit response time.

However, there are ways to accentuate speed. In **Fig 3a,** for example, a feedforward network lets ac signals bypass the LM308 op amp and directly drive a very-high-bandwidth 200-mA current-boost stage. And because the LM308 provides the signal path for dc and low frequencies, the circuit achieves fast response with no sacrifice in overall dc stability.

Current sources Q_1 and Q_2 bias the complementary emitter followers (Q_3/Q_6 and Q_4/Q_7). Because this output stage introduces signal inversion, circuit output feeds back to the LM308's noninverting input. The 10-kΩ/15-

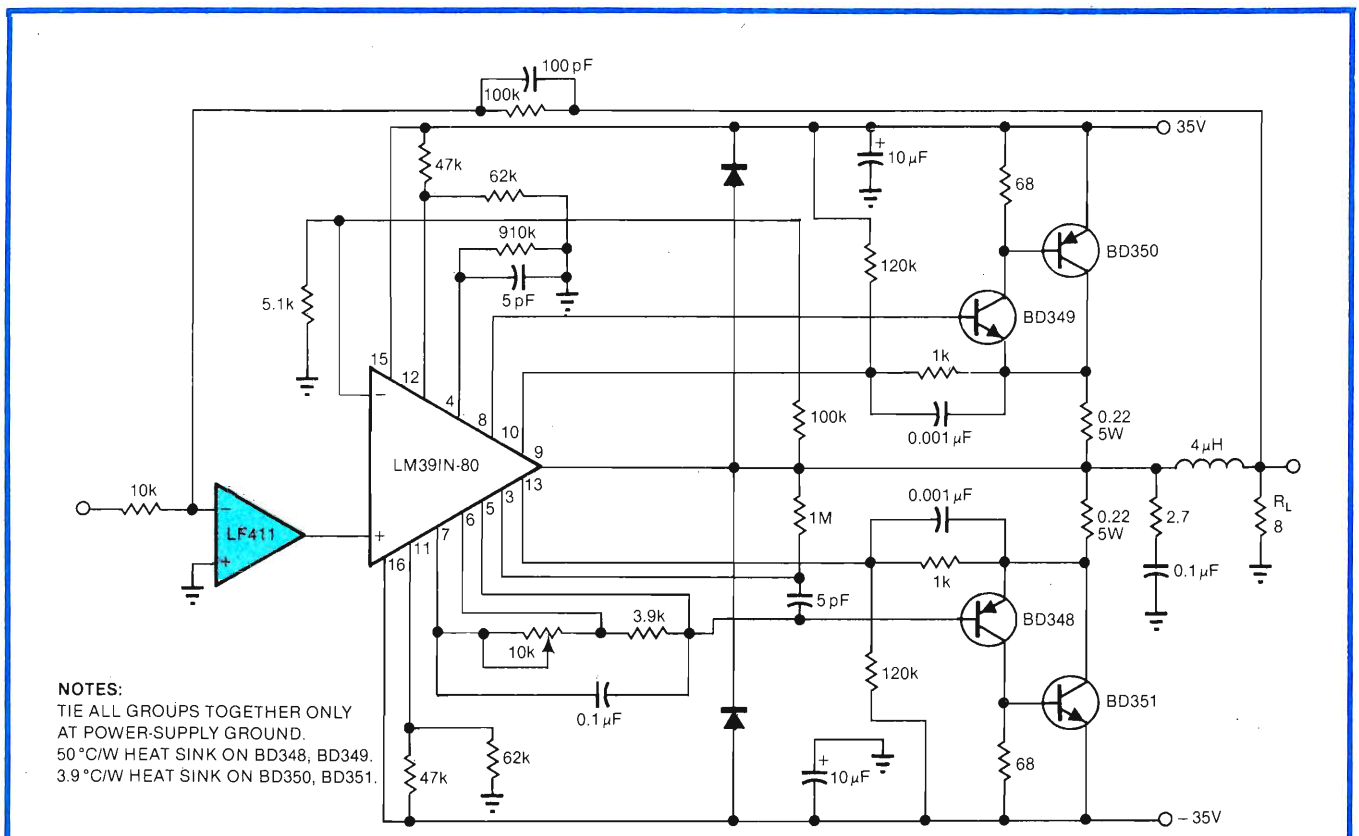
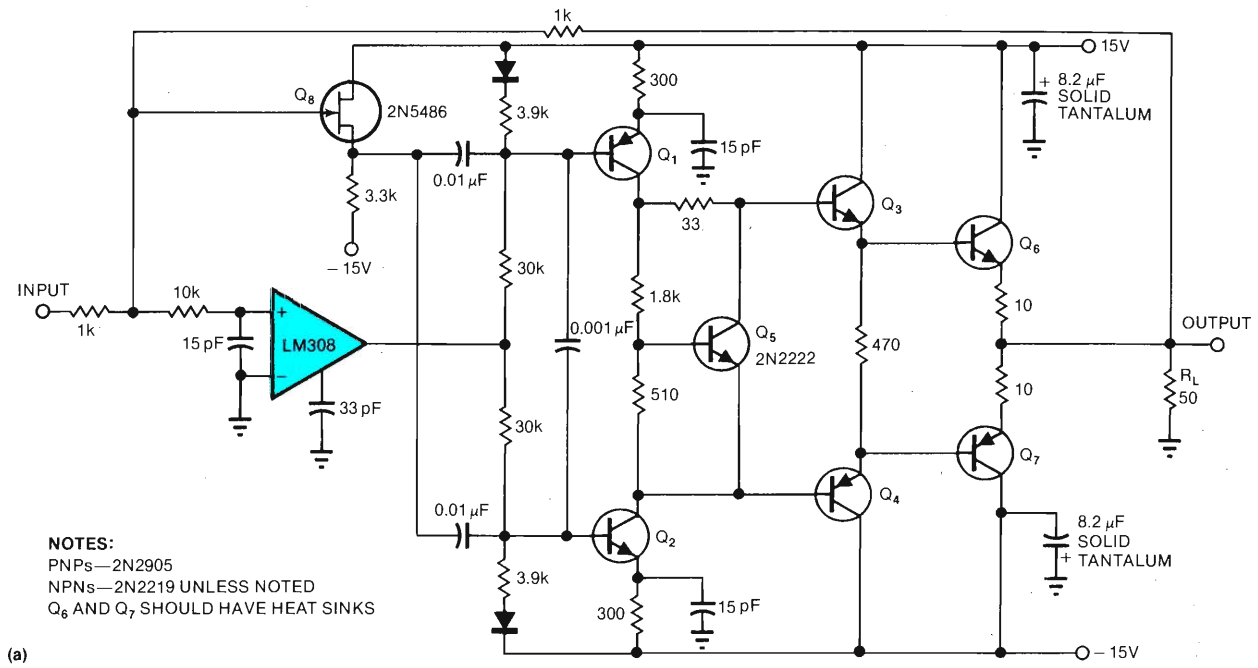
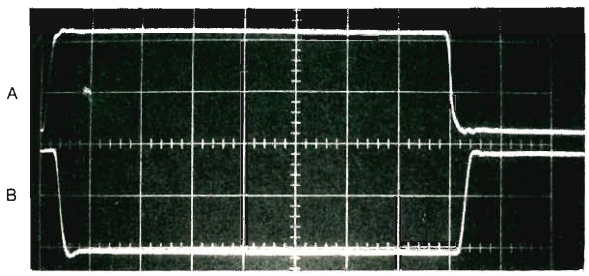


Fig 2—Designed to satisfy high-current needs, *this booster network drives 3A into an 8Ω load. The output RCL network prevents circuit oscillations, and the 10-kΩ pot sets output-stage quiescent current.*

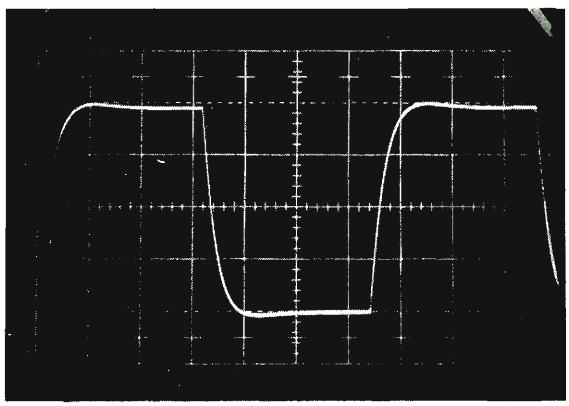


(a)



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	100 nSEC/DIV
B	5V/DIV	100 nSEC/DIV

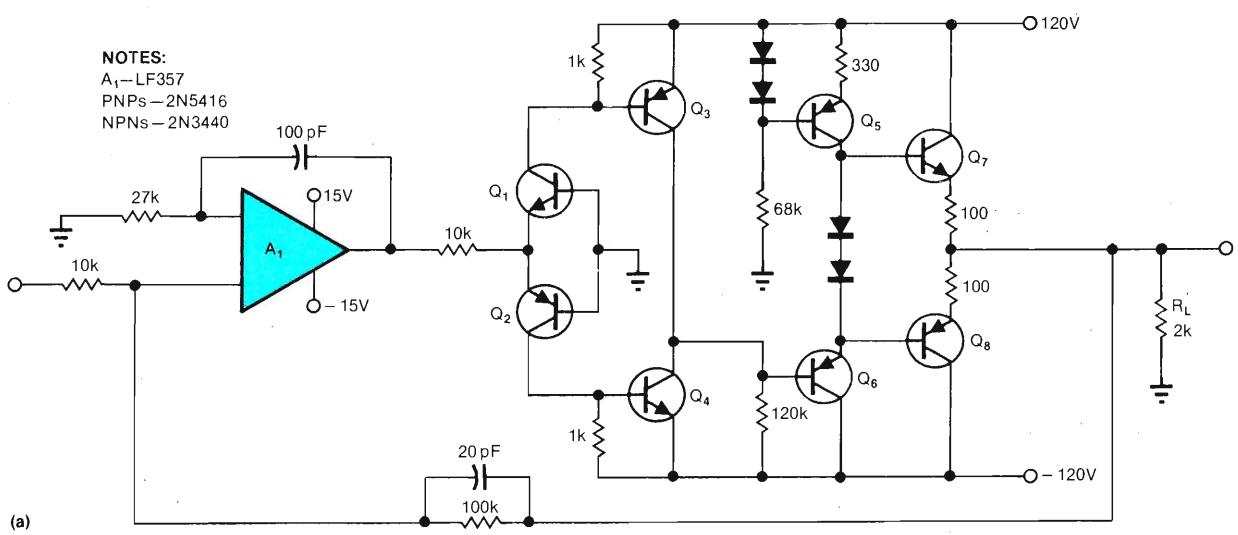
(b)



VERTICAL	HORIZONTAL
50V/DIV	5 μSEC/DIV

(b)

Fig 3—To increase speed, *a booster circuit* ***(a)*** *employs a feedforward network that allows ac signals to bypass the op amp and directly drive the high-bandwidth current-boost stage. Driving a 10V pulse into 50Ω, the booster evidences clean settling characteristics* ***(b);*** *rise and fall times measure less than 15 nsec.*



(a)

Fig 4—If you need extra voltage, *a booster design* ***(a)*** *develops ±100V across a 2-kΩ load. And it readily accommodates 30-kHz signals* ***(b).***

Stacking amplifier outputs effectively doubles voltage swing

pF RC network at the op amp's input shunts the 308's high-frequency inputs. These inputs go directly to the output stage via source follower Q_8.

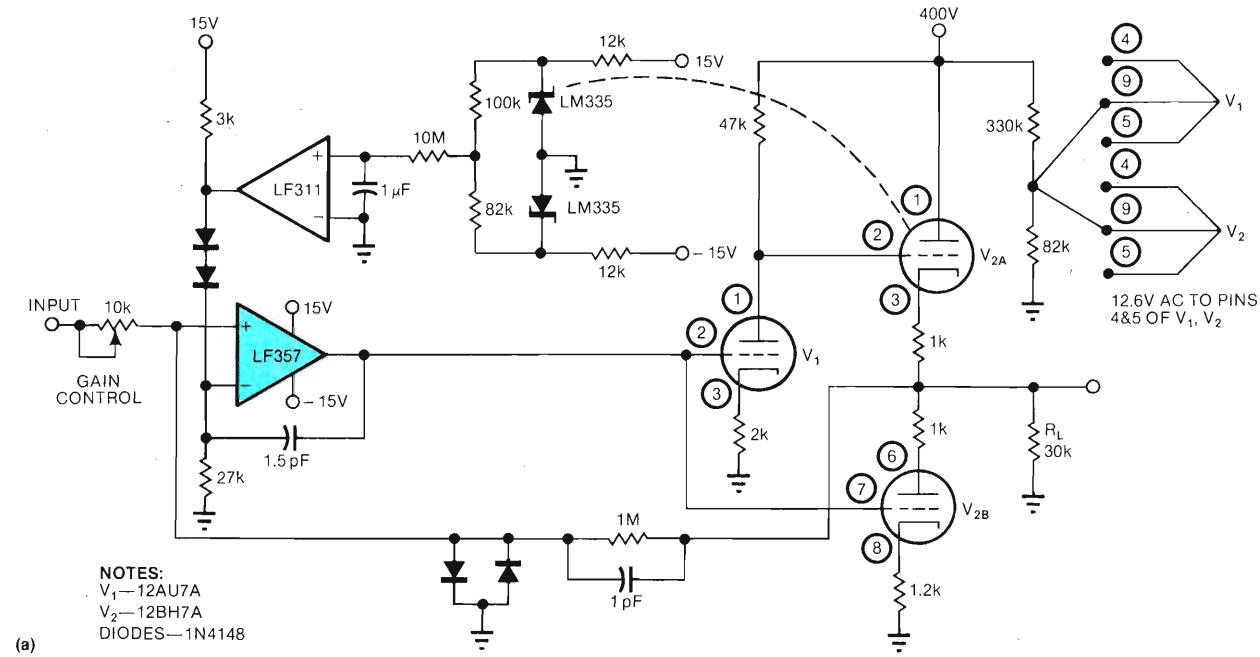
Despite the added complexity, performance is impressive (**Fig 3b**). The boosted amplifier features a 750V/μsec slew rate, full-power (±12V, 200 mA) bandwidth greater than 6 MHz and a 3-dB point beyond 11 MHz.

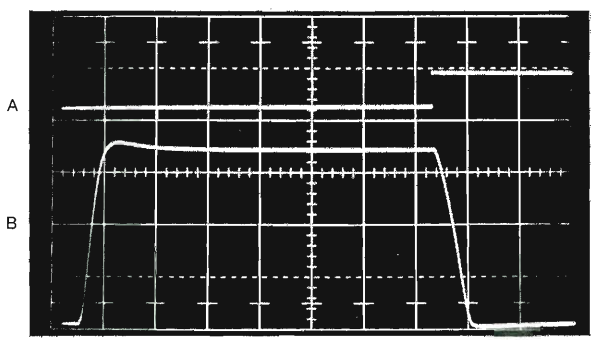
Voltage boosting presents no problems

Turn now to voltage-boosting designs. Thanks to the gain provided by the Q_1/Q_2 complementary common-base stage, the circuit shown in **Fig 4a** drives ±100V into a 2000Ω load. Q_3 and Q_4 furnish additional gain to the Q_7/Q_8 output stage, with Q_5/Q_6 providing the bias. The diodes attached to Q_5's collector minimize crossover distortion.

The circuit employs two feedback loops. Overall output-to-input feedback (returned to the LF357's noninverting input to allow for the Q_3/Q_4 inverting stage) sets A_1's gain at 10 to ensure specified output for ±10V input signals. And local ac feedback around A_1 adds dynamic stability.

With a ±50-mA output level, the circuit also provides some current gain. If your application doesn't require that capability, though, you can eliminate transistors Q_5 through Q_8 (along with their associated components) and close the feedback loop from the Q_3/Q_4 collector line. However, to prevent crossover distortion, make sure





TRACE	VERTICAL	HORIZONTAL
A	20V/DIV	2 μSEC/DIV
B	100V/DIV	2 μSEC/DIV

(b)

Fig 5—Virtually immune to load shorts and reverse voltages, *a positive-output-only booster* ***(a)*** *drives 350V into a 30-kΩ load. With a 15V input pulse, the output rises in 1 μsec and settles in less than 5 μsec* ***(b).*** *The falling edge slews just as rapidly and settles within 4 μsec.*

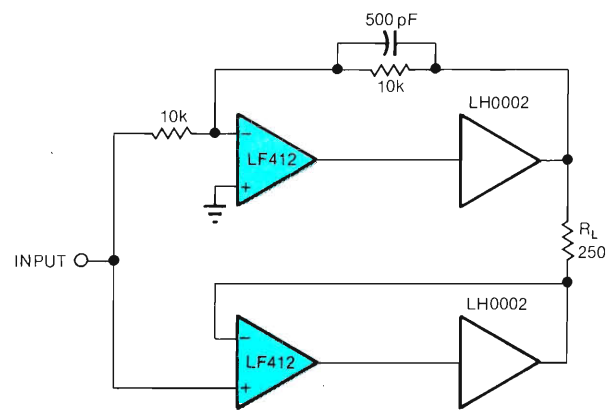


Fig 6—Effectively double the voltage swing *across a load by stacking or bridging amplifier outputs. Although this booster-circuit design is simple and requires no high-voltage supplies, you do have to float the load with respect to ground.*

that resistive output loading doesn't exceed 1 MΩ.

Fig 4b shows the boosted amplifier driving a ±100V square wave into a 200Ω load at 30 kHz. A second high-voltage booster circuit (**Fig 5a**) drives 350V into a 30-kΩ load and is virtually immune to load shorts and reverse voltages. And although the circuit has a 350V limit, tubes with higher plate-voltage ratings can extend the output capacity to several kilovolts.

In **Fig 5a,** the tubes are arranged in a common-cathode (V_{2B}), loaded-cathode-follower (V_{2A}) output configuration driven from a common-cathode (V_1) gain stage. Booster output feeds back to the LF357's noninverting input, with the 1-pF capacitor rolling off loop gain at 1 MHz. Local feedback stabilizes the LF357. The diodes at the summing junction protect the amplifier against high voltages during circuit start-up and slew-rate limiting. **Fig 5b** shows the booster's response at a gain of approximately 25.

In general, tubes are much more tolerant of load shorts and reverse voltages than transistors and are much easier to protect. In this circuit, one of the two LM335 temperature sensors is in contact with V_2, and its output gets compared with that of the second LM335, which monitors ambient temperature.

Under normal operating conditions, V_2 runs about 45°C above ambient temperature, generating a −100-mV signal at the LF311's noninverting input and forcing its output low. When a load fault occurs, V_2's plate dissipation increases causing its associated sensor's output to rise. This action in turn forces the LF311 output high, drives the LF357 output low and shuts down the output stage. V_2's thermal time constant, along with the 10-MΩ/1-μF delay network in the LF311's input line, provides adequate hysteresis.

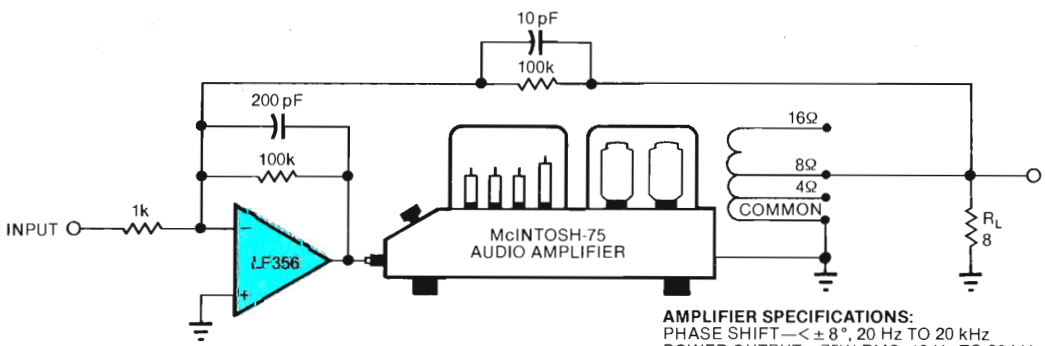


Fig 7—Voltage and current boosting are a snap *when you use a high-quality audio amplifier. For loads in the 4 to 16Ω range, this circuit produces 75W.*

BOOSTER-CIRCUIT PERFORMANCE

FIGURE	VOLTAGE GAIN	CURRENT GAIN	BANDWIDTH	COMMENTS
1	NO	YES (200-mA OUTPUT)	DEPENDS ON OP AMP: 1 MHz TYP.	FULL ± OUTPUT SWING. STABLE INTO 50Ω/10,000-pF LOAD. INVERTING AND NONINVERTING OPERATION. SIMPLE.
2	YES (± 30V OUTPUT)	YES (3A OUTPUT)	50 kHz	FULL ± OUTPUT SWING. ALLOWS INVERTING OR NONINVERTING OPERATION.
3	NO	YES (200-mA OUTPUT)	FULL OUTPUT TO 6 MHz, − 3-dB POINT AT 11 MHz.	ULTRAFAST, 750V/μSEC. FULL BIPOLAR OUTPUT. INVERTING OPERATION ONLY.
4	YES (100V OUTPUT)	YES (50-mA OUTPUT)	50 kHz	FULL ± OUTPUT SWING. ALLOWS INVERTING OR NONINVERTING OPERATION. CAN BE SIMPLIFIED TO DRIVE CRT DEFLECTION PLATE.
5	YES (350V OUTPUT)	NO	500 kHz	OUTPUT VERY RUGGED. GOOD SPEED. POSITIVE OUTPUTS ONLY.
6	YES (24V OUTPUT)	NO	DEPENDS ON OP AMP	REQUIRES THAT THE LOAD FLOAT ABOVE GROUND.
7	YES (70V OUTPUT)	YES (3A OUTPUT)	100 kHz	OUTPUT EXTREMELY RUGGED. WELL SUITED FOR DRIVING DIFFICULT LOADS IN LAB SETUPS. FULL BIPOLAR OUTPUT. AC ONLY.
8	YES (1000V OUTPUT)	YES (300-mA OUTPUT)	50 Hz	HIGH VOLTAGE AT HIGH CURRENT. SWITCHED-MODE OPERATION ALLOWS USE OF ± 15V SUPPLIES. GOOD EFFICIENCY. LIMITED BANDWIDTH WITH ASYMETRICAL SLEWING. POSITIVE OUTPUTS ONLY.

Designs boost current and voltage simultaneously

Multifunction boosting's also possible

Three additional circuit designs all provide combined current- and voltage-output boosting. **Fig 6,** for example, depicts a simple way to effectively double the voltage swing across a load by stacking or bridging amplifier outputs. Each LF412 output feeds an LH0002 amplifier to provide current-drive capability. Because only one of the LF412s inverts, though, the combination produces 24V across the 250Ω load (±12V swings from each leg).

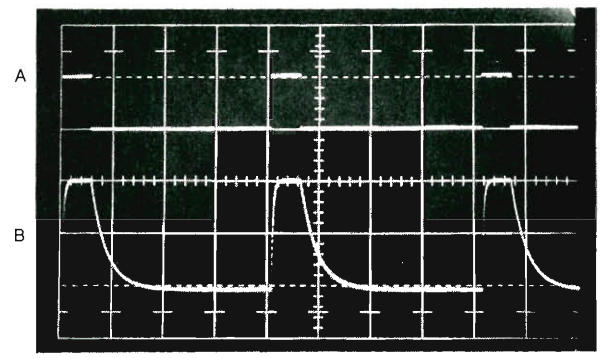
The circuit is simple and requires no high-voltage supplies. However, you must float the load with respect to ground.

Fig 7's circuit uses a high-quality audio amplifier as a current-voltage booster for ac signals. (The McIntosh-75, with its transformer-isolated output and clean response, is a venerable favorite in research labs.) The LF356 op amp's loop is closed locally at a dc gain of 100 and rolled off at 50 kHz by the 200-pF capacitor. Booster output from the audio amplifier feeds back via a 100-kΩ resistor to set overall ac gain at 100.

This design is an excellent choice for laboratory applications because the vacuum-tube-driven, transformer-isolated output is extremely forgiving and almost indestructible. You can use this booster to power ac variable-frequency supplies and shaker-table, motor and gyro drives, as well as other difficult-to-handle inductive and active loads. Power output into 4 to 16Ω loads equals 75W; you can drive 1Ω loads at reduced power output levels.

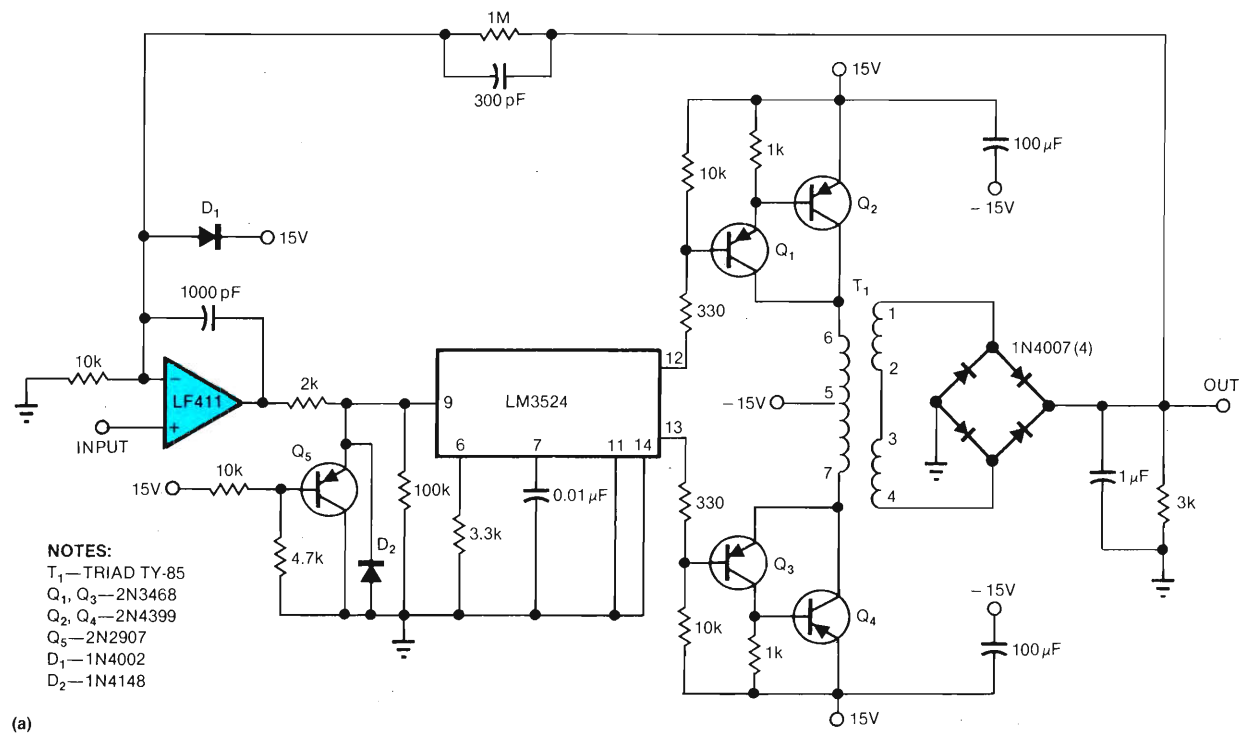
In **Fig 8a,** the LF411 op amp controls as much as 300W for positive outputs ranging to 1000V. The booster achieves this performance without sacrificing efficiency because it operates in switching mode. Additionally, it requires only ±15V supplies to develop its high-potential outputs.

An integral dc/dc converter directly generates the required high output voltage. The LM3524 regulator chip pulse-width-modulates transistors Q_1 through Q_4 to provide switched 20-kHz drive to the stepup transform-



(b)

TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	10 mSEC/DIV
B	500V/DIV	10 mSEC/DIV



(a)

Fig 8—Operating in switching mode, *a high-power booster design* ***(a)*** *features 300W (1000V/300 mA) output capability. Performance is impressive* ***(b):*** *Output rise time equals 1 msec, while fall time measures about 10 msec (due to capacitor discharge time). Slew-rate limiting comes into play during output-pulse rise time—toroid switching action is barely visible on the output pulse's leading edge.* ***(Caution: Output levels are lethal!)***

er. The transformer output, rectified and filtered, feeds back to the LF411, which controls the LM3524 input. Therefore, op-amp feedback action has the same stabilizing effect found in the previous circuit designs.

Two protection networks are provided. The Q_5/diode combination clamps the LF411 output to prevent LM3524 damage during circuit start-up. And the diode at the LF411's summing junction prevents high-voltage transients coupling through the feedback capacitor from destroying the amplifier.

For the component values shown, the circuit exhibits a full-power sine-wave output frequency of 55 Hz. Resistor feedback sets amplifier gain at 100, so a 10V input produces a 1000V output. Although the 20-kHz switching rate sets the upper limit on loop information-transmission speed, the 1-μF capacitor at the output restricts circuit bandwidth. **Fig 8b** shows the LF411's boosted response with a 10V pulse applied to the circuit input.

A word of caution: Approach the construction, testing and applicaton of this circuit *with extreme care.* The output potentials developed are far above lethal levels.

As a design aid, the **table** summarizes pertinent points discussed in this article. Using it can greatly simplify the task of matching a booster circuit to your application. EDN

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Author's biography

Jim Williams, manager of National Semiconductor Corp's Linear Applications Group (Santa Clara, CA), has made a specialty of analog-circuit design and instrumentation development. Before joining National, he was a consultant with Arthur D Little Inc in analog systems and circuits. From 1968 to 1977, Jim directed the Instrumentation Development Lab at the Massachusetts Institute of Technology, where in addition to designing experimental biomedical instruments, he was active in course development and teaching. A former student of psychology at Wayne State University, he lists tennis, art and collecting antique scientific instruments as his leisure interests.

Piezoceramics plus fiber optics boost isolation voltages

Overcoming traditional magnetic-transformer drawbacks, a novel isolation-amplifier design hikes voltage-breakdown limits more than tenfold by incorporating a piezoceramic-based acoustic transformer and a fiber-optic link.

Jim Williams, National Semiconductor Corp

When standard parametric or isolation amplifiers don't adequately isolate or protect your analog measurement systems, the circuit design described in this article can help. Although typical isolation amplifiers achieve about a 2.5-kV max isolation voltage, this one can handle 20- to 100-kV breakdown limits. It incorporates a piezoceramic material structured as an acoustic transformer and a fiber-optic lightpipe.

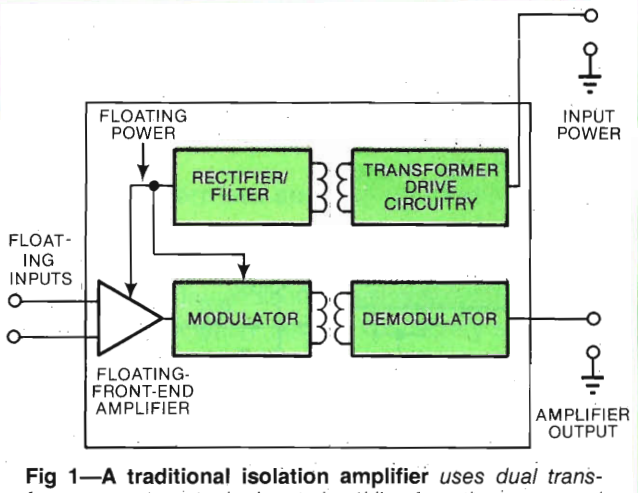


Fig 1—A traditional isolation amplifier *uses dual transformers to separate the input-signal line from the power and output-signal lines. This approach typically results in about a 2.5-kV max input-isolation voltage.*

Isolation amplifiers find use mainly in assuring safe and reliable analog measurements. They surmount the problems of high common-mode voltages in applications such as medical test instruments and completely isolate or interrupt ground loops or paths in equipment such as that used in industrial process-control systems.

Designing isolation amplifiers mandates careful attention to two key factors: isolating the power supply from the input-signal line and galvanically separating the input- and output-signal lines. The first half of the task generally involves the most effort.

Input isolation proves complex

Conventional isolation amplifiers employ a magnetic transformer to convey power to the circuit's floating front end (**Fig 1**). Although this transformer galvanically separates the power supply from the input terminals, it increases in size and cost when common-mode voltages exceed about 2.5 kV. Moreover, its leakage currents can total as much as 2 μA.

To separate the input- and output-signal lines, conventional isolation amplifiers modulate the floating front end's output onto a carrier signal. This signal traditionally passes via another magnetic transformer to the circuit's output terminals. Modulation schemes include pulse width, pulse amplitude and voltage to frequency. Here again, though, magnetic transformers become bulky and inefficient as common-mode voltages and leakage currents rise. And isolation limits depend

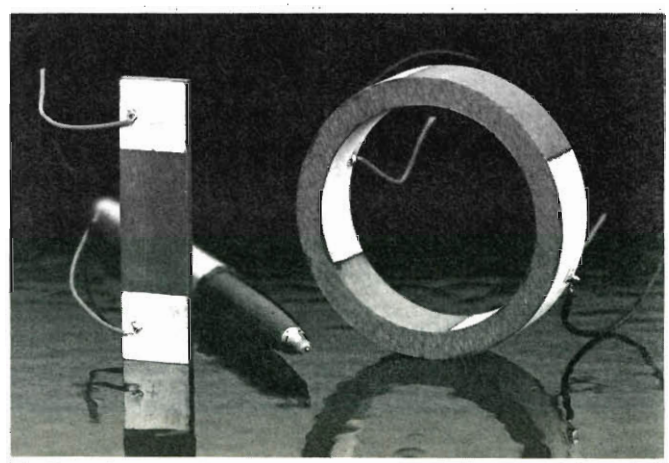


Fig 2—Able to perform as acoustic transformers, *piezoceramic materials come in various sizes and shapes, such as this thin bar and thick toroid (shown with a ballpoint pen for dimensional reference). Observe that two pairs of leads make input and output connections to each piece of piezoceramic material.*

Traditional isolation amplifiers employ magnetic transformers

on the transformer's breakdown rating.

Even when an optoisolator replaces the modulation transformer with a frequency- or light-intensity-coding approach, power requirements for operating the floating front end still require the power transformer. What's more, optoisolators arc under excessive common-mode voltages.

Other methods for transmitting electrical energy with high isolation exist, such as using microwave devices and solar cells, but they prove expensive, inefficient and impractical. Batteries are an alternative power source, but they have maintenance and reliabiliy limitations.

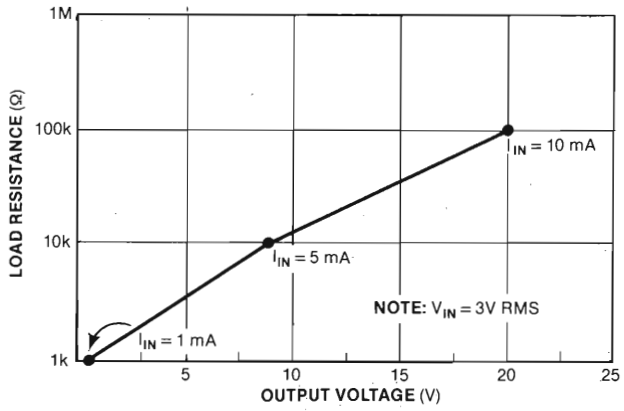
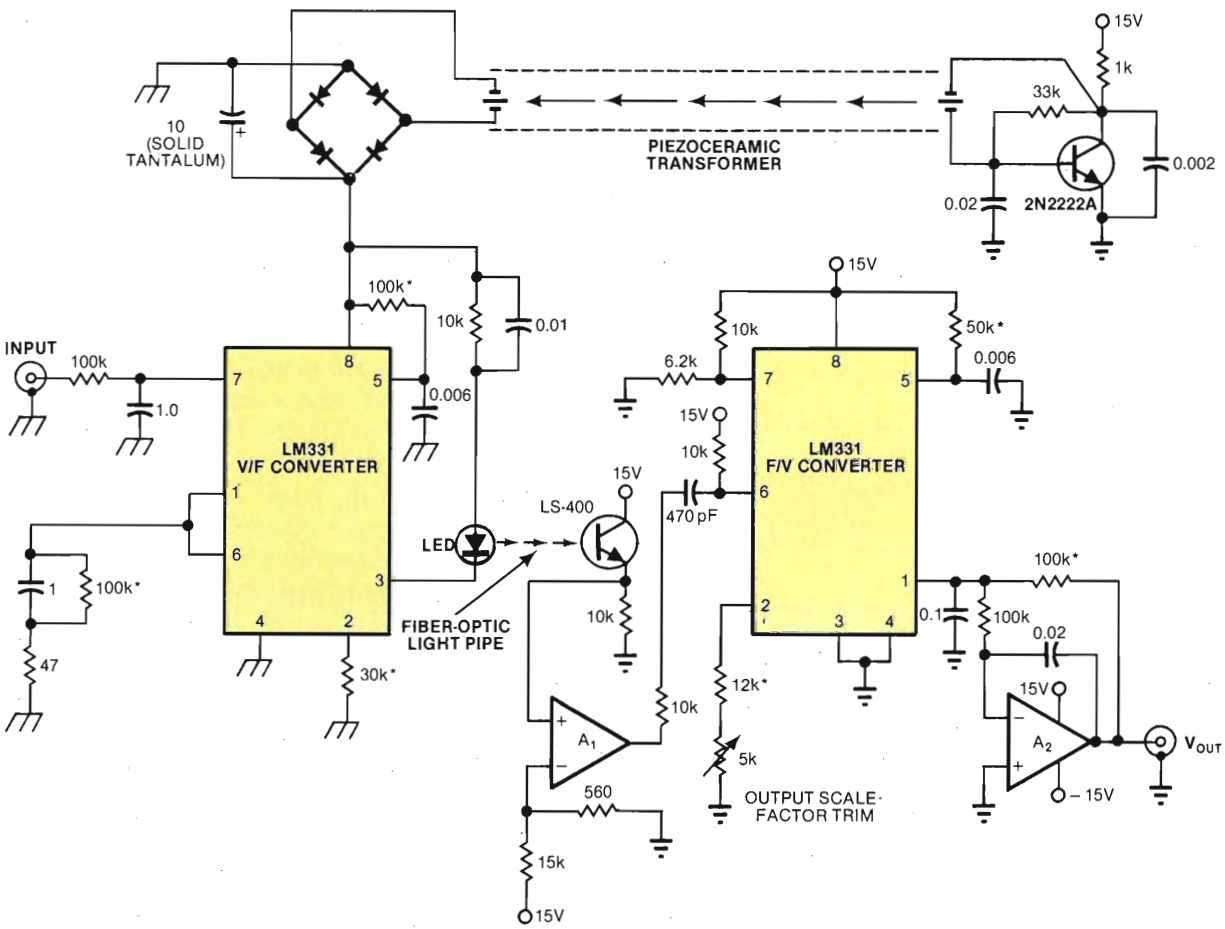


Fig 3—This typical load line *traces an acoustic transformer's performance at resonance. Note that for a constant 3V rms drive voltage and a varying 1- to 100-kΩ load resistance, the acoustic transformer draws up to 10 mA as its output voltage increases to 20V.*



NOTES:
A_1, A_2 = LF353 DUAL
ALL DIODES = 1N4148
* = 1% METAL-FILM RESISTOR
= FLOATING COMMON
= AMPLIFIER GROUND
CAPACITORS IN μF UNLESS NOTED

Fig 4—An innovative isolation-amplifier design *employs piezoceramic material as an acoustic transformer and a fiber-optic lightpipe to separate the input-signal line from the power and output-signal lines, respectively. In this approach, breakdown-voltage limits escalate to 20 to 100 kV.*

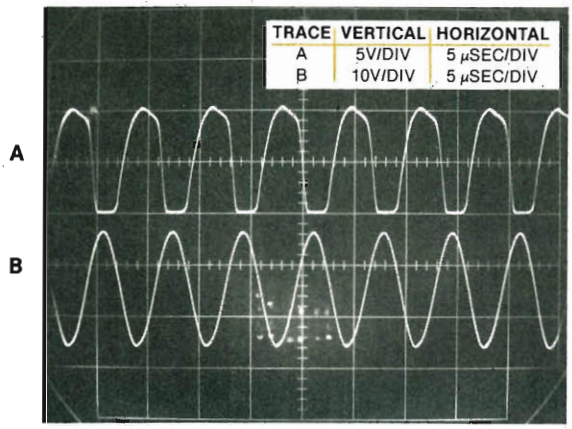


Fig 5—The 2N2222A transistor's output *(from **Fig 4**'s circuit) shows an irregularly shaped sine wave (trace **A**) delivered to the acoustic transformer's input. The transformer's high-Q properties cause it to filter and amplify the waveform into a smooth sinusoid **(B)** at its output.*

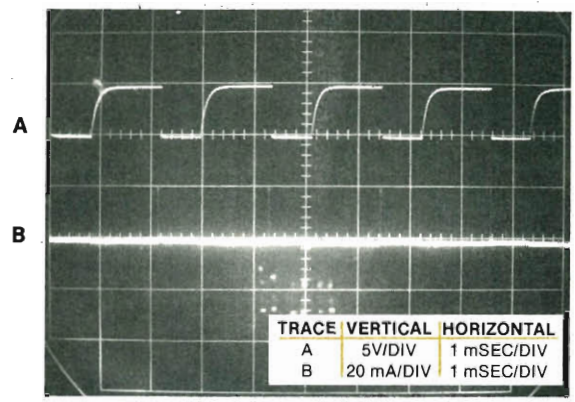


Fig 6—Trace A depicts the LM331 voltage-to-frequency converter's output *(from **Fig 4**'s circuit). This output drives the LED that couples to the fiber-optic lightpipe. Trace **B** indicates the LED's current waveform. Whenever the converter's output is LOW, the LED saves power by passing an extremely narrow (20 mA) light-encoded pulse.*

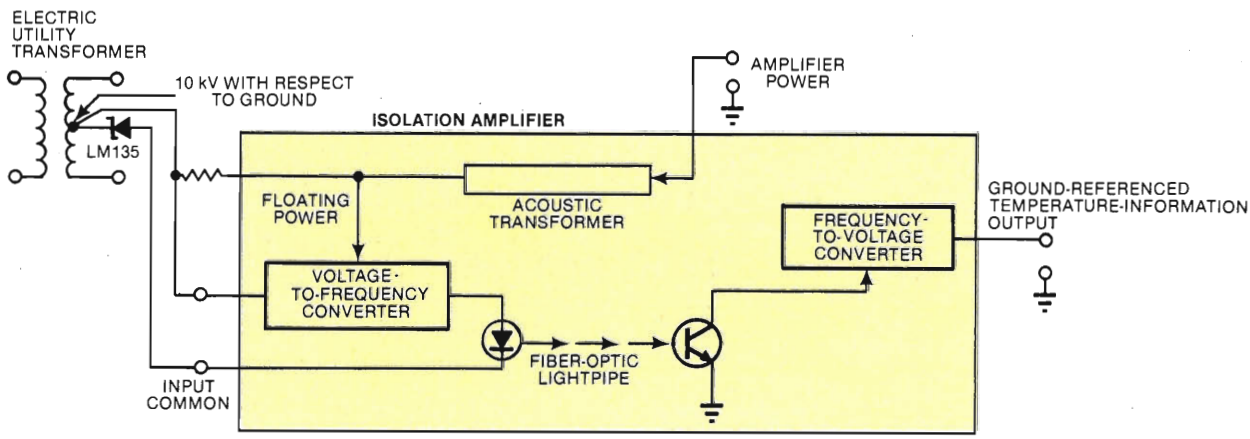


Fig 7—To monitor an electric-utility transformer's winding temperature, *this acoustic-transformer-based isolation amplifier permits the LM135 temperature sensor—which floats at 10 kV—to generate a safe ground-referenced output.*

Acoustic transformers surpass magnetic types

To achieve very high common-mode voltage but extremely low leakage current, the ideal electrical energy transfer device should permit easy implementation, operate efficiently and inexpensively and provide virtually complete isolation.

An acoustic transformer meets these goals by taking advantage of certain ceramic materials' piezoelectric characteristics. Although piezoelectric materials have long been recognized as electric-to-acoustic and acoustic-to-electric transducers (eg, microphones and buzzers), their use for electric-to-acoustic-to-electric energy conversion has not been emphasized. This conversion sequence capitalizes on ceramic materials' unique conductive nature; they furnish excellent electrical-insulation and acoustic-conduction properties.

In an acoustic transformer, acoustic waves and nonconducting piezoceramics serve in place of a conventional transformer's magnetic flux and conductive core. **Fig 2** shows two acoustic-transformer types; you make either type by merely bonding a pair of leads to each end of the piezoceramic material.

Tests reveal that this material's electrical resistance exceeds $10^{12}\Omega$; primary-to-secondary capacitance typically measures a few picofarads. The material's physical properties and configuration determine its resonant frequency as a transformer.

In operation, an acoustic transformer employs an oscillator-driven piezoelectric resonator at one end of the ceramic material. The resonator sends acoustical energy along the material at about 150 kHz. At the other end, an identical resonator receives the acoustical energy and converts it back to electrical energy. After rectification and filtering, the electrical energy powers the isolation amplifier's front end.

With this approach, isolation amplifiers can achieve breakdown limits greater than 20 kV, using piezoceramic material 0.25 to 12 in. long. In fact, meticulous designs have achieved isolation voltages as high as 100 kV.

As an additional advantage, acoustic transformers cost less than their magnetic counterparts. Further, they possess higher operating efficiency because the piezoceramic material is tuned to its natural resonance

An acoustic transformer isolates the power supply from the input

point.

Fig 3 depicts a typical acoustic transformer's output characteristics when driven at resonance. Note that the transformer's power-transfer efficiency can exceed 75%, depending on load conditions. Short-circuit output current for this device equals 35 mA.

Fiber optics upgrades input/output isolation

The other key design factor in designing isolation amplifiers—nearly total input-to-output line separation—is accomplished via fiber optics by stretching both lines further apart than an optoisolator can. This optical-encoding method works as it would in a typical optoisolator, but with an increased distance between transmitter and receiver yielding higher isolation voltages.

In practice, a light-emitting diode (LED) transmits optically encoded signals through a single-fiber cable to a photodiode receiver. The exact cable length depends on the particular circuit requirements.

Put it all together

Combining an acoustic transformer and a fiber-optic link in an isolation amplifier (**Fig 4**) extends conventional breakdown limits by more than a factor of 10. In this circuit, the acoustic transformer's high-Q characteristics allow self resonance in a manner similar to that of a quartz crystal. Resonance eliminates the need for a stable oscillator to drive the acoustic transformer.

To start operation, the 2N2222A transistor excites the piezoceramic transformer's primary (**Fig 5**). At the secondary, four diodes and a capacitor rectify and filter the transformer's electrical output. This output in turn energizes the LM331 V/F converter.

The converter transforms its amplitude-based input signal into a frequency-based output. This signal then drives an LED, whose output travels along a fiber-optic cable.

Each time the V/F converter's output goes LOW, a narrow (20-mA) spike passes through the LED via the 0.01-μF capacitor (**Fig 6**). This short duty cycle keeps the average current value small, minimizing power requirements.

At the receiver end, a photodiode detects the light-encoded signals. It in turn passes the signals to the LM331 for demodulation.

Amplifier accommodates varied uses

An acoustic-transformer/fiber-optic isolation amplifier finds use in diverse applications. In one example, an LM135 transducer tracks the winding temperature of an electric-utility transformer operating at 10 kV (**Fig 7**). The transducer's output biases the isolation amplifier's input. Temperature information at the amplifier's output is thus safely referenced to ground.

In another ground-referenced application, the isolation amplifier's high-common-mode voltage blocking

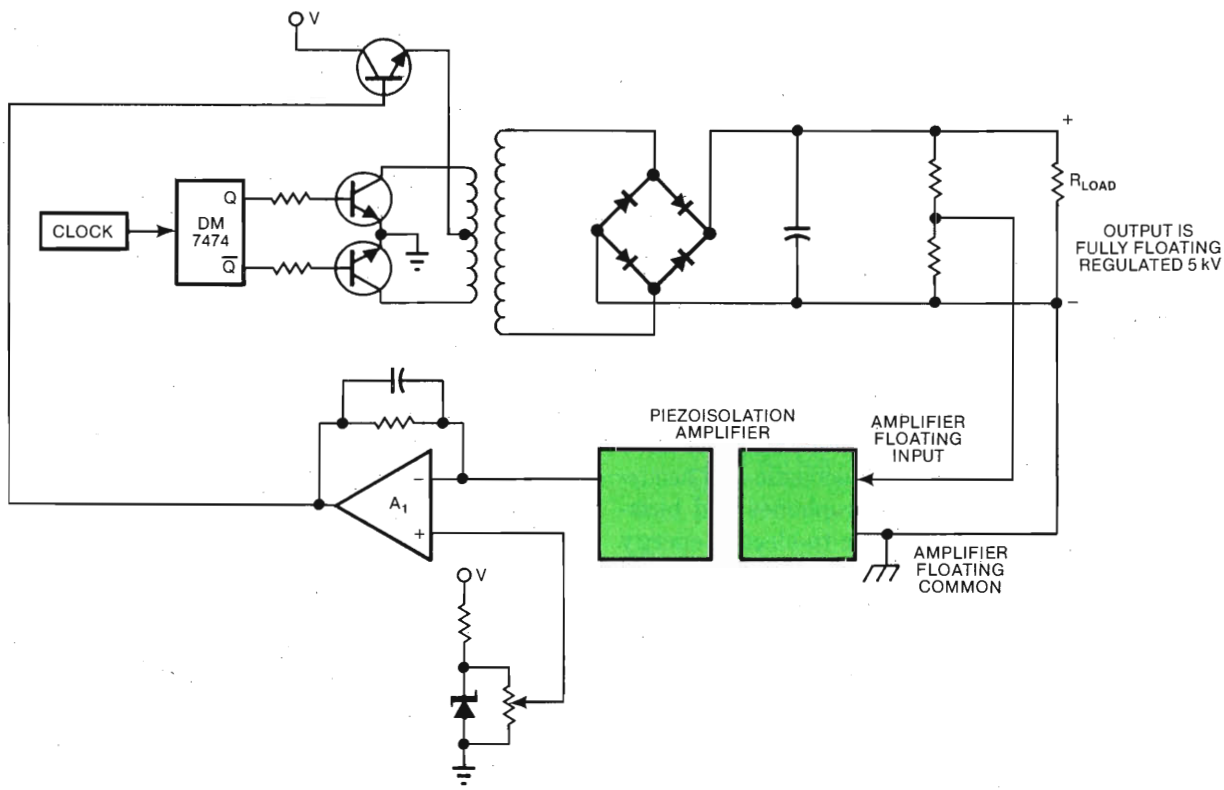


Fig 8—The piezoisolation amplifier *in this application provides a ground-referenced feedback path for the 5-kV regulated power supply. The power supply's output thus fully floats.*

A fiber-optic link galvanically separates output and input lines

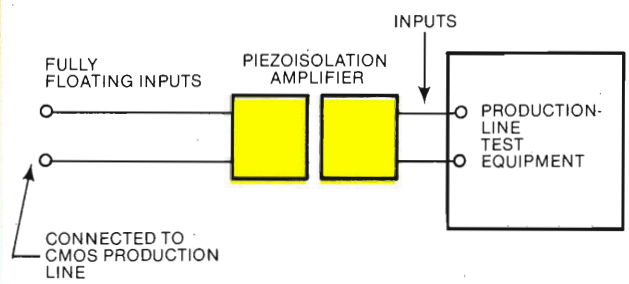


Fig 9—Production-line test equipment *for checking CMOS products is fail-safe isolated via a piezoisolation amplifier. This amplifier keeps static discharge away from the sensitive CMOS parts even when the test equipment develops a substantial charge.*

allows a 5-kV regulated power supply's output to fully float (**Fig 8**). Here, a push/pull dc/dc converter generates the high-voltage output. The isolation amplifier provides a ground-referenced output-feedback signal to op amp A_1, which controls the transformer's drive, completing the feedback loop.

For a fail-safe test application, an acoustic/fiber-optic amplifier isolates instrument inputs connected to CMOS ICs on a production line (**Fig 9**). This arrangement prevents static-discharge damage, even when the instruments have accumulated a substantial charge. EDN

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Piezoceramic Catalog 761-01, Channel Industries Inc, Santa Barbara, CA, 1980.

Author's biography

Jim Williams, applications manager with National Semiconductor's Linear Applications Group (Santa Clara, CA), specializes in analog-circuit design and instrumentation development. Before joining the firm, he served as a consultant at Arthur D Little Inc and directed the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art and collecting antique scientific instruments in his spare time.

Employ pulse-width modulators in a wide range of controllers

Generally considered a power-supply controller, the pulse-width modulator suits many other applications such as lamp-intensity control and motor-speed regulation.

Jim Williams, National Semiconductor Corp

By applying the pulse-width-modulator (PWM) capabilities that serve so well in high-efficiency power supplies, you can control many diverse functions. PWM ICs such as the LM3524 contain several operational blocks (see **box,** "A pulser plus"), giving them the versatility to simplify control tasks.

Level a lamp's luminosity

As a first example, consider what happens when evaluating optoelectronic sensors or trying to accurately duplicate a 35-mm color slide. The light source used must maintain constant intensity. **Fig** 1 demonstrates how you can combine a PWM with a photodiode/amplifier stage to servo-level a lamp's output intensity and thereby meet this need.

In this design, the LF356 op amp functions as a current-to-voltage converter. Thus, as the lamp's output increases, the resulting higher radiant energy causes the photodiode to draw more current out of the op amp's summing junction. The amp responds by generating a positive-going output voltage that feeds back into the input and re-establishes the summing junction's requisite zero balance.

The op amp's output voltage—a function of the photodiode's light-induced current flow—also feeds the PWM's on-chip error amplifier. This amplifier compares the unknown voltage at pin 1 with the intensity-control value set by the 2.5-kΩ potentiometer. (Note that the reference voltage for the intensity setting comes from the PWM's on-chip 5V supply.) This error voltage, amplified by approximately 70 dB as determined by the 1-MΩ resistor loading pin 9, controls the PWM's ON time.

In addition to the 1-MΩ resistor, a 0.001-μF capacitor loads pin 9. This RC combination provides the feedback loop with the proper frequency compensation

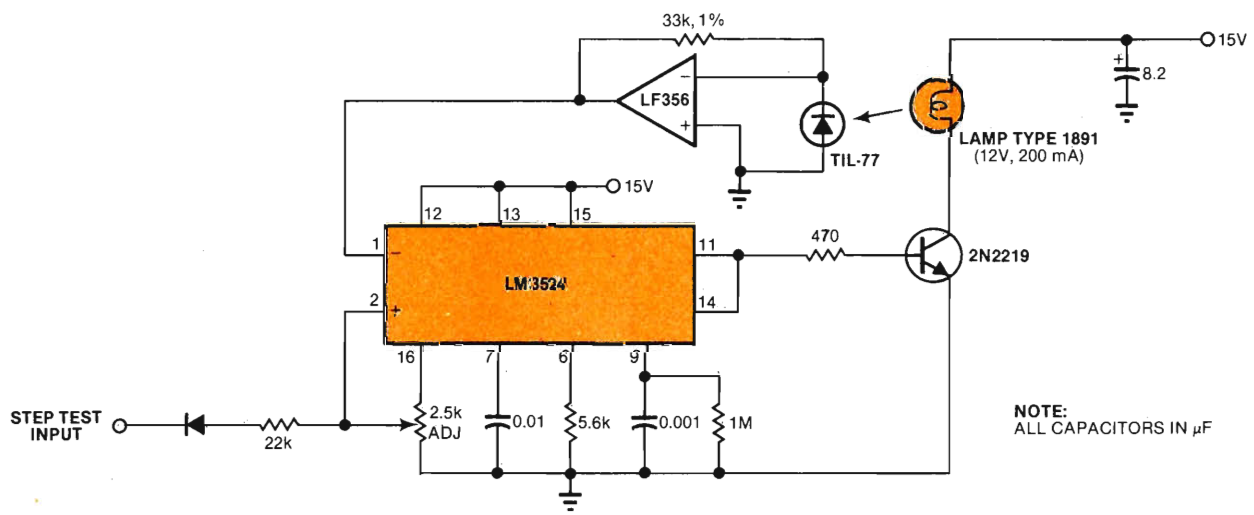


Fig 1—A lamp's intensity remains constant *when you drive the lamp with a pulse-width modulator (PWM) in an optical closed-loop feedback scheme. Here the PWM's ON time is controlled by comparing a photodiode's output with a preset intensity reference level.*

Pulse-width-modulate a lamp to keep its brightness constant

by rolling off with a 1-msec time constant. Similarly, the 5.6-kΩ/0.01-μF combination connected to pins 6 and 7 sets the PWM's oscillator frequency to about 30 kHz.

The lamp is driven by a combination of the IC's on-chip transistors and a discrete 2N2219. **Fig 2a** shows the design's servo action; note that when the 2N2219's collector pulses ON (upper trace), the LM356's output ramps up rapidly (lower trace). But when the drive ramps up rapidly (lower trace). But when the drive-transistor turns off, the resultant negative-going signal ramps much slower because the lamp accepts energy more readily than it gives energy up.

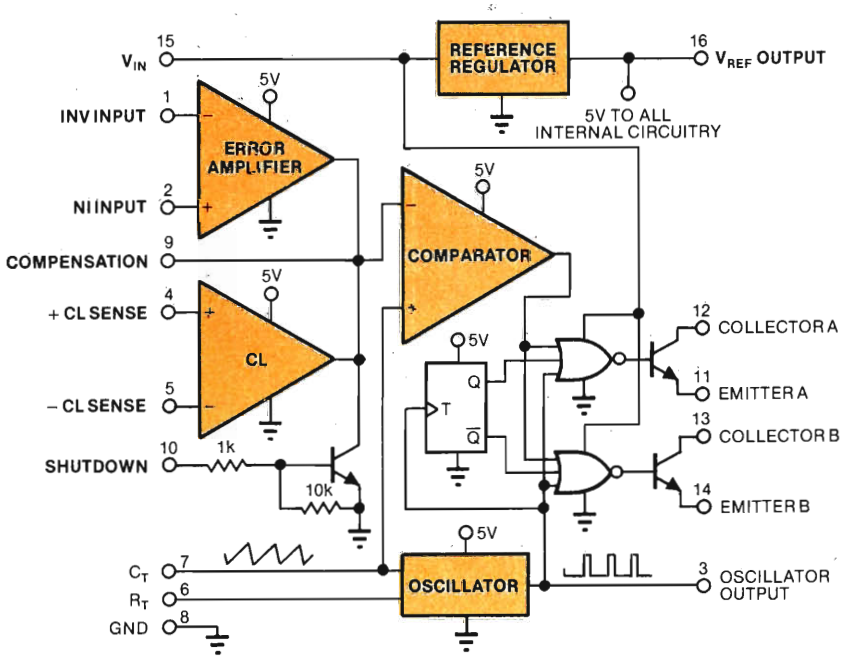
Figs 2b and **c** better illustrate the lamp's action. Here the servo loop is artificially upset by introducing an external pulse via **Fig 1**'s circuit's Step Test port. As shown in **Fig 2b,** when the input pulse (upper trace) goes HIGH, the diode blocks any bias injection, and the op amp's output (lower trace)—and therefore the lamp's brightness—remains constant. However, when the input pulse goes LOW, current flows out of the intensity-control potentiometer's wiper via the 22-kΩ

A pulser plus

Pulse-width-modulator (PWM) ICs—such as the LM3524—include several on-chip function blocks that aid application to circuit designs other than regulated power supplies. By gaining an understanding of these circuits' operation, you'll discover how to employ a PWM in many applications.

The **figure** depicts the PWM's major functions:

- An on-chip voltage regulator supplies a stable 5V, 50-mA output for external usage in addition to handling all on-chip supply requirements. Capable of operating over an input voltage range of 8 to 40V (pin 15), this stage's output (pin 16) varies no more than 30 mV with a varying input. Thus, it provides an excellent reference level for closed-loop feedback schemes.
- The differential-input transconductance error amplifier (pins 1 and 2) has a typical open-loop gain of 80 dB. Because the stage's output impedance equals approximately 5 MΩ, you can tailor its gain-vs-frequency characteristics by adding a suitable RC network to its output at pin 9. Additionally, you can override the amplifier's effects by applying a dc signal directly to pin 9 and thereby forcing the IC to a specific output duty cycle. This stage's common-mode input voltage can range from 1.8 to 3.4V.
- The current-limit (CL) comparator (pins 4 and 5) can override the error amplifier and take control



Pulse-width-modulator ICs *contain several sense-and-control function blocks that extend the device's capabilities to other application areas. Error-voltage-amplifying, current-sensing and logic-level-shutdown stages are part of the chip's resources.*

of the output's duty cycle. This takeover occurs when the inherent 200-mV threshold is exceeded. At that level, the output's pulse width decreases to approximately 25%. And if the input signal increases to 210 mV, the output's duty cycle drops to 0%.

- The oscillator generates the comparator's reference ramp and the toggle (T) flip flop's clock signal. Set by timing capacitor C_T (pin 7) and resistor R_T (pin 6), the oscillator's frequency ranges from at least 1 kHz to 300 kHz. With the oscillator's output pulse (pin 3), you can disable ("blank") transient-sensitive external circuits during the PWM's switching phase.
- The pair of alternately switched output transistors considerably extends the device's versatility by providing two control options: First, by connecting the transistors in parallel, you can achieve output pulse-width duty cycles spanning 0 to 90% at a 100-mA peak current; second, you can operate these transistors independently in a push/pull configuration. Under these conditions, you can vary the duty cycle for each device from 0 to 45%.

resistor. This action causes the servo loop to lower the drive level to the lamp proportionately.

Note again how the lamp's ON and OFF times differ. But at high intensity levels, the lamp's on/off characteristics reverse themselves (**Fig 2c**) because the lamp then acts as a more efficient radiant-energy source.

µPs read pulse width vs temperature

In a second application, a µP-based data-acquisition system can directly monitor a wide temperature range, using **Fig 3**'s design. The temperature transducer, an LM135 IC, provides a highly linear 10-mV/°K output voltage over its calibrated range of −55 to +150°C. (You can operate the IC to 200°C on an intermittent basis.) The voltage-to-pulse-width conversion circuits—the op amp, PWM and associated networks—can convert any slowly changing 0.1 to 5.0V input signal to a 0 to 500-µsec-wide output pulse with 0.1% linearity. Thus, this scheme satisfies many data-acquisition requirements without modification; just connect an unknown signal to the 100-kΩ input resistor.

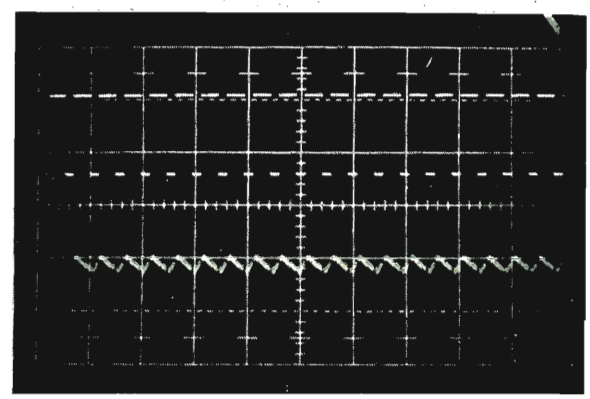
In **Fig 3**'s configuration, the input resistor string divides down the temperature transducer's output and applies it to the op amp's noninverting (+) input. This positive input voltage, once amplified, directly drives the PWM's on-chip comparator. (The on-chip error amplifier isn't used because its limited common-mode input range of 1.8 to 3.4V can't encompass the overall design's full capability. The off-chip LM358, on the other hand, handles inputs down to 0V.)

The PWM responds to a variable input voltage by generating a variable-width output pulse: 0.1V yields a zero-width output pulse and 5V produces a 500-µsec-wide output. The resulting TTL-compatible output pulse is clipped to 1.235V by the LM185 and integrated by the 1-MΩ/0.1-µF network. This dc feedback voltage gets summed at the op amp's inverting (−) input and linearizes the voltage-to-pulse-width conversion. (The 1000-pF feedback capacitor provides loop stability.) Adjusting the converter to data-acquisition requirements proves simple: Trim the 5-kΩ potentiometer for the proper pulse width at a known input temperature.

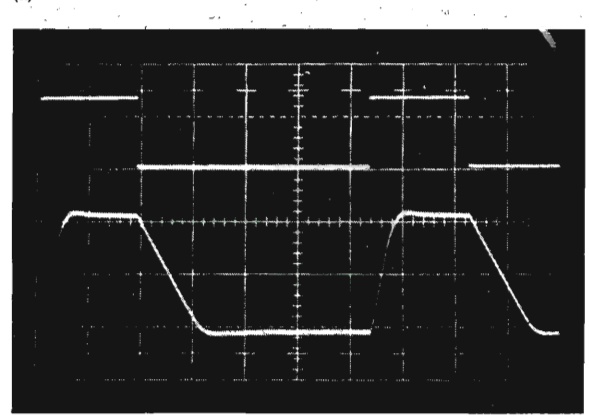
Pulse-width-control an oven

Fig 4 shows how you can regulate an oven's temperature using just the pulse-width-modulator chip. Here, a platinum resistance temperature detector (RTD) functions as the variable element in a resistive-bridge circuit. When you first apply power, the RTD—with its positive temperature coefficient—has a lower resistance than the corresponding 2-kΩ resistor in the bridge, and as a result, the LM3524's + input is at a more positive voltage than its inverting input. This imbalance forces the PWM's output pulse to its maximum value of 90%; it also turns on the 2N3507 power transistor and thus the oven's heater. When the oven reaches its operating temperature, the servo shuts down to the value needed to maintain temperature equilibrium.

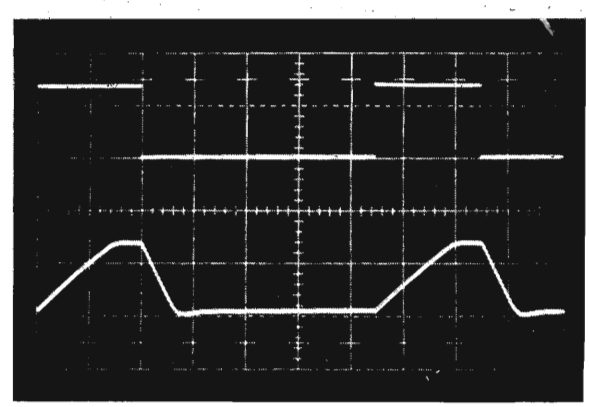
The 330-kΩ/4.7-µF combination sets the servo's gain



(a)



(b)



(c)

PHOTO	TRACE	VERTICAL	HORIZONTAL
(a)	UPPER	10V/DIV	100 µSEC/DIV
	LOWER	0.005V/DIV (ON 1V DC LEVEL)	
(b)	UPPER	5V/DIV	1 mSEC/DIV
	LOWER	0.05V/DIV (ON 1V DC LEVEL)	
(c)	UPPER	5V/DIV	1 mSEC/DIV
	LOWER	0.05V/DIV (ON 1V DC LEVEL)	

Fig 2—A closed-loop-servo design *closely tracks and corrects for a lamp's changing intensity. As shown in* ***(a)****, when* ***Fig 1****'s lamp-driver transistor pulses ON (upper trace), the loop amplifier's output starts ramping up to re-establish the loop's stability. Note how the lamp's turn-on time is shorter than its turn-off time when operating at low intensity levels* ***(b)****. This situation reverses* ***(c)****, however, at high output levels.*

Hold an oven to within 0.1°C using an RTD and one IC

to approximately 55 dB at 1 Hz—more than adequate for most applications. Similarly, the 2.7-kΩ/0.2-μF timing components set the pulse's frequency to approximately 15 kHz, a point far removed from the servo's 1-Hz pole frequency. If you maintain a close thermal proximity between the RTD and the heater, this design easily maintains a 0.1°C control point over widely varying ambient temperatures.

A tachless motor controller

A tachometer or other speed-sensing device isn't necessary when you employ **Fig 5**'s motor controller. Instead of a tach, this scheme uses the motor's back EMF to bias the feedback loop that governs the motor's speed.

When you apply power, the PWM's + input lies at a higher potential than its − input. The PWM outputs a 90% ON pulse that (via the 2N5023) starts the motor turning (**Fig 6**) and feeds the 1000-pF/500-kΩ differentiator network. The LM393 compares this level with the PWM's 5V reference, and the resulting delayed pulse triggers the LF198 sample-and-hold (S/H) device. As shown in **Fig 6**'s waveforms (traces b and d), the S/H IC is triggered HIGH (ON) just as the 2N5023 stops supplying current to the motor (traces a and c). At this instant, the motor coils generate a flyback pulse that's damped by the shunt-opposed diode. But even after the flyback pulse decays, the motor's back EMF remains, and this voltage, held by the S/H chip when the trigger pulse ceases, then controls motor speed.

The 10-kΩ/4-kΩ divider attenuates the motor's back EMF to ensure that the S/H output doesn't exceed the PWM's common-mode input range. Additionally, the S/H's output is filtered to keep things quiet during the sampling period and clamped to prevent any negative-going signals from damaging the PWM input. (The S/H's 10-MΩ bleeder resistor prevents the servo from never achieving stability in the unlikely event that the 0.01-μF sampling capacitor charges to a level greater than the motor's back EMF.) The 39-kΩ/100-μF time constant sets the loop's frequency response, and the 60-kΩ/0.1-μF combination determines the pulse-modulation frequency (300 Hz). You avoid overshoot problems and aid the loop's transient response by employing the 2-kΩ resistor divider and diode network; this configuration limits the maximum output duty cycle to 80%.

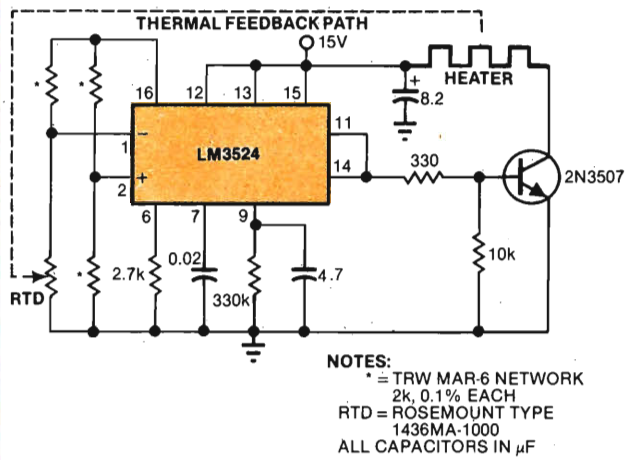


Fig 4—An oven's temperature remains constant *to within 0.1°C when a pulse-width modulator (PWM) controls the heater's power. Switching at 15 kHz, the PWM obtains the error signal from a platinum resistance temperature detector.*

Supply analog circuits at ±15V

Analog designers interested in the previous circuit seldom have much use for the 5V-only dc power supplies that digital designs thrive on. They will, however, find plenty of use for **Fig 7**'s design; it converts a 5V source into a ±15V, 100-mA supply suitable for analog designs.

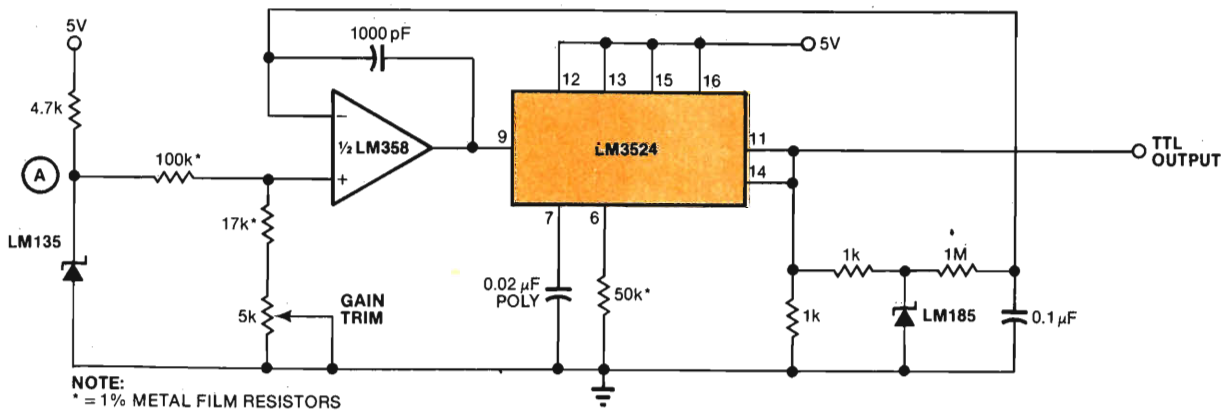


Fig 3—Temperature-to-pulse-width conversion *results when an LM135 transducer provides a temperature-dependent error signal directly to the pulse-width modulator's comparator input. The TTL output's pulse width varies from 0 to 500 μsec for a 0.1 to 5V input swing at point A.*

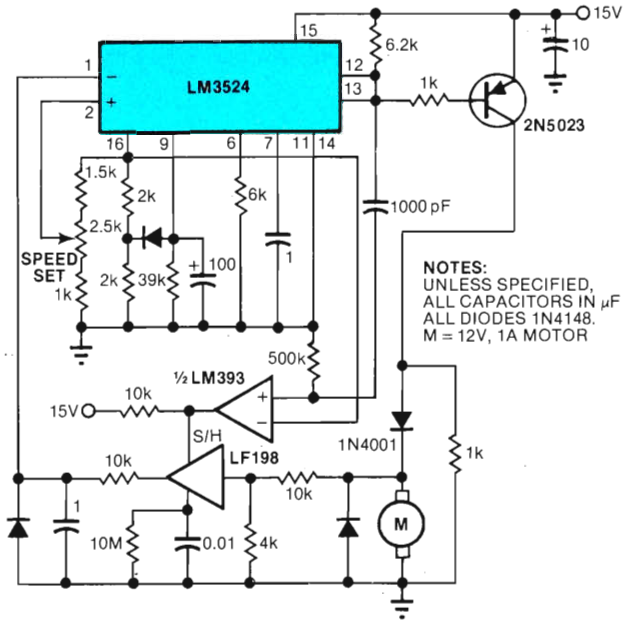


Fig 5—A motor's back EMF *provides the error signal in this motor-speed-control servo loop. After passing through a sample/hold stage* ***(Fig 6),*** *the smoothed error signal feeds the pulse-width modulator's control input.*

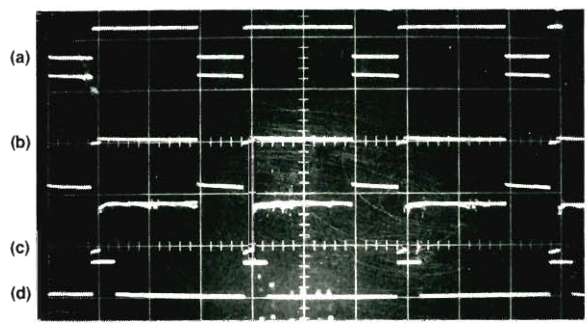


Fig 6—The motor's back EMF is sampled *(traces b and d) at the time* ***Fig 5****'s motor-drive transistor stops conducting (traces a and c). Although the motor generates a flyback pulse when the drive current stops, the remaining back voltage is what's held.*

Unlike the previous examples, the LM3524's on-chip output transistors here operate out of phase to provide a pulse-width-modulated push/pull signal to the transformer's driver transistors. Switching at 30 kHz, the transformer's output is rectified and filtered to obtain complementary but unregulated dc output voltages. The 15V output feeds back via an adjustable resistor divider and is compared with a reference voltage by the PWM's error amplifier. (The reference must stay at 2.4V to ensure that the error amplifier operates within its common-mode range.) This feedback loop regulates the +15V output, and an LM137 supplies the −15V.

Overcurrent protection results when the PWM's on-chip current-limit comparator senses a 200-mV level across the 2N2219s' 0.33Ω emitter resistor. When the current exceeds this threshold level, the comparator shuts down the chip's internal drivers and thus the entire converter. You can disable the converter during, for example, power-up sequencing by applying a TTL HIGH at pin 10. **EDN**

Author's biography

Jim Williams, applications manager with National Semiconductor's Linear Applications Group (Santa Clara, CA), specializes in analog-circuit and instrumentation development. Before joining the firm, he served as a consultant at Arthur D Little Inc and directed the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art and collecting antique scientific instruments in his spare time.

Article Interest Quotient (Circle One)
High **473** ***Medium*** **474** ***Low*** **475**

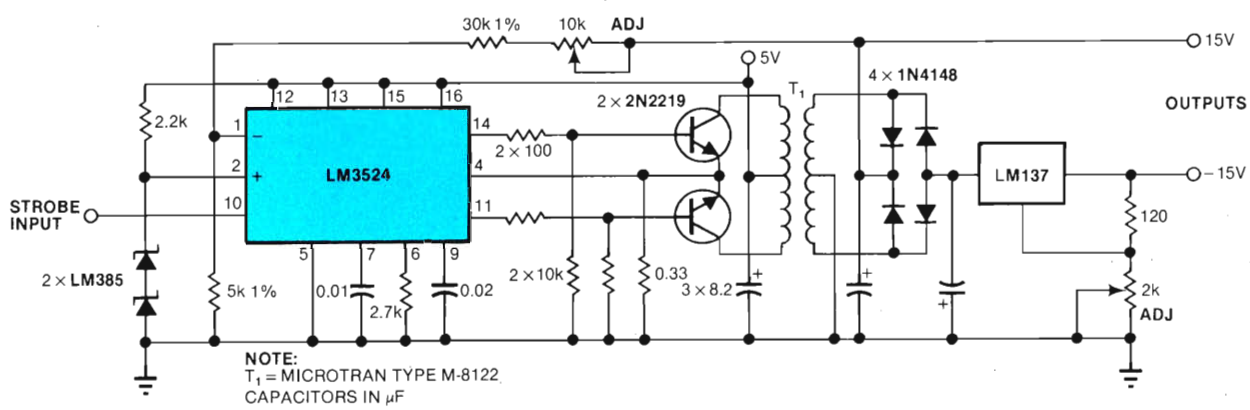


Fig 7—Convert a 5V digital-IC power supply *into a ±15V analog supply by using a pulse-width modulator to control the driver transistor's ON time. The PWM compares the 15V output against a reference and adjusts its output pulse widths accordingly. Overcurrent protection comes from sensing the driver transistors' emitter current, and a TTL-level input permits power-up sequencing.*

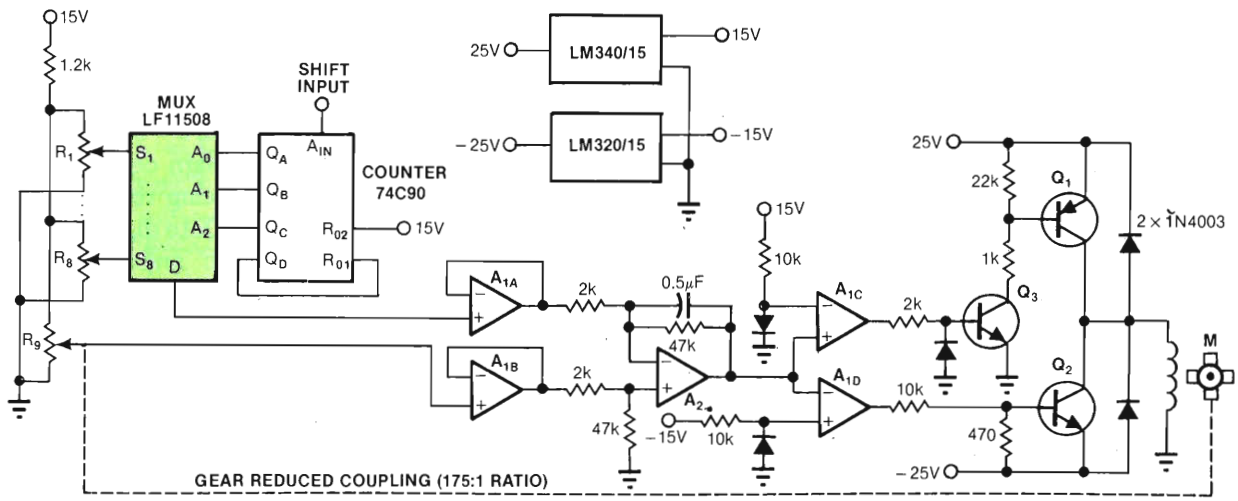
Increase your design options with analog-MUX ICs

Useful for more than commutating analog signals in data-acquisition systems, multiplexer ICs can also provide alternative and often superior solutions to many design problems. Applications range from servo positioning to waveform synthesis.

Jim Williams, National Semiconductor Corp

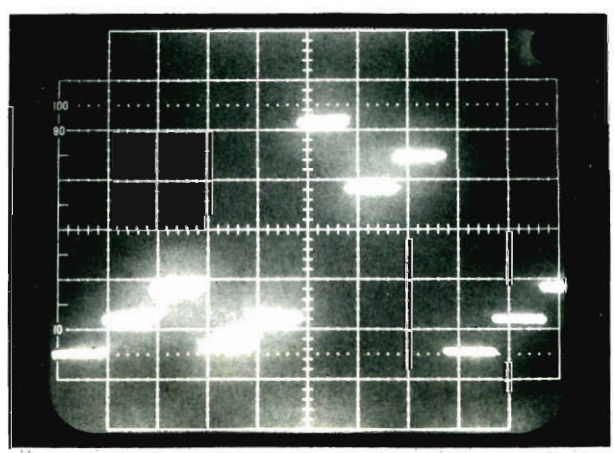
An analog data-multiplexer (MUX) IC's capabilities provide you with an additional tool for solving a range of diverse design problems. These features—fast multipole switching, high input-to-output isolation and direct digital interfacing—allow you to achieve some interesting and useful circuit realizations.

The design shown in **Fig 1,** for example, uses an 8-pole MUX in an arrangement that permits setting a servomotor in any of eight predetermined positions. You can preset these positions—via potentiometers R_1



NOTES:
A_1 = LF444
A_2 = LF441
UNMARKED DIODES = 1N4148
Q_1 = 2N5023
Q_2 = LM395
Q_3 = 2N2222
R_1 - R_8 = 50k
R_9 = SPECTROL 500-173, 5k
M = MOTORDYNE 1150-1

(a)



(b)

VERTICAL	HORIZONTAL
2V/DIV	200 mSEC/DIV

Fig 1—A servomotor's shaft position *settles into one of eight MUX-selected locations when a motor-driven potentiometer (R_9) balances out the addressed potentiometers' (R_{1-8}) preset level* ***(a).*** *Driven by a Shift pulse* ***(b),*** *the counter sequentially selects—via the MUX—each reference voltage.*

Analog-multiplexer ICs steer servomotors to random positions

through R_8—and then sequentially home the motor in. And because the drive circuits are complementary, the motor can run bidirectionally.

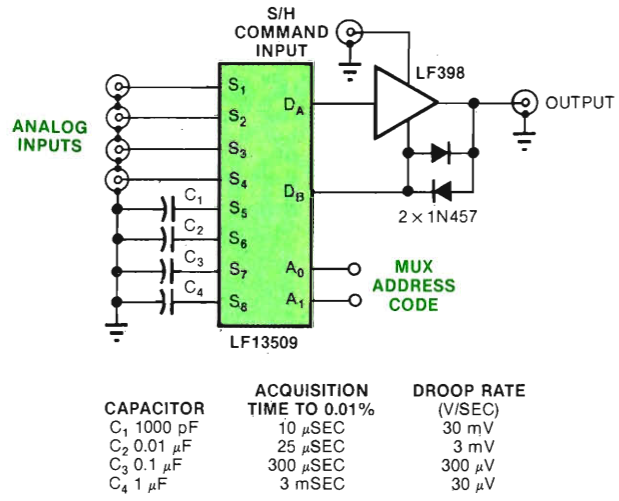
Assume power has just been applied and the counter's output is 0000. This all-ZERO input to the MUX closes its first switch (S_1) and feeds R_1's wiper voltage into the feedback loop. The potential difference between R_1's output and the servo potentiometer's (R_9) gets amplified by A_{1A} and A_{1B} and fed to A_2. This stage algebraically sums the signals and drives A_{1C} and A_{1D}, amplifiers configured as a dual limit comparator with deadband. Depending on A_2's output polarity, the appropriate comparator outputs a high-level voltage and turns its associated driver on. This action in turn drives the motor in the direction necessary to force a null at A_2's output. When that output falls within the diode-generated 0.6V deadband, both comparators' outputs drop LOW, and the motor stops.

A_2 operates at a gain of 30 and thus provides adequate sensitivity for precise positioning. Good loop dynamics result from using ±25V supplies and the indicated gear reduction ratio. (The 0.5-μF capacitor in A_2's feedback path sets loop roll-off.)

You step the motor through its positions by applying a Shift pulse to the counter. Upon application of the pulse, the MUX advances to its next switch position, and the different preset voltage level again forces the servo to seek a new position, rebalancing the loop.

Fig 1b, a stored-trace display of the MUX's output port, shows the servo at work. In it, eight discrete positions are sequentially selected in a dispersed, nonmonotone fashion. (Note how you can attain any desired positioning sequence without requiring the loop to hunt through any intermediate locations.) This scheme doesn't requre a voltage reference because both the servo's and the position-setting potentiometers' levels get derived from a common supply. Additionally, because the shaft's positions are "stored" by the potentiometers' settings, the design doesn't require a power-up initialization or sequencing routine.

You can also use an analog MUX to digitally select an instrumentation amplifier's gain and frequency response, making use of the techniques shown in **Fig 2.** In



CAPACITOR	ACQUISITION TIME TO 0.01%	DROOP RATE (V/SEC)
C_1 1000 pF	10 μSEC	30 mV
C_2 0.01 μF	25 μSEC	3 mV
C_3 0.1 μF	300 μSEC	300 μV
C_4 1 μF	3 mSEC	30 μV

Fig 3—A multiplexer selects this sample/hold amplifier's 1-of-4 inputs *and its acquisition time. Requiring only a 2-bit address, the 4-channel MUX can apply any hold capacitor to any input signal.*

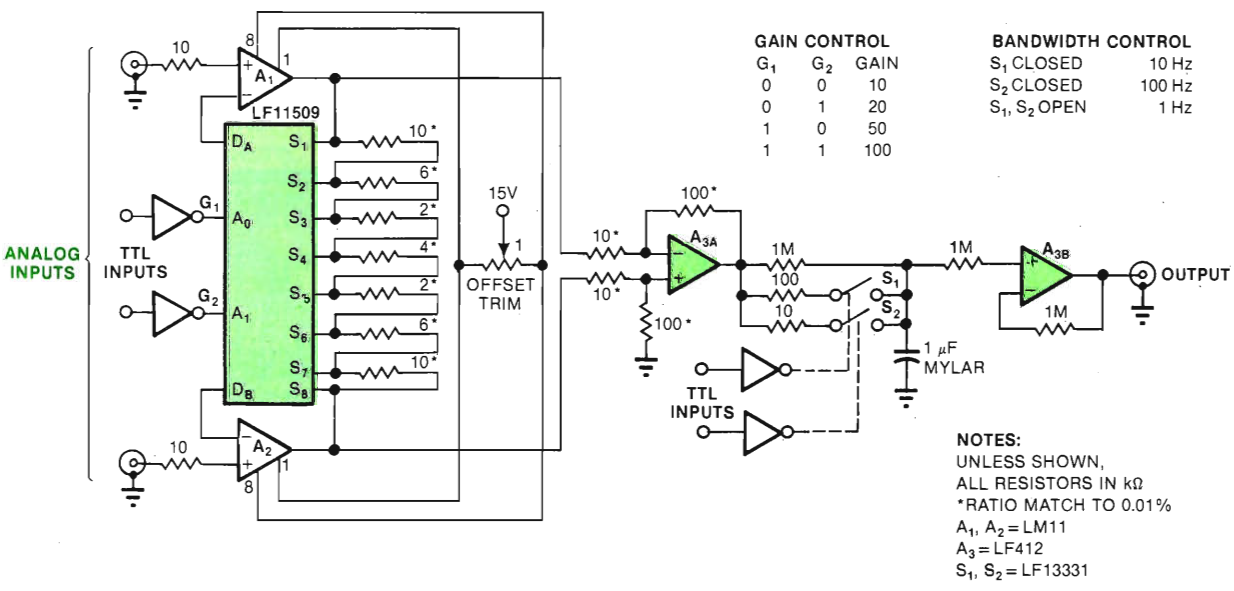


Fig 2—An instrumentation amplifier's gain and response *are controlled by a 4-bit digital signal. A 4-channel differential MUX decodes two bits and selects the amplifier's gain resistors; the remaining two bits determine the circuit's bandwidth.*

this approach, a 4-channel differentially switched MUX selects the feedback resistors for the design's input stages, A_1 and A_2. These stages' differential outputs get summed and amplified at a gain of 10 by A_{3A}. The resultant single-ended signal feeds an RC low-pass network consisting of 1-of-3 switch-selected resistors and a 1-μF capacitor. The final stage (A_{3B}) functions as an output buffer.

Thus, with a 4-bit digital signal, you can determine the amplifier's gain and response; two bits set the gain and the remaining two set the response as shown in **Fig 2**'s tables. You can realize true instrumentation-amplifier performance by using LM11s for A_1 and A_2; circuit drift then remains within 2 μV/°C, and you can achieve a CMRR of 100 dB with 0.01% resistor matching.

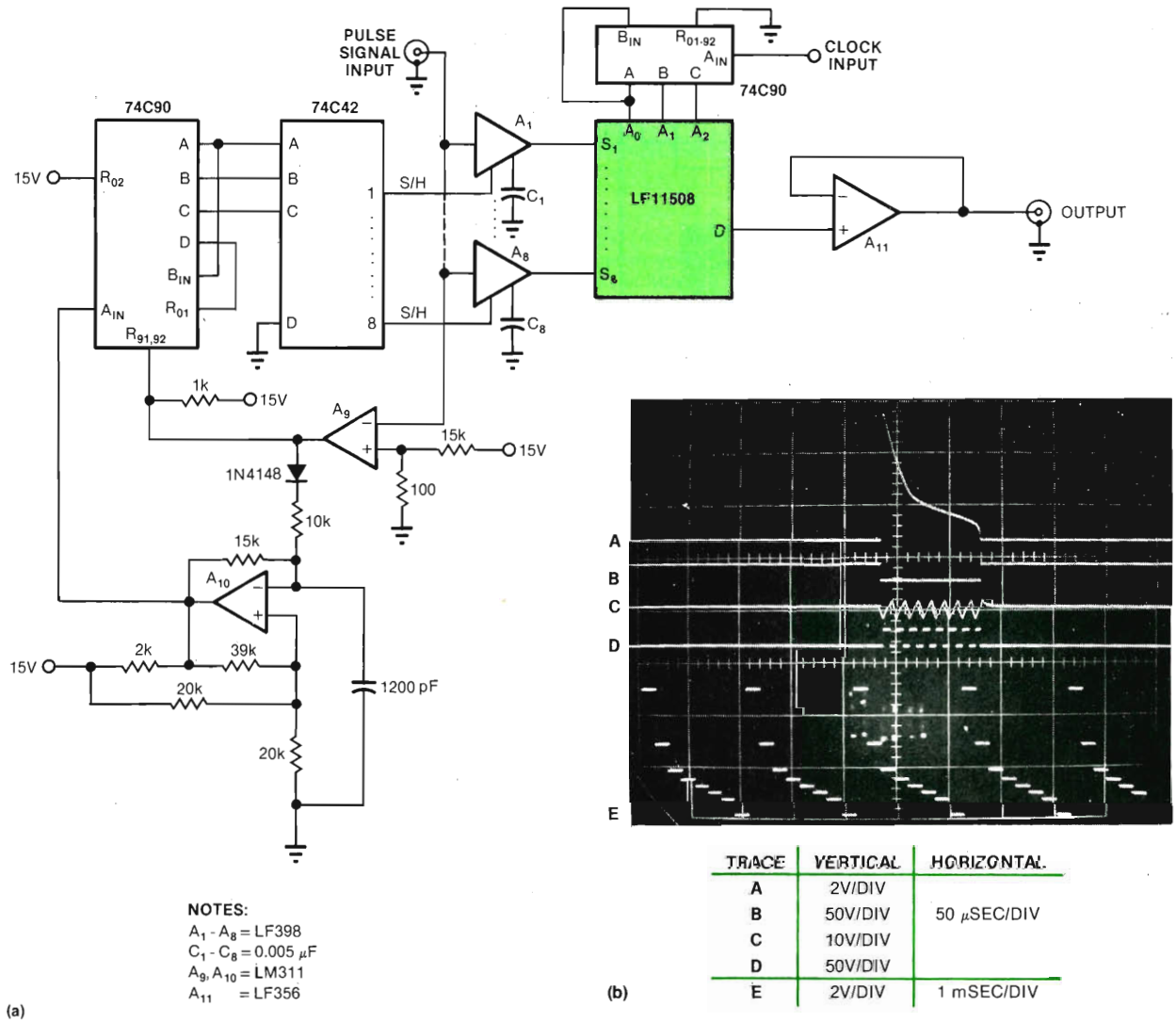
MUX a S/H amplifier for variable performance

Another analog-MUX application occurs when you're using sample-and-hold (S/H) amplifiers, which are usually constrained to processing a single input signal over a limited range of acquisition times and droop rates. The MUX-based design shown in **Fig 3** not only accepts any of four inputs, it also provides a wide range of acquisition and droop options.

This approach employs a 4-channel differential MUX to sort out the input and hold-capacitor options; half of the MUX selects the desired input, and the other half determines the in-circuit hold capacitor's value. Because any address code simultaneously selects the corresponding switches in both halves of the MUX, you can use any desired hold capacitance for any input.

A flash sampler captures single events

Fig 4a illustrates a technique for using analog MUXs for capturing single-shot or low-repetition-rate waveforms and then repetitively displaying the signal on an oscilloscope. It doesn't require a pretrigger signal because the input signal itself initiates the sampler



TRACE	VERTICAL	HORIZONTAL
A	2V/DIV	
B	50V/DIV	50 μSEC/DIV
C	10V/DIV	
D	50V/DIV	
E	2V/DIV	1 mSEC/DIV

Fig 4—This flash-sampler design (a) *captures single-event signals and provides an instant and repetitive scope display. An incoming signal (**(b)**, trace **A**) triggers A_9 **(B)**, resets the counter and starts the oscillator A_{10} **(C)**. A_{10}'s output **(D)** drives the counter that sequentially addresses the sampling amplifiers, A_1 through A_8. A clocked counter then steps through the MUX's switches and reconstructs the sampled input **(E)**.*

An analog flash converter can provide an instant signal replay

string. And because the circuit's output is independently clocked, you can vary the scope's display rate to suit your requirements.

An incoming signal (**Fig 4b,** trace **A**) triggers comparator A_9 LOW, as shown by trace **B.** This action allows A_{10}'s 15-kΩ/1200-pF combination to start charging (**C**); as a result, A_{10} outputs a pulse train (**D**). Advanced in count by these pulses, the counter's BCD-encoded output gets decoded by the 74C42 and is used to sequentially drive the eight paralleled sample/hold amps (A_1 through A_8). In this manner, each S/H stage acquires a fraction of the input signal.

When the input signal ceases, A_9's output again goes HIGH, A_{10} no longer generates pulses and the sampling procedure stops. To display the stored waveform, enable the clock input to the MUX-controlling counter. The counter's outputs sequentially address the MUX's switches, and stored signal segments go to the output buffer (A_{11}). Trace **E** demonstrates how you can repetitively display the reconstructed waveform at a rate governed by the clock's frequency.

A μC-driven MUX calibrates strain gauges

Fig 5's design shows how you can use a MUX to realize an autocalibration arrangement that eliminates

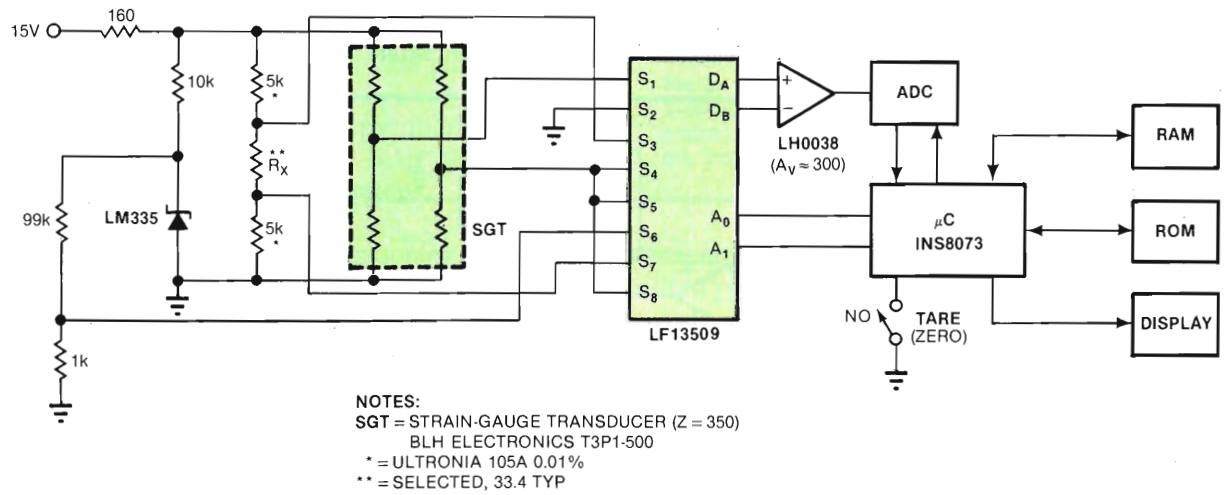


Fig 5—Strain-gauge calibration *results when a μC-controlled analog MUX sequentially acquires the bridge's characteristics. Parameters such as temperature dependence and full-scale output get A/D converted and stored in RAM. Then, after a weight is measured and converted, the μC runs a correction-factor program and displays the result.*

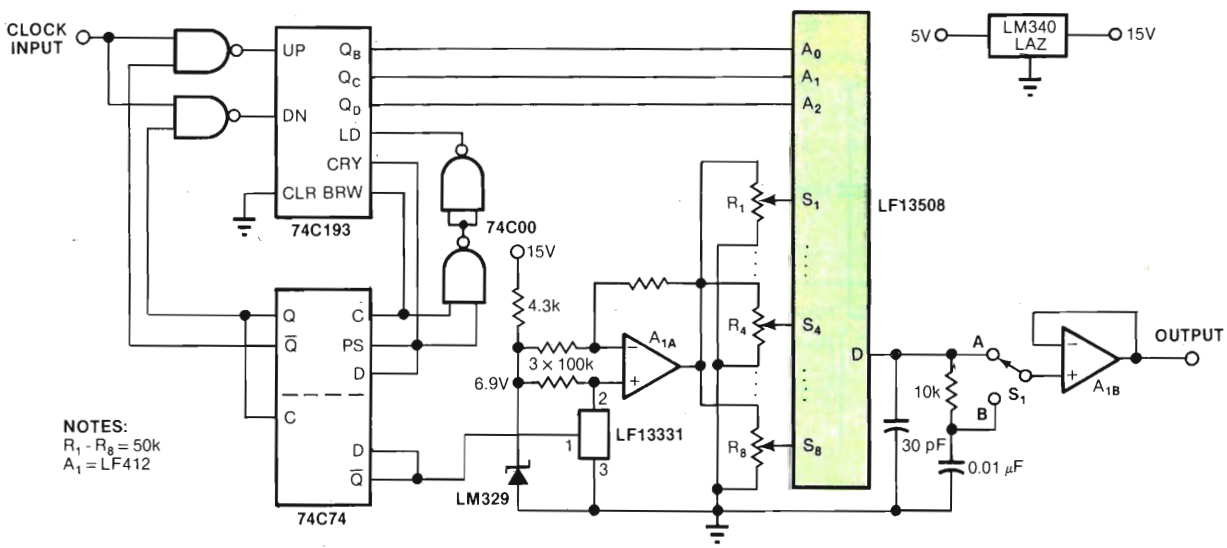


Fig 6—A programmable waveform *is created when a counter-driven 8-channel MUX samples preset potentiometers. When clocked, the counter counts up and then down and in the process switches the amplifier's input between 6.9V and ground. This action permits the amplifier to synthesize both the positive- and negative-going portions of the waveform, as shown in* ***Fig 7.***

almost all of the errors inherent in strain-gauge load-cell transducer measurements. Errors arising from drift over time and temperature are cancelled, and you can interchange transducers without having to rezero or recalibrate the circuit's gain. This design performs four separate operations to determine the factors necessary for correcting transducer output.

The measurement cycle commences when the μC switches the MUX into position 1. This action connects the strain gauge's output to the instrumentation amplifier. After amplification, the analog signal gets converted to a digital equivalent and stored in the RAM. When advanced to position 2, the MUX acquires the output of the load-cell-mounted LM335 temperature sensor. This value is also amplified, converted and stored in memory. (Note that the LM335's high output must be divided to prevent saturating the amplifier.)

The load cell's precise full-scale output voltage gets acquired when the MUX is in position 3 and connected to R_X, the cell-mounted resistor. By making this data inherently available with each cell, the system can ascertain (and correct for) the cell's gain slope. This capability eliminates the need for recalibration whenever you change cells. Position 4 provides the system with an electrical zero by connecting both of the amplifier's inputs to the bridge's common-mode point.

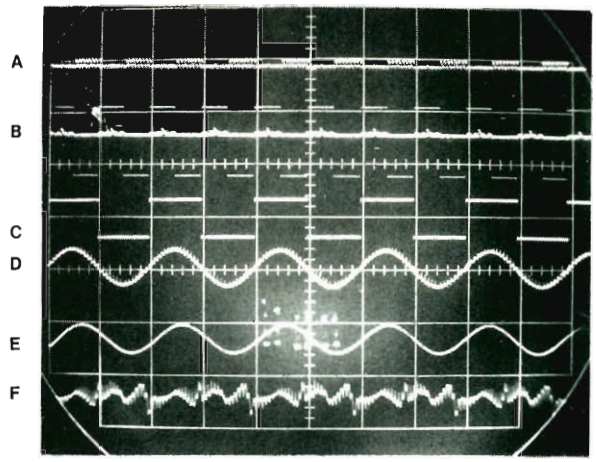
Physical-zero information (ie, tare (container) weight) is fed to the μC when you operate the pushbutton with no load on the cell. (You must perform this operation only when the system is turned on or after a different cell has been connected.) The system's memory then holds values for zero, the loaded bridge's output, its full-scale output and its temperature. Additionally, a tare-weight value has been determined. Using this data, the μC's program can calculate the strain gauge's precise loading regardless of drifts or the cells' individual gain-slope characteristics.

The temperature information provides a first-order correction factor for the relatively small effect that ambient temperature has on gain slope and zero. The bridge's voltage needn't be stabilized because it's common to the gain-calibration string and therefore ratiometrically cancels. In fact, the system's stability is governed solely by the stability of the gain-calibration string's resistors. MUX-controlled systems of this type achieve repeatability of one part in 20,000 in industrial environments.

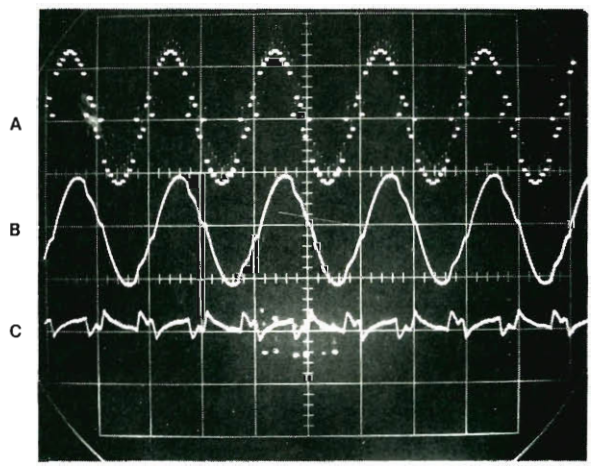
Switched resistors generate waveforms

Fig 6 diagrams how you can use an 8-channel MUX to generate a 32-piece approximation of any desired waveform—a sine wave demonstrates the approach. When clocked, the logic circuits combine to force the MUX to count up to eight. (The counter's Up/Down control inputs appear as traces **A** and **B** in **Fig 7**'s top photo.) When this operation is completed, the MUX counts down to zero and resamples the potentiometers' settings in the process. These two cycles create the positive half of the output's waveform.

The logic next inverts the potentiometers' voltage by



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	
B	5V/DIV	
C	20V/DIV	500 μSEC/DIV
D	20V/DIV	
E	20V/DIV	
F	0.5V/DIV	



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	
B	5V/DIV	500 μSEC/DIV
C	0.5V/DIV	

Fig 7—Waveform synthesis *proceeds when* ***Fig 6****'s counter cycles through its first up/down sequence (top, traces* ***A*** *and* ***B****). After this sequence, the D flip flop's Q output drives the amplifier's input (and therefore its output) LOW* ***(C)****. The counter/MUX combination recycles through the up/down sequence and creates the negative half of the waveform. The unfiltered* ***(D)*** *and filtered* ***(E)*** *outputs indicate how well a sine wave can be synthesized. This 32-step approximation results in a distortion level of less than 0.5%* ***(F)****. The bottom photo depicts how you can intentionally distort a waveform: The unfiltered* ***(A)*** *and filtered* ***(B)*** *outputs indicate that trace* ***C****'s 7% distortion is easily achieved.*

MUXing a strain-gauge bridge relieves recalibration pains

grounding A_{1A}'s + input via an LF1331 FET switch. This action forces the amplifier's output to −6.9V, as shown by trace **C**. Concurrently, the logic again forces the MUX to count up to eight and back down to zero, an action that synthesizes the negative half of the output's waveform. At the conclusion of these 32 counts, the logic resets, A_{1A}'s output switches to a 6.9V level and the entire cycle repeats.

When appropriately set, the potentiometers can provide the correct levels for synthesizing a sine wave, as shown by trace **D**. When filtered, this signal (**E**) contains less than 0.5% distortion (**F**). As the bottom photo in **Fig 7** shows, you can intentionally distort the output by resetting the potentiometers. Trace **A** displays the 32-piece approximation of the distorted signal, and **B** shows the filtered version. A distortion analyzer's output signal (**C**) indicates a 7% distortion level. **EDN**

Author's biography

Jim Williams, manager of National Semiconductor Corp's Linear Applications Group (Santa Clara, CA), has made a specialty of analog-circuit design and instrumentation development. Before joining National, he was a consultant with Arthur D Little Inc in analog systems and circuits. From 1968 to 1977, Jim directed the Instrumentation Development Lab at the Massachusetts Institute of Technology, where in addition to designing experimental biomedical instruments, he was active in course development and teaching. A former student of psychology at Wayne State University, he lists tennis, art and collecting antique scientific instruments as his leisure interests.

Article Interest Quotient (Circle One)
High **479** ***Medium*** **480** ***Low*** **481**

Conversion techniques adapt voltages to your needs

Different parts of your system often need specialized voltages. A variety of conversion techniques can help you obtain these voltages from the main supply.

Jim Williams, National Semiconductor Corp

Need more than one voltage in a single-supply system design? You can tailor the main system supply by using a variety of techniques; understanding how each works lets you choose the one most appropriate to producing the levels—and characteristics—you need.

Analog circuits need ±15V

Specifically, note that if you have a 5V logic rail available in your system but need ±15V, it's easy to construct a dc/dc converter with an oscillator, a transformer and a rectifier circuit. However, most dc/dc converters suffer from large noise spikes generated by the fast-switching oscillator. So if the analog circuitry is especially sensitive to power-supply noise, you can eliminate or minimize the switching noise by using an interrupt-driven converter or a full-duty-cycle, low-noise converter.

Fig 1 shows an interrupt-driven circuit. The LM3524 switching regulator runs open-loop; its Q_1-Q_2 output pair drives the step-up transformer. Unlike a standard

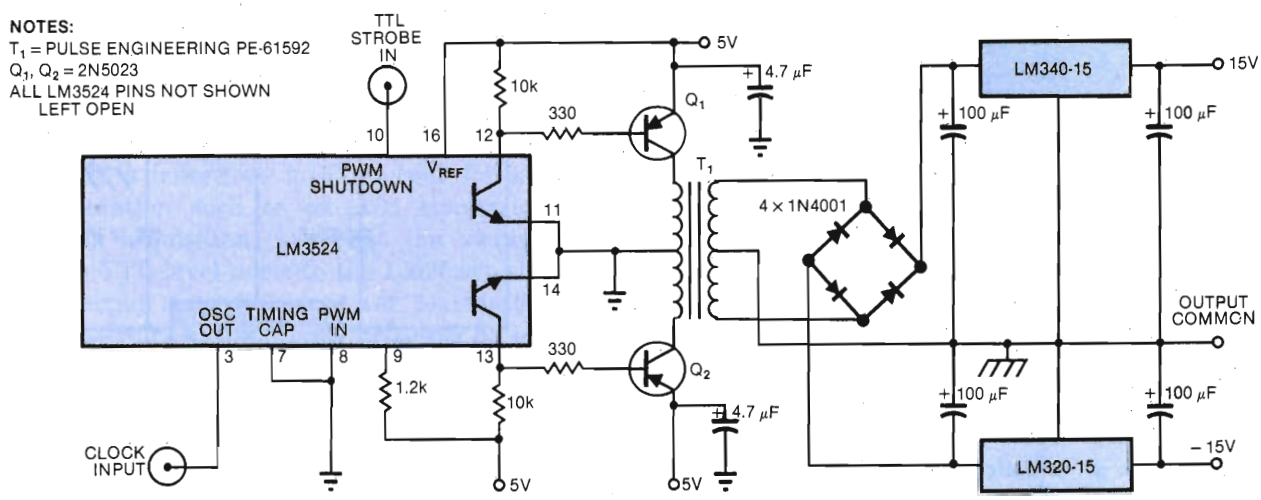
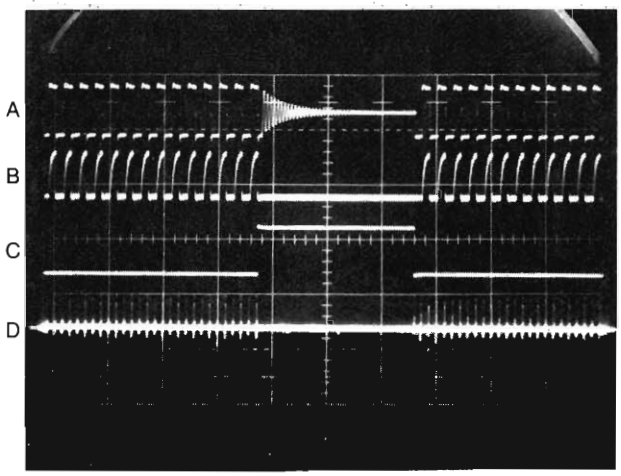


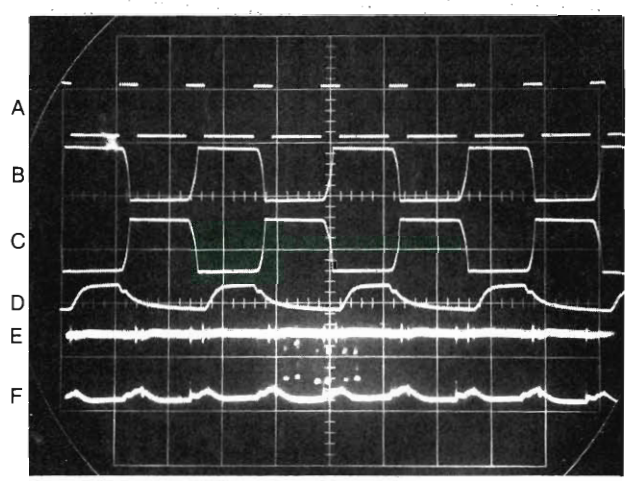
Fig 1—Totally noise free, *this 5V to ±15V converter stops running when you supply a TTL shutdown pulse. The 100-µF output capacitors provide voltage hold-up while your circuit operates.*

Interrupt switching for noise-free operation



TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	200 μSEC/DIV
B	1A/DIV	200 μSEC/DIV
C	5V/DIV	200 μSEC/DIV
D	20 mV/DIV (AC COUPLED)	200 μSEC/DIV

Fig 2—The center portion *of this scope photo shows the drop in output noise (trace D) that occurs when* ***Fig 1****'s converter shuts down.*



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	20 μSEC/DIV
B	10V/DIV	20 μSEC/DIV
C	10V/DIV	20 μSEC/DIV
D	500 mA/DIV	20 μSEC/DIV
E	2 mV/DIV (AC COUPLED)	20 μSEC/DIV
F	100 mV/DIV	20 μSEC/DIV

Fig 4—Barely discernible spikiness *is visible in the output (trace E) of* ***Fig 3****'s low-noise converter.*

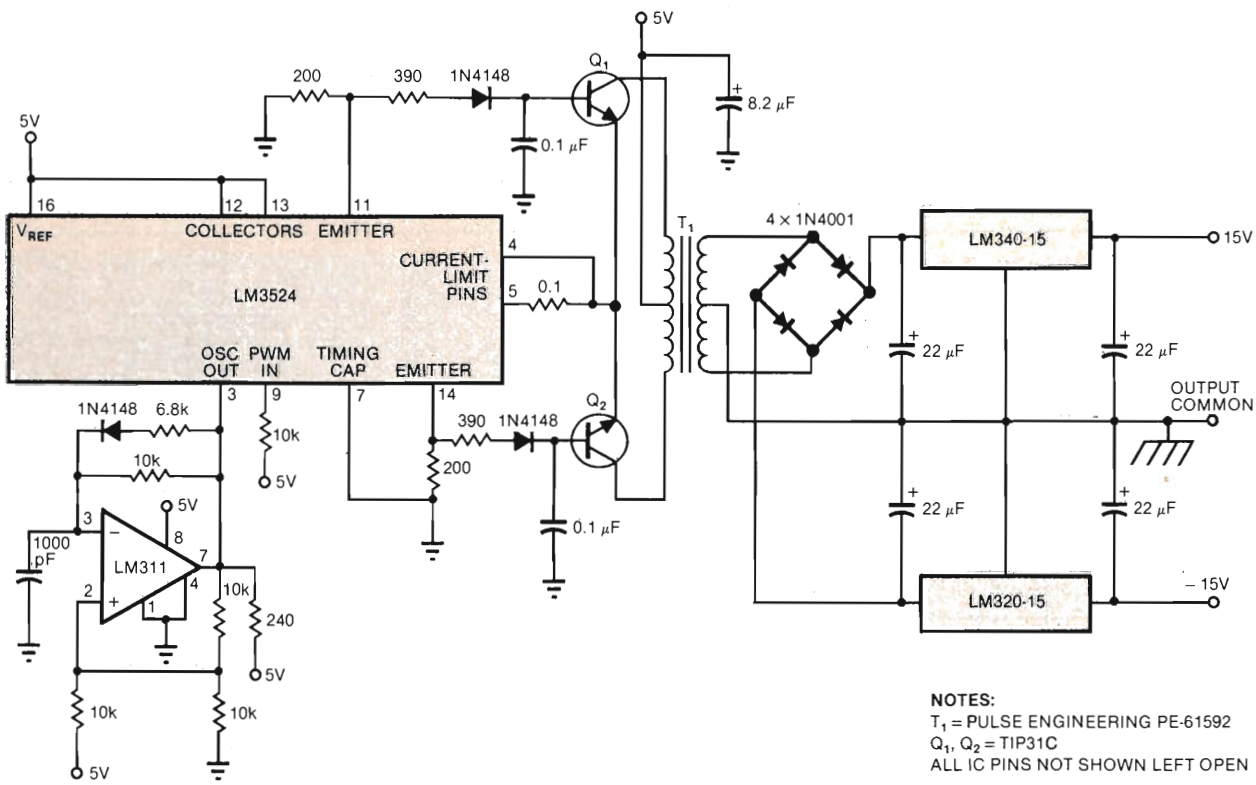


Fig 3—A low-noise converter, *this 5V to ±15V circuit runs continuously, but the output transistors' controlled turn-on and turn-off minimize spikes.*

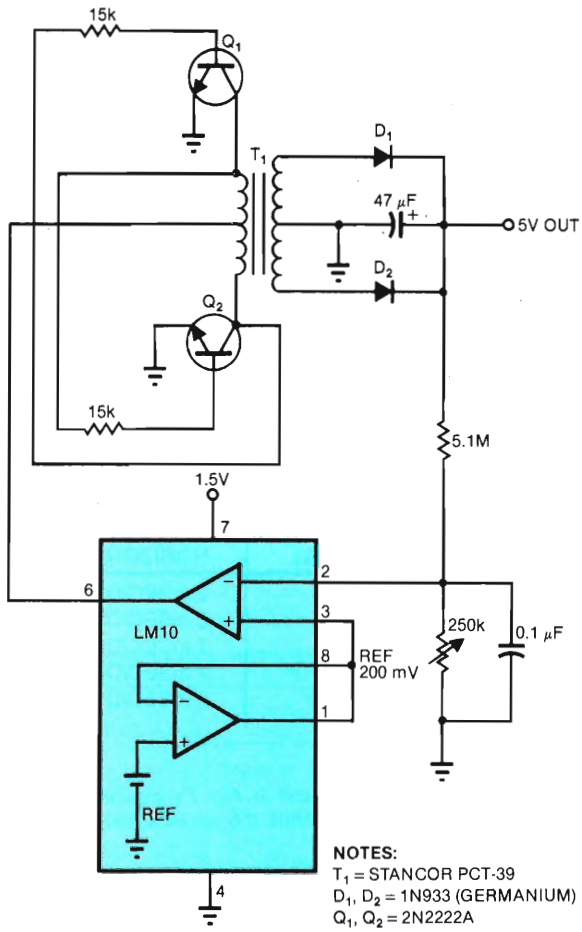


Fig 5—Powered by a 1.5V battery, *this 5V-output design can drive low-power circuitry for months from one cell.*

dc/dc converter, this circuit uses an external clocked oscillator, allowing you to synchronize the converter to the host system. To use this feature, you disable the LM3524's internal oscillator by grounding the capacitor timing pin and apply the system clock to the oscillator output, yielding a 50% switching duty cycle.

To obtain a noise-free ±15V output for a critical circuit operation such as an A/D conversion or a sample/hold acquisition, interrupt the switching by applying a TTL-level pulse to the LM3524's shutdown pin. This action stops the converter, leaving the large output capacitors as a virtually noiseless dc source to power the output regulators.

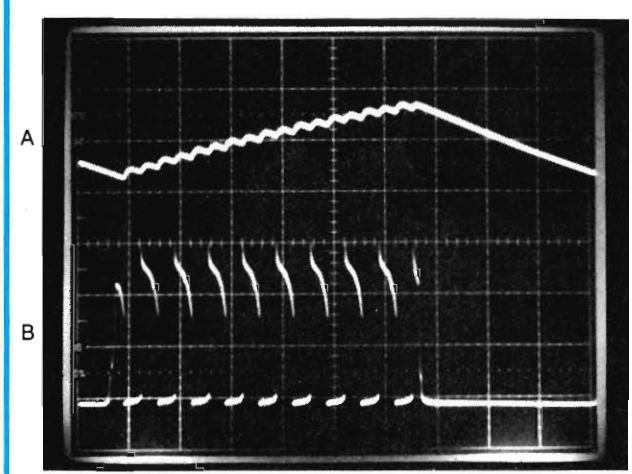
Fig 2 details the circuit's performance; traces A and B show Q_1's voltage and current waveforms, respectively (Q_2's waveforms are similar). Trace D depicts the 15V output line (the −15V line is similar): The noise pulses caused by the switching circuitry are clearly visible. When the interrupt pulse is applied (trace C), the noise disappears. The large output filter capacitors provide adequate ±15V holdup time for the critical operation required while the interrupt pulse is HIGH.

Don't interrupt—just quiet down

If you need a 5V to ±15V converter with low (but not necessarily zero) noise, consider the continuously running circuit shown in **Fig 3.** Here, the LM311 multivibrator clocks the LM3524 (**Fig 4,** trace A), whose internal oscillator is again disabled by grounding the timing-capacitor pin. While the LM311's output is HIGH, the LM3524 cuts the drive to Q_1 and Q_2, helping to minimize switching noise.

The main contributor to low-noise performance is the base-drive slowdown network used with Q_1 and Q_2: The 390Ω/0.1-μF time constant slows turn-on, and the diode forces base-emitter charge trapping to delay turn-off.

The effect of these components is evident in the Q_1-Q_2 collector-voltage waveforms (**Fig 4,** traces B and C) and Q_2's current waveform (**Fig 4,** trace D). Note that the LM311's long ON time permits no current to flow in Q_2 until well after Q_1 has turned off. Moreover, the current's rise and fall times are smoothly controlled and long, unlike those of the more common fast-switching converters. Therefore, very little harmonic content appears in the transformer drive, so converter output noise (**Fig 4,** trace E) is exceptionally low. In addition,



TRACE	VERTICAL	HORIZONTAL
A	0.1V/DIV (AC COUPLED)	10 mSEC/DIV
B	1V/DIV	10 mSEC/DIV

Fig 6—The on-demand operation *of* ***Fig 5****'s 1.5V to 5V converter is evident in this scope photo. The converter turns on when the output drops to approximately 4.93V and off when it rises to roughly 5.07V.*

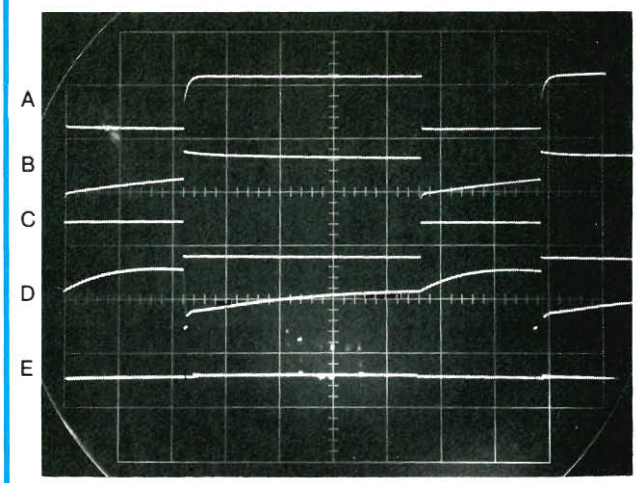
the disturbance to the 5V rail (**Fig 4,** trace F) is small compared with standard designs.

This circuit's low noise comes at the expense of efficiency and available output power, though: During the slow base transitions, Q_1 and Q_2 dissipate power, reducing efficiency to about 50% and available output to approximately 50 mA. Heat-sinking Q_1 and Q_2 won't help, either, because it involves the risk of secondary breakdown. The circuit is, however, short-circuit protected by the 0.1Ω emitter resistor and the LM3524's current-limiting circuitry.

Power circuits from a battery

What if your basic system supply is a battery? The circuit depicted in **Fig 5** supplies 5V from a 1.5V source—such as a battery, saltwater cells or a solar-cell stack. With 125-μA load current (typically 20 CMOS ICs), it runs for 3 months on one D cell.

The circuit is unusual because the amount of time required for Q_1 and Q_2 to drive the transformer is directly related to the load resistance. The LM10 op-amp/reference IC compares the converter's output with its own internal 200-mV reference via the 5.1-MΩ/250-kΩ voltage divider. Whenever the converter's output drops below 5V, the LM10 output goes HIGH, driving the Q_1-Q_2-T_1 oscillator circuit. The rectified transformer output then charges the 47-μF



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	2 mSEC/DIV
B	5V/DIV	2 mSEC/DIV
C	5V/DIV	2 mSEC/DIV
D	50 mA/DIV	2 mSEC/DIV
E	200V/DIV	2 mSEC/DIV

Fig 8—The inductor current *in* ***Fig 7****'s design (trace D) supplies the energy to generate the circuit's 200V output.*

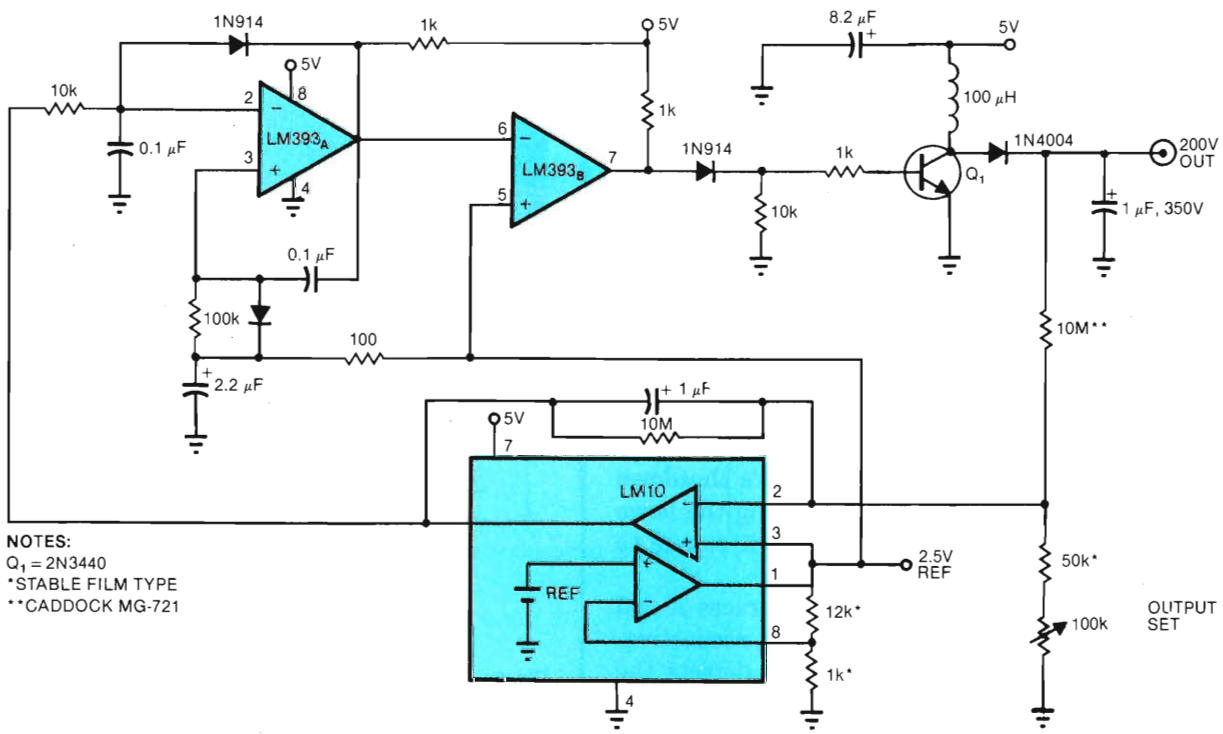


Fig 7—A 40-fold multiplication *of the 5V supply results with this flyback-type converter. It furnishes 200V into a 500-μA load.*

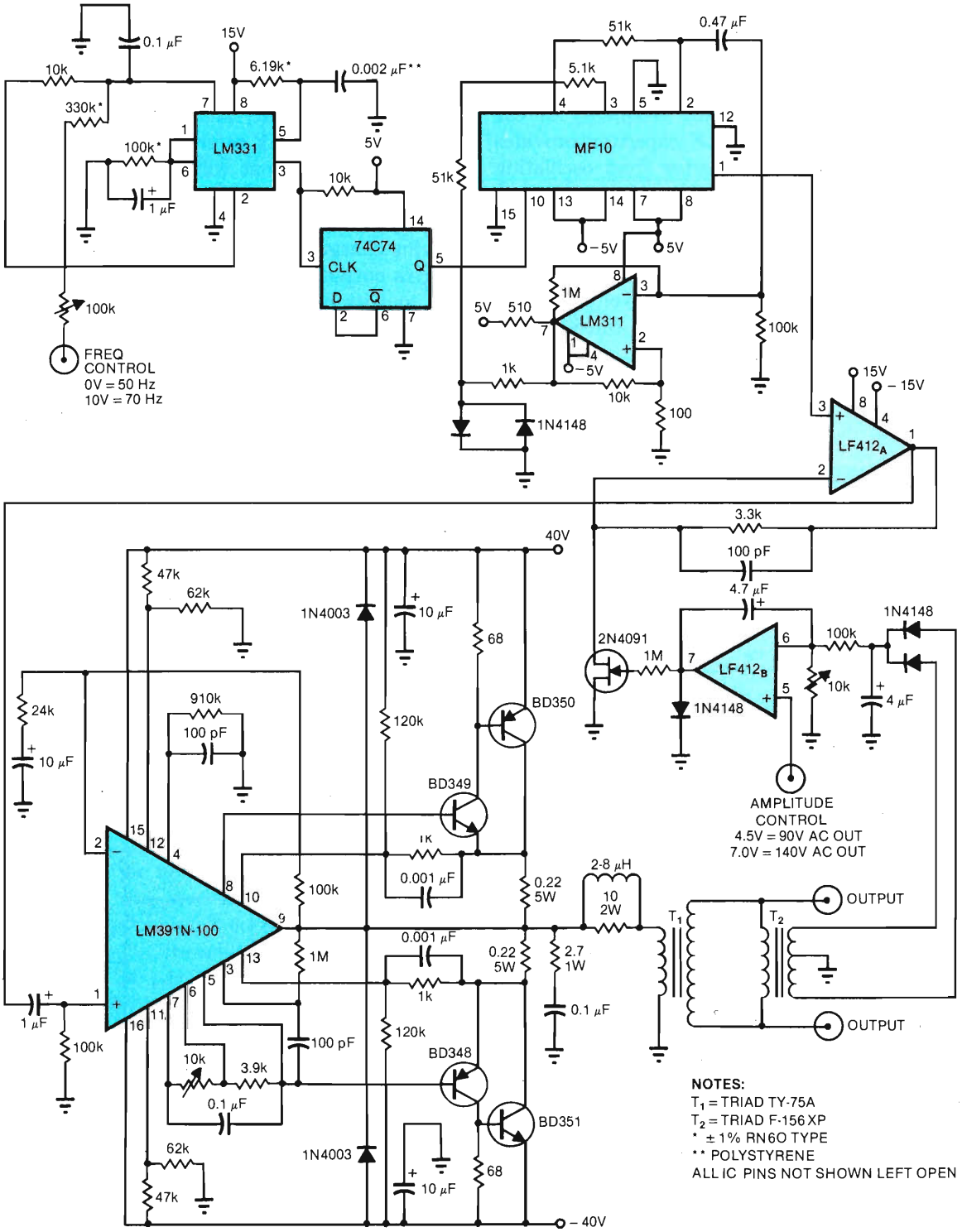


Fig 9—Test line-operated devices *with this variable-voltage and -frequency converter. From a 40V dc input, you can get 90 to 140V ac at 50 to 70 Hz.*

Use a flyback circuit to obtain high voltages

capacitor to a value high enough to cause the LM10 output to go LOW, thereby cutting off the oscillation.

In **Fig 6,** trace B shows the collector voltage of Q_1; trace A shows the converter's output voltage (ac coupled). Note that each time the output voltage drops a certain amount, the LM10 drives the oscillator, causing the output voltage to rise until it's sufficiently high to switch the LM10 to its LOW state.

The output load determines the frequency of the regulating action, and the 0.1-μF capacitor provides hysteresis, preventing the converter from oscillating around the trip point. Very low loading of the converter results in virtually zero oscillator ON time, while large loads cause the oscillator to run almost constantly (typical operating frequencies are between 0.1 and 40 Hz). The germanium rectifiers minimize voltage drop.

If you need a very high voltage, consider the flyback-type converter shown in **Fig 7.** It generates 200V (regulated) into a 500-μA load from a 5V supply and thus serves applications such as gas-discharge displays, piezoelectric transducers and strobe lamps. Half of the LM393 op amp ($LM393_A$) functions as a constant-width-output voltage-to-pulse-rate clock. The 0.1-μF/100-kΩ combination, together with the 2.5V from the LM10 op-amp/reference IC, fixes the output width at about 4 msec. The 100Ω/2.2-μF pair provides bypassing for the 2.5V reference, and the 0.1-μF/10-kΩ constant and the input voltage set clock frequency.

Each time $LM393_A$'s minus input charges above its plus input, its output goes LOW (**Fig 8,** trace A), drawing charge from both 0.1-μF capacitors. When the device's output is LOW, its minus input is clamped at 0.6V and its plus input (**Fig 8,** trace B) rises until it exceeds that level. Then the output goes HIGH, ending

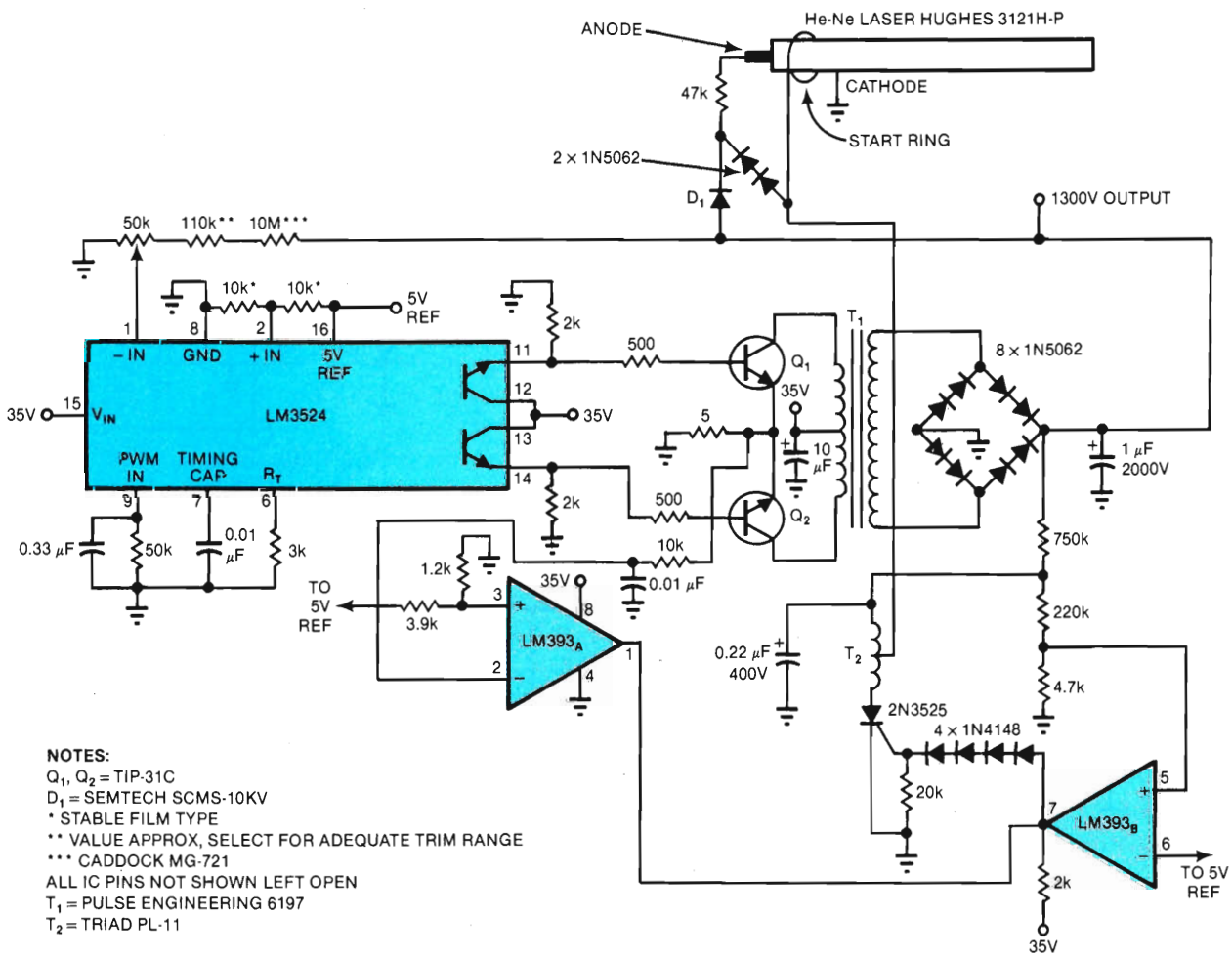


Fig 10—Start and run a laser *with this 35V to 1300V converter. It furnishes an 8000V pulse that repeats as often as needed until the laser starts.*

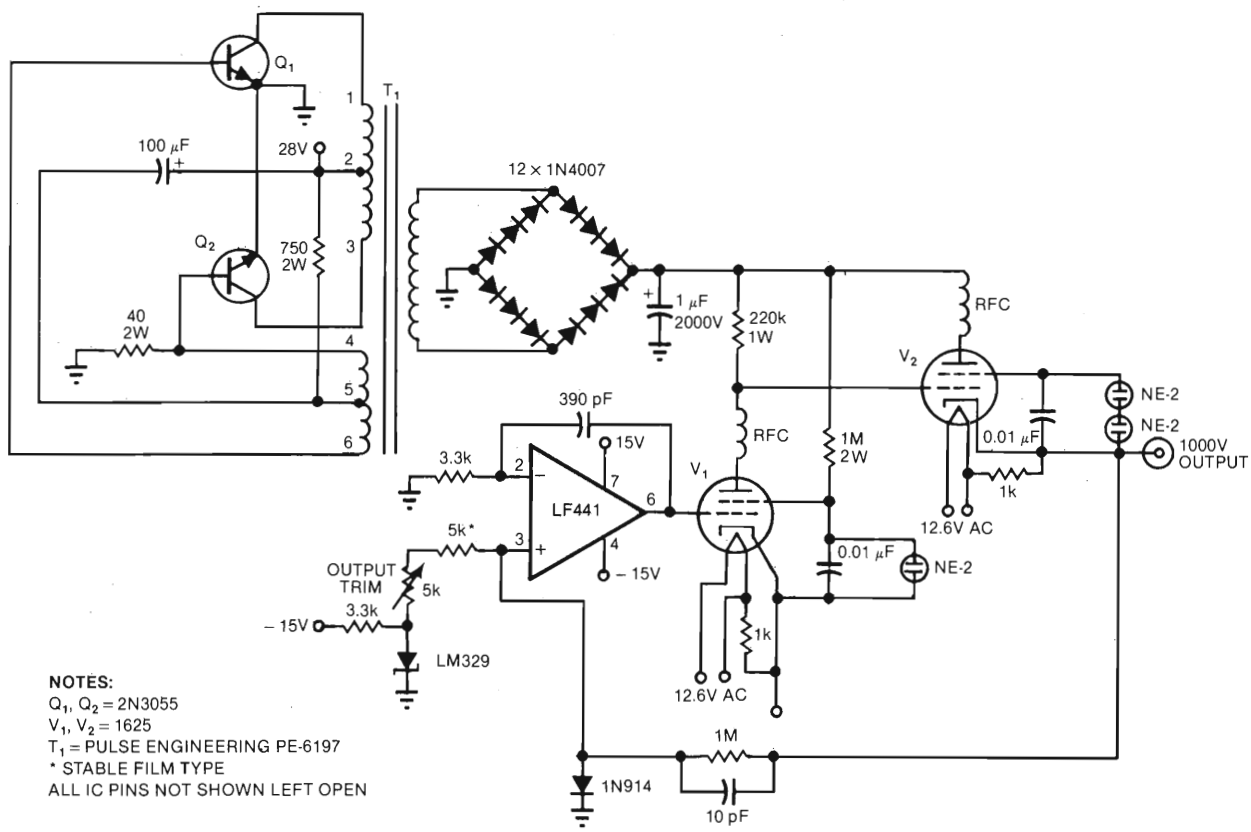


Fig 11—Using tried-and-true technology, *this ±15V to 1000V hybrid-semiconductor/vacuum-tube converter incorporates inexpensive components and is very forgiving of overloads.*

the timing cycle and reinitializing the entire process. The 1N914 diode prevents a differentiated positive response at LM393$_A$'s plus input, allowing the circuit to recover quickly for the next cycle.

LM393$_B$, meanwhile, inverts the clock's output and drives Q_1. When this op amp's output goes HIGH (**Fig 8**, trace C), Q_1 turns on, its collector current rises (**Fig 8**, trace D) and the 100-μH inductor stores energy. *(Ed Note: The current probe is ac coupled—the long tail is actually flat.)* When LM393$_B$'s output goes LOW, the magnetic field in the inductor collapses and Q_1's collector voltage rises to about 200V (**Fig 8**, trace E). This high-voltage spike gets clamped and stored by the 1N4004/1-μF combination at the circuit's output.

The LM10 compares a divided-down portion of the output with its 2.5V internal reference. The difference voltage at the LM10 output then closes the loop at LM393$_A$'s clock. The 10-MΩ/1-μF feedback components set loop gain and frequency compensation.

Vary voltage, frequency with ac line converter

If you must generate a variable-frequency and -amplitude ac supply from a 40V source, consider **Fig 9**'s circuit. This arrangement is ideal for testing 115V ac, 60-Hz line-powered loads for sensitivity to amplitude and frequency variations. The frequency of its sinusoidal output is voltage controllable from 50 to 90 Hz; output amplitude is also voltage controllable over a 90 to 140V ac range.

In the circuit, the LM331 V/F converter and flip flop form a voltage-controlled square-wave clock that drives the MF10 filter. That device, together with an LM311 comparator, forms a resonator that generates stable-amplitude sine outputs without using AGC circuitry. The MF10 operates as a Q-of-10 bandpass filter that rings at its resonant frequency in response to a step input. The LM311, upon receipt of this ringing signal, creates a square-wave input signal for the bandpass to regenerate the oscillation.

The bandpass output is the filtered fundamental frequency of a 50%-duty cycle square wave. The clock controls the filter's center frequency, in turn setting the oscillation frequency. The peak-to-peak swing of the MF10's square-wave input (defined by the back-to-

back diode clamps at the LM311 output) determines the circuit's output amplitude.

The LM331 is biased so that a 0 to 10V input yields a 50- to 70-Hz sine-wave output at the MF10. This output goes to $LF412_A$, whose output biases the LM391 circuit, a gain-of-5 power amplifier that drives step-up transformer T_1. A portion of T_1's output—fed back to $LF412_B$ via T_2 and its rectifier/filter network—gets compared at $LF412_B$ with the amplitude control voltage. $LF412_B$'s output then biases the 2N4091 FET, which controls $LF412_A$'s gain, closing the amplitude control loop.

This circuit achieves a fully isolated output because of the galvanic isolation provided by T_1 and T_2. It sources 10W of sine-wave power over a controllable range of 90 to 140V ac and 50 to 70 Hz.

Make a laser run with only 35V

A laser is a good example of a component that forms part of a larger system and has special voltage requirements. The He-Ne laser shown in **Fig 10,** for example, requires 1300V operating and an 8000V start pulse. You can meet both of these requirements by up-converting the system's 35V supply.

The LM3524 pulse-width-modulator IC, in conjunction with Q_1 and Q_2, drives T_1 to provide a stepped-up voltage. T_1's rectified and filtered output, via feedback to the LM3524, is a regulated 1300V. C_T and R_T set the 20-kHz switching frequency; the 50-kΩ/0.33-μF pair controls the loop's gain-rolloff characteristics. You trim the 1300V output (applied to the laser's anode) with the 50-kΩ Output Set potentiometer.

When you first apply power to the circuit, the 1300V is insufficient to start the laser; hence, very little current is drawn from the 1300V supply. The low supply current results in a small average current through Q_1 and Q_2, in turn resulting in a small voltage drop across the 50Ω emitter resistor. This voltage is below the threshold at $LM393_A$'s plus input, so the amplifier's open collector unclamps.

When the 0.22-μF capacitor at T_2 charges, the voltage at $LM393_B$'s plus input exceeds 5V, and its output goes HIGH, allowing gate current to flow into the SCR. The SCR then fires, dumping the 0.22-μF capacitor's energy through T_2, a flyback photoflash unit. This action causes an 8-kV spike to appear at the laser's start ring, normally causing gas breakdown and starting the laser. Diode steering prevents the spike from affecting the normal 1300V output.

When the laser starts, the Q_1-Q_2 emitter current increases enough so that $LM393_A$ is forced LOW, cutting off drive to the SCR and disabling the start circuitry. But if the laser does not start, $LM393_A$

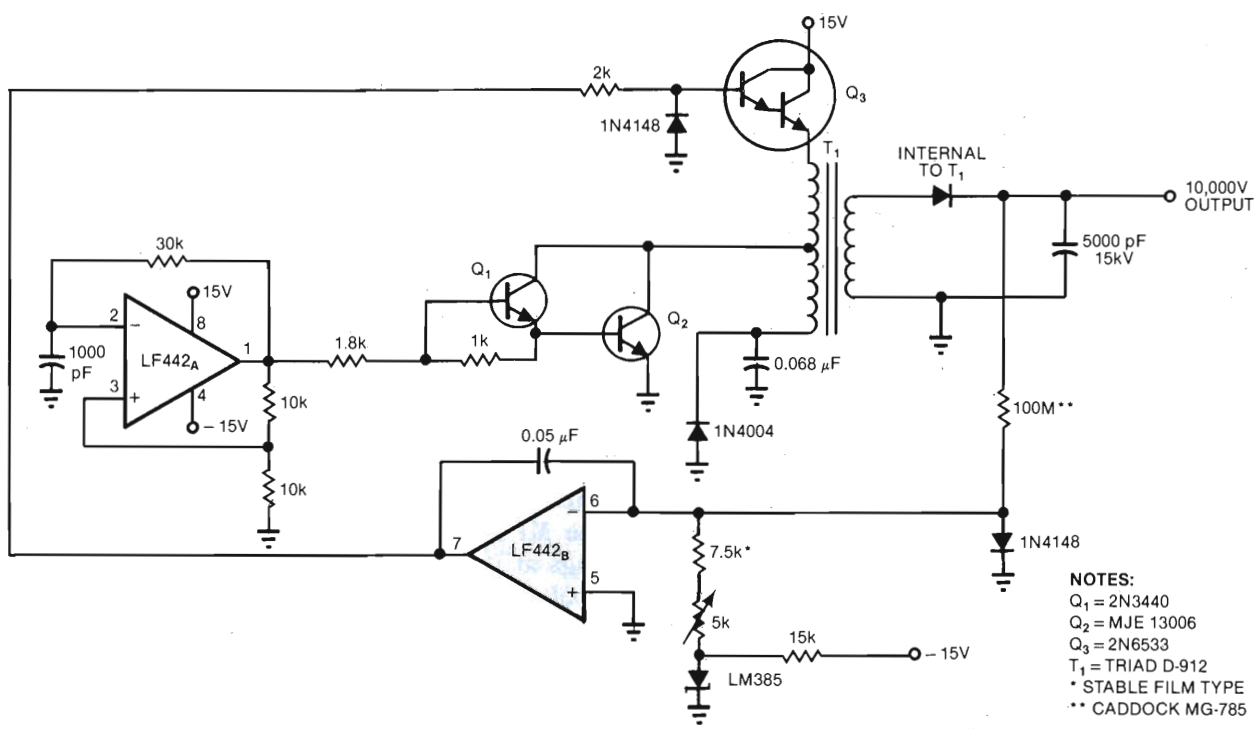


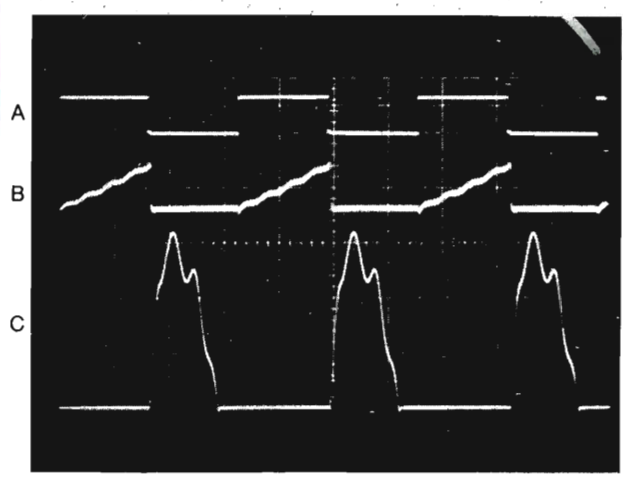
Fig 12—Accelerate electrons in a CRT *with this ±15V to 10-kV flyback-type converter; its servo loop ensures output stability.*

Meet lasers' special needs with a PWM IC

remains unclamped. When the 0.22-μF capacitor charges fully, $LM393_B$'s plus input exceeds 5V, and the SCR again drives T_2, producing the 8-kV start pulse. This action continues until the laser runs.

Don't write off vacuum tubes

Fig 10's laser supply achieves its 1300V output through servo control around a transformer. A potential problem with this type of converter is that its transient response is limited by the modulation frequency applied to the transformer. The best way to avoid the problem is to regulate with a series-pass



TRACE	VERTICAL	HORIZONTAL
A	50V/DIV	20 μSEC/DIV
B	4A/DIV	20 μSEC/DIV
C	50V/DIV	20 μSEC/DIV

Fig 13—Magnetic-field collapse *in* ***Fig 12****'s* T_1 *primary produces the high* Q_2 *collector-voltage pulses in trace C.*

element on the transformer's high-voltage side. But this action usually implies the use of expensive high-voltage transistors and a substantial amount of protective circuitry. **Fig 11** shows a converter that deals with these problems. It's inexpensive, provides the fast transient response of a series regulator and requires no output protection. Moreover, it withstands short circuits and output-current or -voltage reversals arising from reactive loads.

The self-exciting dc/dc converter composed of T_1, Q_1, Q_2 and their associated components generates the unregulated high voltage from a 28V supply. This converter's rectified and filtered output is applied to the plates of the two 1625 vacuum tubes, which are configured in a common-cathode-driven cathode-

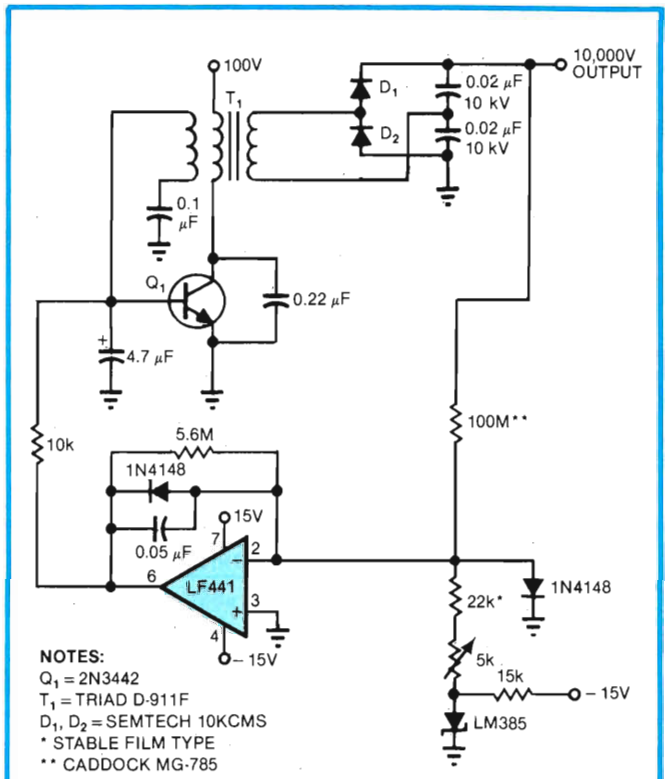


Fig 14—Using sinusoidal signals, *this converter supplies 10 kV with no radiated noise or spikiness.*

follower arrangement, with NE-2 neon-lamp screen-to-cathode clamps. Feedback from V_2 to the LF441 provides overall loop stabilization. The 390-pF/3.3-kΩ pair provides local rolloff at the LF441; overall compensation comes from the 10-pF/1-MΩ network. The 1N914 prevents capacitively coupled transients from appearing at the LF441's input.

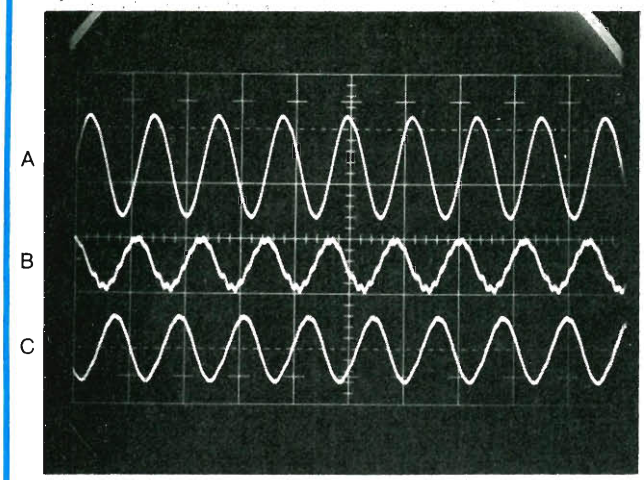
Set the output voltage with the 5-kΩ potentiometer at the LM329 reference. The power-handling capability of T_1 limits the circuit's output to 10W at 1000V—a chore that V_2 can perform effortlessly. If you anticipate extended (greater than 5 min) short circuits at the output, consider fusing V_2's plate circuit.

Multiply ±15V for voltage-hungry CRTs

In data-terminal designs, you must often convert the supply rails to the high voltage needed for CRT electron-beam acceleration. You can use a flyback approach for this task, but for more demanding applications (such as oscilloscopes), you might have to use a sine-wave conversion technique. So consider examples of conversion circuits that use each method.

In **Fig 12**'s flyback circuit, $LF442_A$ functions as an oscillator whose output (**Fig 13,** trace A) drives the Q_1-Q_2 Darlington pair. When the output is HIGH, Q_1 and Q_2 conduct and the current through T_1's primary

Use vacuum tubes for a low-cost high-voltage supply



TRACE	VERTICAL	HORIZONTAL
A	100V/DIV	50 μSEC/DIV
B	5A/DIV	50 μSEC/DIV
C	100 mV/DIV (AC COUPLED)	50 μSEC/DIV

Fig 15—The linear nature *of* ***Fig 14****'s converter is evident in this scope photo.*

builds up (**Fig 13,** trace B). When $LF442_A$ goes LOW, however, the field in T_1's primary collapses and a large flyback voltage appears at Q_2's collector (**Fig 13,** trace C). This field collapse also appears at T_1's secondary and produces a very-high-voltage output, which is rectified and filtered and fed back to $LF442_B$ via a divider. $LF442_B$'s output then servo-controls Q_3, which determines the amount of drive available to T_1. The 0.05-μF capacitor provides stable loop compensation; the LM385 and the 5-kΩ pot set the output voltage.

Although effective, this circuit produces unavoidable radiated noise and supply spiking—which some sensitive data terminals and oscilloscopes can't tolerate. **Fig 14**'s sine-wave-based high-voltage converter eliminates these problems.

When you apply power to this circuit, the LM385 reference pulls the LF441's minus input LOW, causing the LF441's output to rise. This action in turn causes Q_1's collector voltage to drop (**Fig 15,** trace A) and its collector current to rise (**Fig 15,** trace B). Concurrently, the 0.1-μF capacitor in T_1's feedback winding charges to a negative voltage. When the current in T_1 stops building, T_1's feedback winding pulls Q_1's base negative (**Fig 15,** trace C), cutting off Q_1 and causing its collector voltage to rise.

When the voltage on the 0.1-μF capacitor becomes positive, Q_1 starts to conduct, its collector voltage drops and the cycle repeats. The 0.22- and 4.7-μF capacitors provide stabilization, and the high-voltage output is current-summed with the LM385's negative reference current at the LF441 servo amplifier.

The LF441's output servo-controls the drive to Q_1,

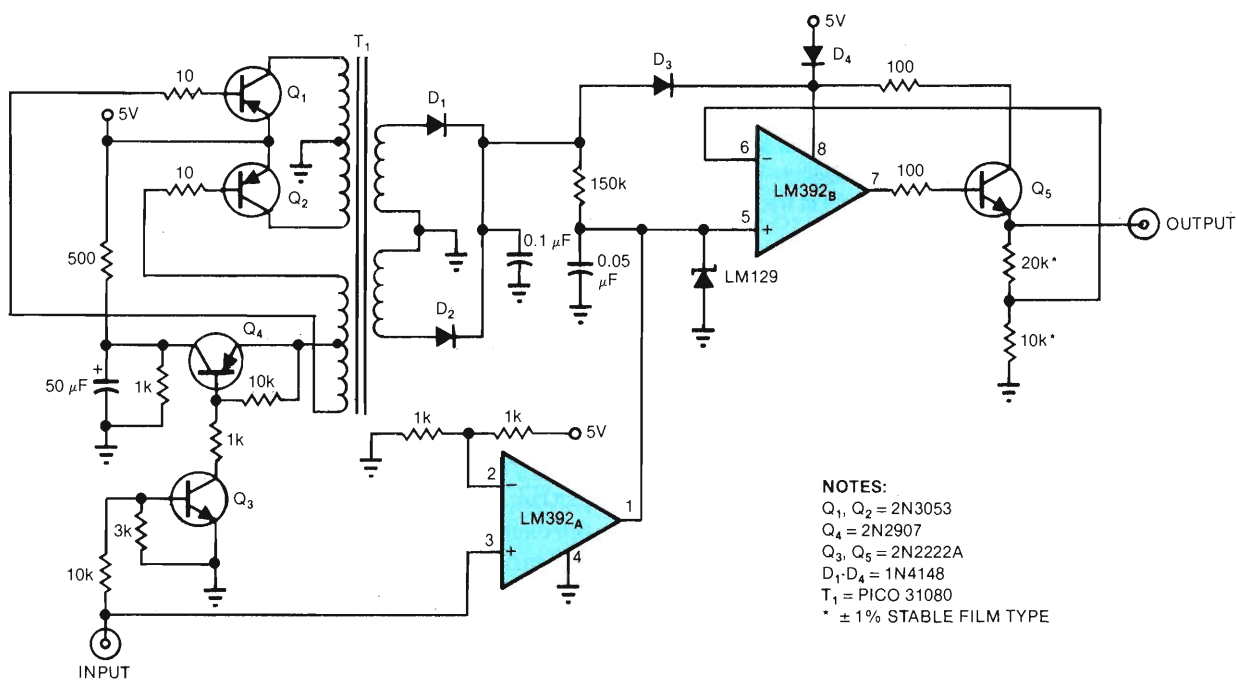


Fig 16—Memories are made of this—*a converter that supplies the 21V pulses for EEPROM programming. It achieves controlled rise time; you determine the pulse's width with a TTL command.*

closing the feedback loop around the transformer. Because the transformer isn't used in the flyback mode, the voltage step-up ratio is smaller than in **Fig 12**'s design, so you need higher initial input voltages. Alternatively, you could use a voltage-doubler network at the transformer output.

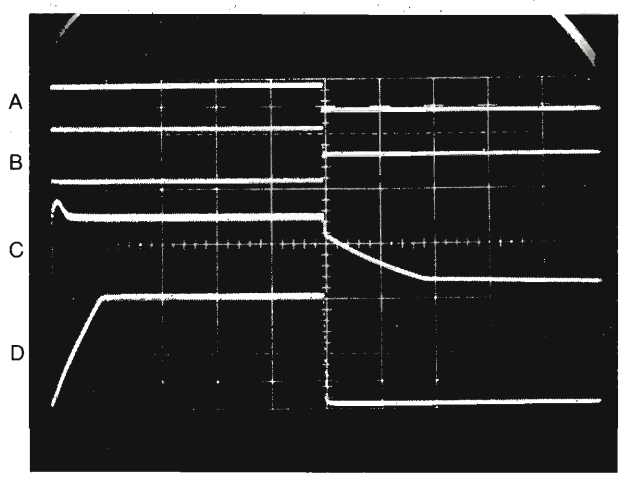
An easy way to power memory programming

What about the voltage required by programmable memories? Widely used EEPROM types such as the 2816 require controlled-rise-time 21V pulses for programming. **Fig 16** shows a converter that generates the necessary high-voltage pulses from the 5V rail.

T_1, in conjunction with Q_1 and Q_2, forms a self-driven 5 to 30V dc/dc converter. Q_3 and Q_4 serve as a strobe for this converter, allowing it to draw power and run only when a TTL signal is present at the circuit's input. When you apply a signal to the input (**Fig 17,** trace A), the Q_3-Q_4 pair conducts, biasing Q_1 and Q_2 so the converter runs (Q_2's collector waveform appears in **Fig 17,** trace B). The converter's output (**Fig 17,** trace C) is very lightly filtered by the 0.1-μF capacitor, allowing it to rise quickly. This output charges the 0.05-μF/150-kΩ combination.

The gain-of-3 $LM392_B$ amplifies the 0.05-μF capacitor voltage; Q_5 serves as an output-current booster. As the 0.05-μF capacitor charges, Q_5's emitter voltage rises, providing the leading edge of the programming pulse (**Fig 17,** trace D). When the capacitor voltage reaches 7V, the LM129 clamps, charging ceases and the output remains at 21V.

When you switch the TTL input pulse LOW, the $LM392_A$'s open-collector output clamps LOW, discharging the 0.05-μF capacitor and readying the circuit for the next pulse. You can satisfy any EEPROM's programming requirement by varying the gain of $LM392_B$, the time constant at its input or the zener clamp across the 0.05-μF capacitor. **EDN**



TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	2 mSEC/DIV
B	10V/DIV	2 mSEC/DIV
C	20V/DIV	2 mSEC/DIV
D	10V/DIV	2 mSEC/DIV

Fig 17—The programming pulse *of* ***Fig 16****'s circuit appears in trace D. Note the cleanly rising leading edge.*

Author's biography

Jim Williams, now a consultant, was applications manager in National Semiconductor's Linear Applications Group (Santa Clara, CA), specializing in analog-circuit and instrumentation development, when he wrote this article. Before joining the firm, he served as a consultant at Arthur D Little Inc and directed the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art and collecting antique scientific instruments in his spare time.

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Article Interest Quotient (Circle One)
High **476** ***Medium*** **477** ***Low*** **478**

Exploit D/A converters in unusual controller designs

More than just a data manipulator, a multiplying DAC simplifies designs such as scanner positioners, temperature regulators and electronic locks.

Jim Williams, National Semiconductor Corp

Employing multiplying digital-to-analog-converter (MDAC) ICs in other-than-standard data-handling tasks allows you to control many diverse—and difficult-to-interface—analog functions. MDACs such as the 12-bit DAC1218 and the 10-bit DAC1020 provide features that bring digital accuracy to familiar control chores involving temperature, voltage and vibration.

Digitally position mechanical scanners

Consider, for example, the use of these devices in the scanning-electrophoresis technique that biochemists employ to separate unidentified cells or molecular structures from each other. In one form of this process, a motor-driven scanner examines a sample suspended in a suitable liquid and contained within a glass or quartz tube approximately 1 ft long. A high voltage applied along the tube's length separates the cells according to their charge gradient, resulting in a series of bands within the tube where like cells collect. Photometrically scanning the tube's length, noting the bands' distances from a reference point and matching these locations against the potential's gradient, accomplishes cell identification.

The key to this technique lies in the scanning process:

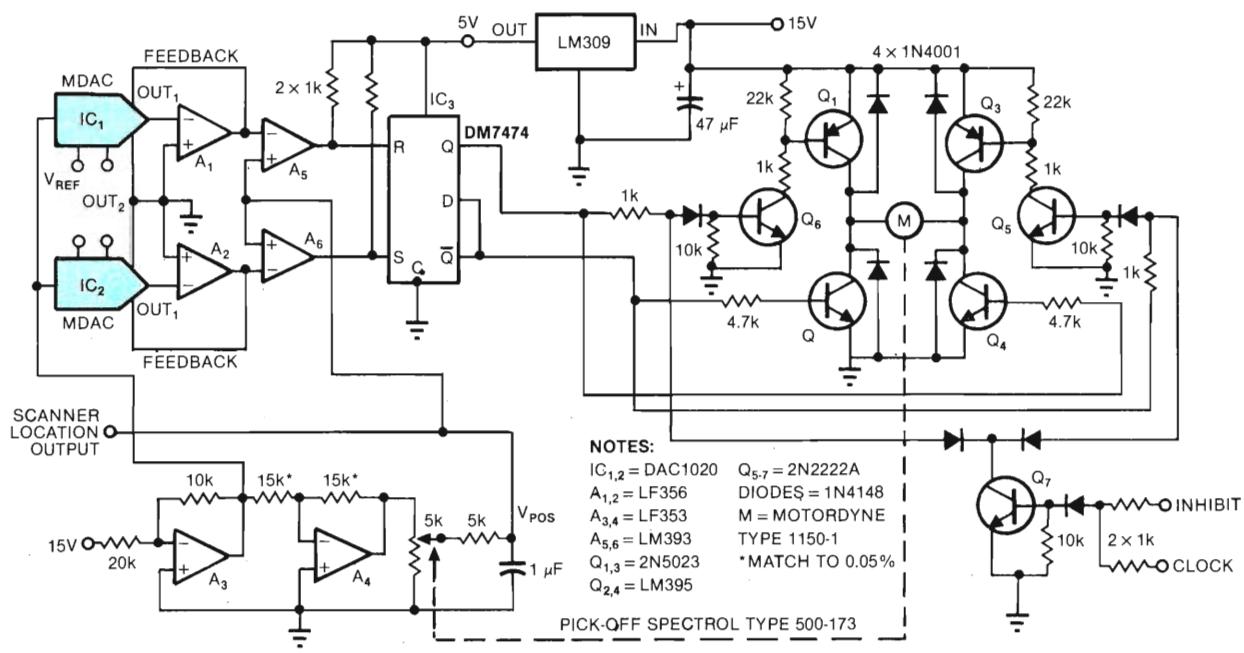


Fig 1—Digital words *determine a motor-driven scanner's excursion limits via a dual-MDAC-controlled transistor-bridge drive scheme. Two comparators (A_5, A_6) match a motor-position analog voltage (V_{POS}) with the MDAC's outputs and set or reset flip flop IC_3 accordingly. When the flip flop is set, for example, its Q output goes HIGH and turns transistors Q_1 and Q_4 on until V_{POS} is nulled.*

Digital-to-analog converters provide biochemical controls

Ideally, both the scanner's speed and the minimum and maximum scan length should be programmable. In Fig 1's approach, MDACs establish the scanner's travel limits via two sets of digital input codes. The scanner's motor drives a pick-off potentiometer, providing an analog voltage proportional to the scanner's position. This signal in turn feeds limit comparators A_5 and A_6, driving one of these device's outputs HIGH when either the high (A_5 and IC_1)- or low-position limit (A_6 and IC_2)

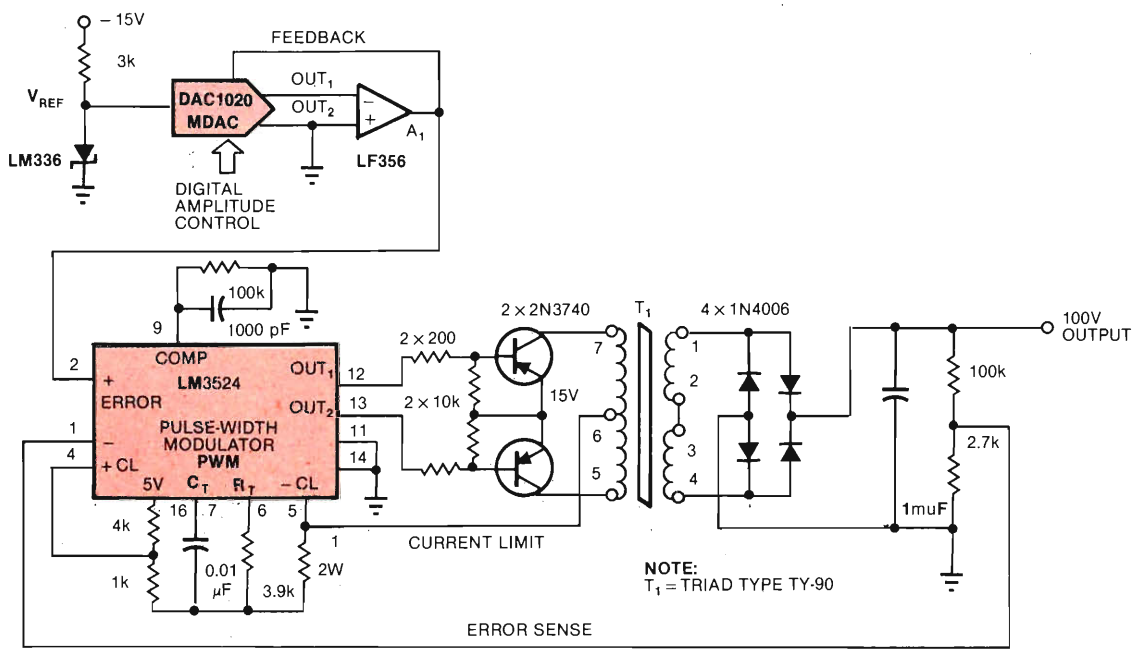


Fig 2—A settable output voltage *results when an MDAC controls a pulse-width modulator's input reference voltage. Overcurrent protection occurs when the voltage to the PWM's –CL input exceeds its +CL reference.*

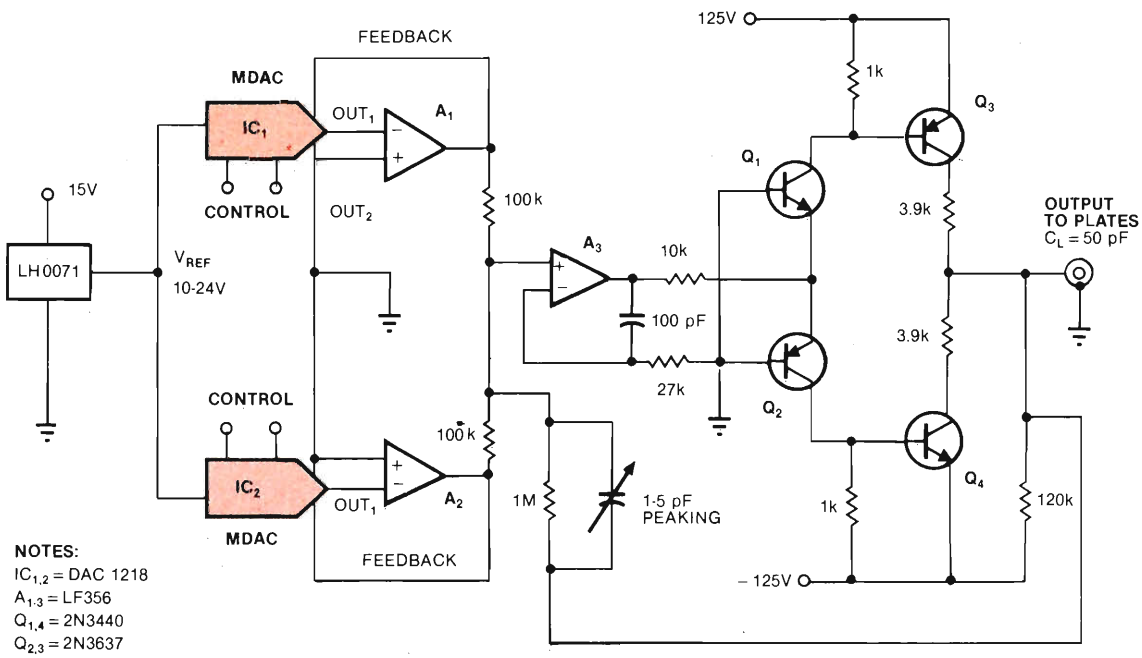
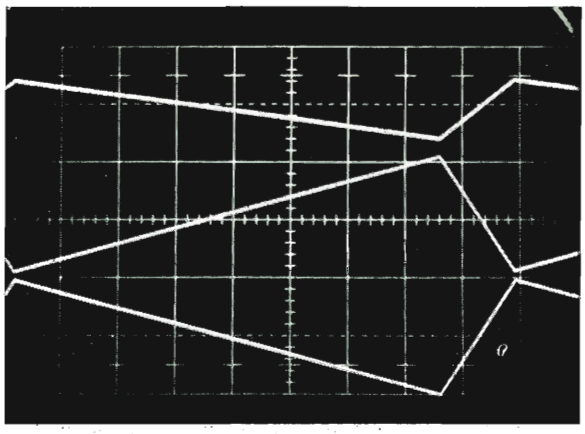


Fig 3—Dual MDACs *provide both dc and ac output voltages when driving a complementary transistor pair. A fixed digital code controls one MDAC to set the dc level; the other MDAC generates the ac component when its digital inputs are varied.*

is exceeded. (A_1 and A_2 serve as current-to-voltage converters, while A_3 and A_4 establish the feedback loop's reference voltages.)

When the scanner reaches a limit condition, these limit comparators set (S) or reset (R) flip flop IC_3; the resulting HIGH Q or $\overline{Q}$ output switches a transistor bridge on in a direction that reverses the motor's rotation. Thus, the scanner's motor bidirectionally runs the photometer head between the encoded scan limits.

Q_7 and its associated diodes control the motor's speed. When both Inhibit and Clock inputs are LOW, Q_7 is OFF and the flip flop's Q and $\overline{Q}$ signals can drive Q_5 and Q_6. However, if either Inhibit or Clock is HIGH, Q_7 turns on and shunts the drive signals to ground. You can employ a μC to generate all the scanner's control functions. For example, using a software-generated pulse-width-modulated signal as the clock allows you to dynamically alter the scanner's speed to run rapidly across distances where there aren't cell bands and slowly where there are. Similarly, you can use software to set the scan limits to home in on a cell-populated portion of the tube.



TRACE	VERTICAL	HORIZONTAL
TOP	10V/DIV	
MIDDLE	100V/DIV	50 μSEC/DIV
BOTTOM	100V/DIV	

Fig 4—An ac-driven MDAC *generates these CRT deflection voltages using the scheme shown in* ***Fig 3.*** *Buffer amplifier A_1's output (top) can be converted to a high-voltage complementary (middle) or in-phase equivalent (bottom) waveform.*

5V logic sets high-voltage levels

MDACs can control high-voltage sources as well as scanner positioners. Consider, for example, **Fig 2**'s circuit, which serves as a digitally controlled 15 to 100V supply suited to automatic-testing applications. This circuit couples a pulse-width-modulator (PWM)-driven push/pull voltage-converter stage with an MDAC in a feedback loop. The MDAC, in conjunction with A_1, establishes the PWM's setpoint voltage. The PWM in turn drives the transistors and—via the step-up transformer—converts the 15V to as much as 100V.

The transformer's square-wave output gets rectified, filtered and divided down by the resistor string. The resulting voltage level feeds back to the PWM's error amplifier, completing the control loop. You set the loop's gain and frequency characteristics with the 1000-pF/100-kΩ pair. Short-circuit protection results

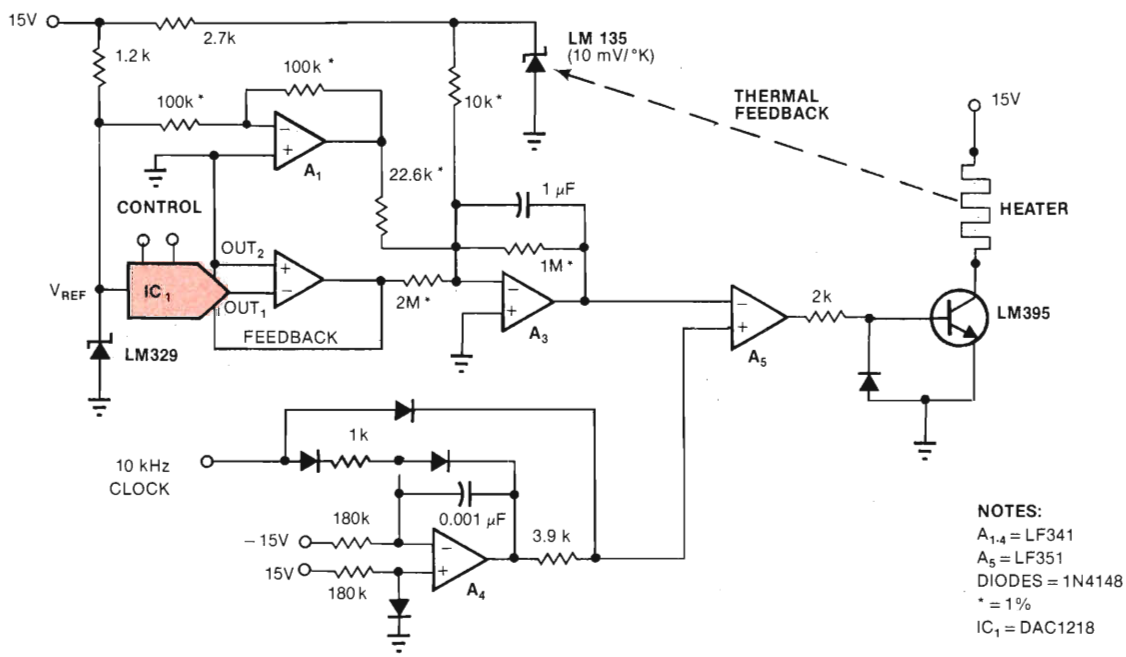


Fig 5—Precise temperature excursions *result when A_3 sums an MDAC-generated triangular waveform with A_1's fixed reference and the LM135's temperature-dependent signal. A_4 pulse-width-modulates the resulting error voltage and controls the heater's ON time.*

Set a shaker table's frequency with a D/A-converter IC

when the IR drop across the 1Ω resistor exceeds the 1V reference at the PWM's +CL input. (For a complete discussion of the PWM's functions, see EDN, September 2, pg 202.)

Although you can rapidly update the MDAC's output, the transformer's 20-kHz capability and the loop's time constants limit the design's bandwidth. In practice, though, you can modulate the MDAC's input at 250 Hz and still deliver a 100V sine wave into a 1-kΩ load.

Digitally modulate your CRT's plates

Another high-voltage requirement centers on modulating a CRT's deflection plates in electron-optics applications. In contrast to the previous high-voltage circuit, this design operates at greater bandwidths but has a low current-delivering capability. (Actually, this low-current limitation is not significant because the CRT's plates act like a very large resistor shunted by 50 pF.)

Fig 3's scheme uses two MDAC/op-amp pairs to generate the CRT's signals: One MDAC establishes the static (dc) bias; the second provides the dynamic (ac) drive signal (typically a ramp). A_3 sums these signals and feeds the result to the high-voltage stage, consisting of Q_1 through Q_4. This stage acts as an inverting, complementary, common-base-driven common-emitter amplifier with gain. And because the output-current requirements are low, you can avoid the usual crossover-distortion problems without complex compensation circuitry; merely tie the stage's output to the −125V rail via a 120-kΩ resistor. Closing the feedback loop with a 1-MΩ resistor yields the quick, clean response shown in **Fig 4.** (In this figure, two complete MDAC-driven amplifiers were used to produce the traces.) The top trace shows the ac signal created by digitally modulating IC_1's inputs; the middle and bottom traces depict the resulting high-voltage outputs.

MDACs regulate temperatures

MDACs also serve in temperature-regulating applications—such as those involving critical biochemical reactions occurring only within or at the edges of very specific (and often very narrow) temperature limits. **Fig 5**'s circuit, for example, employs an MDAC to regulate a heater and overcome the inability of standard temperature-control methods to provide both fine-grain resolution and long-term stability.

The basic temperature-control loop comprises an MDAC-controlled PWM (A_1 through A_5). Thermal feedback to the LM135 closes the loop; it varies the PWM's duty cycle to establish the controller's setpoint. Note that the PWM action results from A_5's comparing A_3's setpoint-equivalent output with the ramp output generated by the clock-driven integrator, A_4. A_3's output is in turn a function of the setpoint current flowing through the 22.6-kΩ resistor as well as the LM135's signal. (Amplifier A_3's 10-MΩ/1-μF feedback values limit the loop's response to 0.1 Hz.)

You control the temperature's excursions around the setpoint by modulating the MDAC's digital inputs with a slowly varying digitally encoded triangular waveform; the number of bits changed controls the temperature's span. **Fig 6**'s strip-chart recording demonstrates this design's advantages: Temperature can vary by ±1.5°C around a 37.5°C setpoint for many hours.

MDACs develop high-power audio signals

Now consider an MDAC's use in an audio-frequency application—control of the shaker tables frequently employed to test finished assemblies for vibration-induced failures. In order for these tests to be

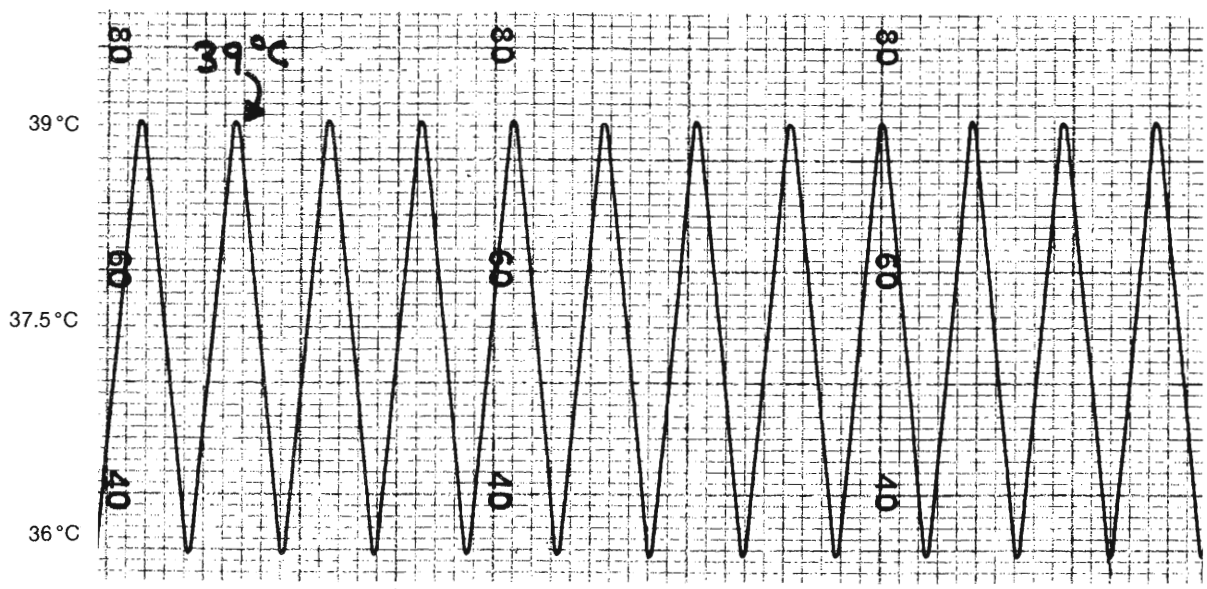


Fig 6—Long-term temperature control *is the result when* **Fig 5***'s design modulates the 37.5°C baseline setting via a triangular-wave-driven MDAC. The MDAC's digital input code controls the peak-to-peak oscillation amplitude.*

meaningful, the vibration patterns must be tightly controlled in terms of duration, frequency and amplitude. **Fig 7**'s dual-MDAC scheme can meet these requirements.

Frequency control results when MDAC IC_1 drives the integrator formed by A_1. This stage's output ramps until its 10-kΩ derived current just balances the feedback current at comparator A_2's + input. At this point, A_2's output changes state and forces the zener-diode network to furnish an equal-magnitude but opposite-polarity reference voltage. Because this now-inverted reference feeds both the MDAC and the comparator, the integrator generates a triangular waveform symmetrically centered on ground. Using this circuit technique, you can use 12 bits to encode the MDAC and synthesize a 1-Hz to 30-kHz output signal.

A sine wave results when the synthesized triangular signal feeds the dual npn/pnp stage; the logarithmic relationship between the LM394's collector current and its V_{BE} performs the smoothing function. You adjust the offset and wave-shape pots for low distortion.

The digital amplitude-control feature occurs in the

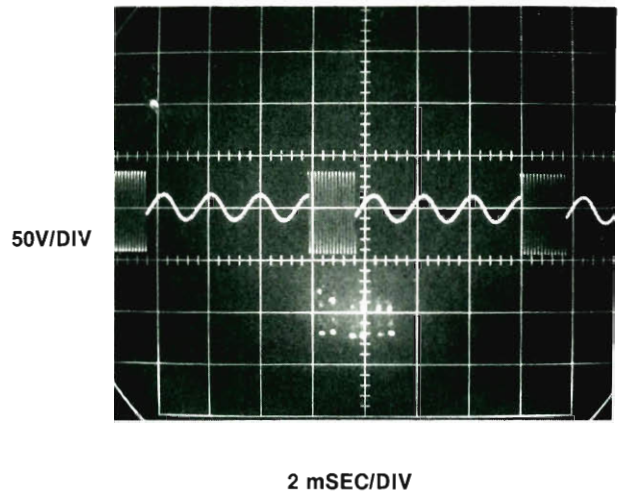


Fig 8—A signal's frequency or amplitude *is quickly changed by* ***Fig 7****'s MDAC controllers. Using this technique, you can vary output frequency from 1 Hz to 30 kHz.*

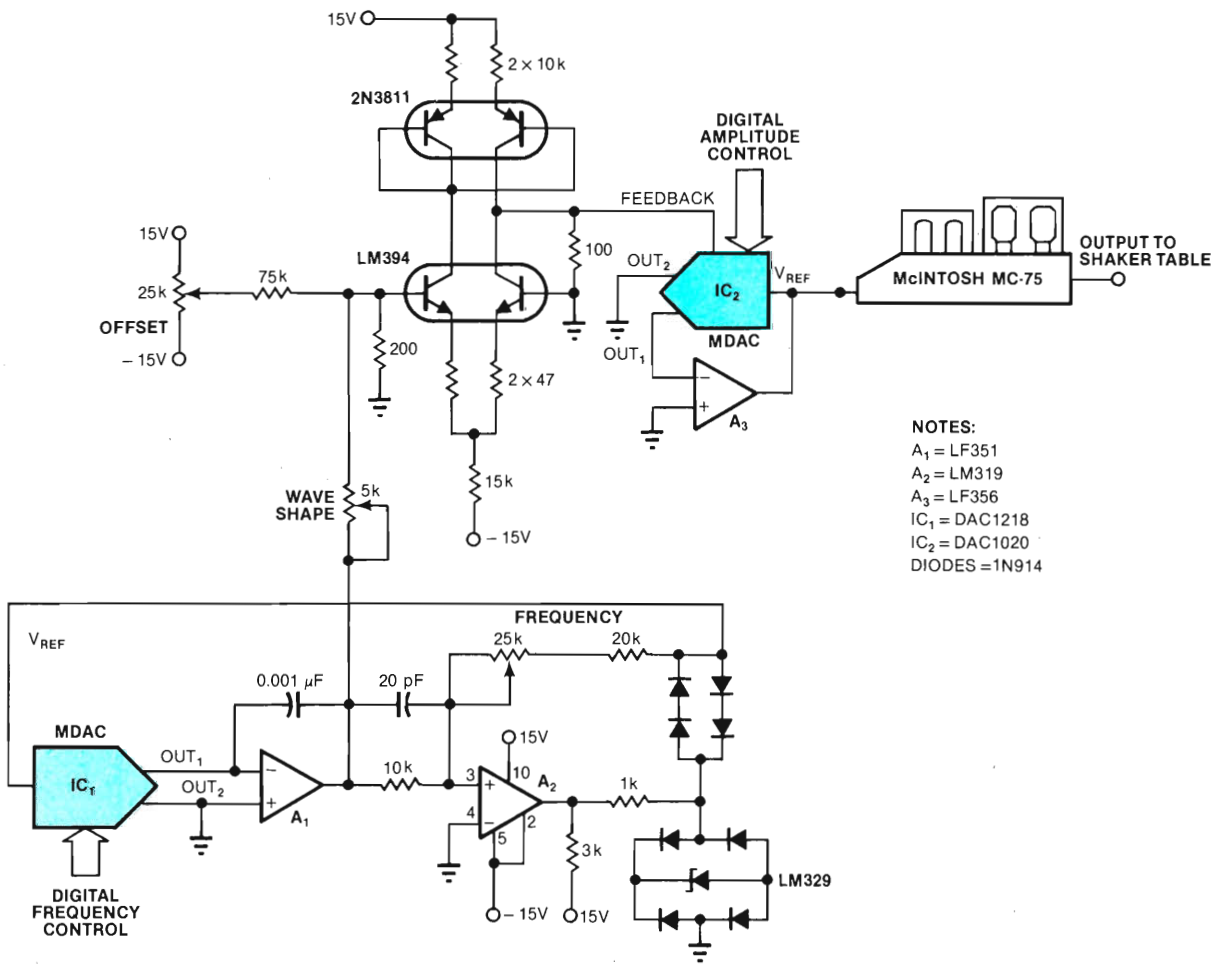


Fig 7—Digitally variable frequency and amplitude signals *arise when the triangular wave generated by* IC_1 *through* A_2 *is converted to a sine wave by the pnp/npn stage and modulated by MDAC* IC_2*. Both the frequency and amplitude functions can be fixed (via switches) or swept.*

Pick-proof electronic locks by digitally reading the key

associated MDAC/op-amp network. Here the MDAC (IC_2) operates as the programmable gain element in the op amp's feedback loop. This trick provides a millivolts-to-volts range at A_3's output pin.

Because a shaker table's input impedance is resistively low and inductively high, a vacuum-tube amplifier is your best choice for the power stage; its transformer-isolated output is immune to the table's inductively induced flyback spikes. **Fig 8** shows this design's output waveform when both MDACs are simultaneously updated. Note its clean and essentially instantaneous response to both frequency and amplitude steps.

Digital codes "pick-proof" a lock

Fig 9's circuit serves an unusual MDAC application: the programming of an electronically keyed combination lock. Because the inserted key is an 0.01% resistor, security is assured against all but the most determined and sophisticated thieves. If the key you insert isn't the correct one, the circuit knows it within 250 msec and ignores any further lock-opening attempts for 5 min. Decade-box- or potentiometer-equipped thieves thus don't have a chance.

When "key resistor" R_K has the correct value, the MDAC's output current precisely balances R_K's current at A_1's input and drives A_1's output to zero. The absolute-value stages (A_2 and A_3) sense this condition, and A_3's output, Q_1's emitter and A_4's + input also go to zero. And when A_4's input reaches zero, its output goes negative, Q_3 cuts off and C_1 starts charging toward the 15V supply level via the 22-kΩ/diode network. During this 250-msec charging time, A_5's HIGH output level turns the Q_1/Q_2 stage on and therefore opens the door's lock. When C_1 charges past 5V, A_5's output goes LOW and disables the lock again.

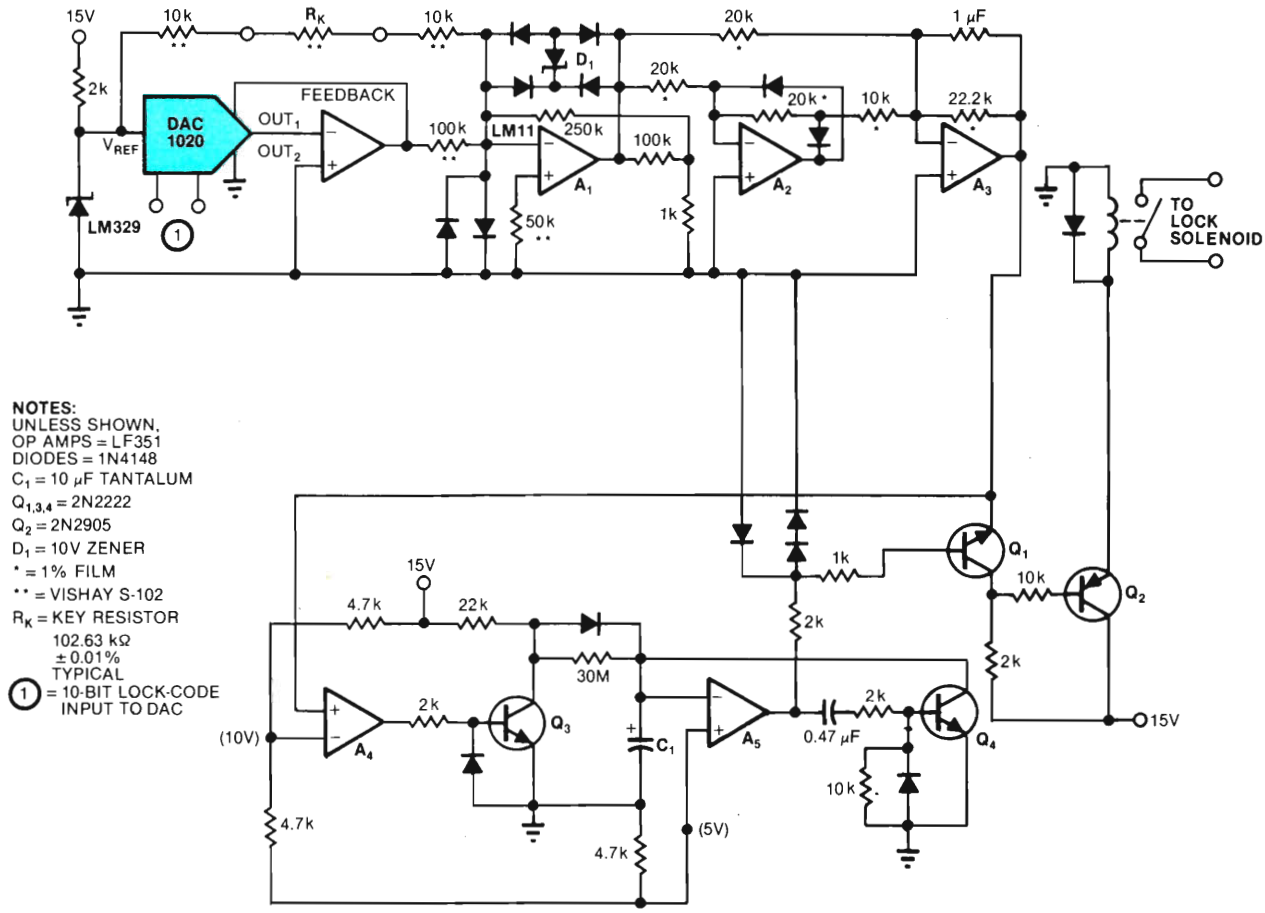


Fig 9—A virtually pick-proof electronic lock *employs an MDAC in a digital-code-to-resistor-value comparison loop. Resistor R_K serves as a key. When the inserted resistor's value isn't correct and accepted within 250 msec, the circuit inhibits another lock-opening attempt for 5 min.*

Pick-proof lock frustrates sophisticated thieves

If you try opening the lock with an illegal R_K, the absolute-value stages (A_2, A_3) don't settle to zero and Q_1 remains OFF. Under these conditions, it takes 5 min before C_1 discharges back down to 5V—via the 30-MΩ resistor—and is reset to 0V by Q_4.

This design discourages even the most sophisticated and/or frustrated thieves: Amplifier A_1's zener-diode bridge and input clamps prevent anyone from monitoring the summing junction's requirements or intentionally destroying the unit. And the 12-bit MDAC provides security via 4096 possible combinations. **EDN**

Author's biography

Jim Williams, applications manager with National Semiconductor's Linear Applications Group (Santa Clara, CA), specializes in analog-circuit and instrumentation development. Before joining the firm, he served as a consultant at Arthur D Little Inc and directed the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art and collecting antique scientific instruments in his spare time.

Use off-the-shelf linear ICs for sophisticated audio designs

With a little creativity and a good understanding of common linear circuits, you can produce high-performance audio designs—such as V/F converters, VCAs, preamps and panning circuits—with simple, inexpensive parts.

Jim Williams, National Semiconductor Corp

Op amps can serve in applications other than audio amplifiers; you can apply them and other off-the-shelf linear ICs to create more sophisticated audio and electronic-music circuits. And although these applications present stringent performance demands, don't assume you'll need excessively complicated and expensive designs; the linear circuits described here achieve high performance at low cost.

As an example of the unusual use of conventional components, consider **Fig 1**'s exponential V/F converter. Suitable for use in music synthesizers, this circuit provides an output that changes its frequency one octave in response to a 1V control-input variation. Similar to conventional nonlinear converters, it exploits

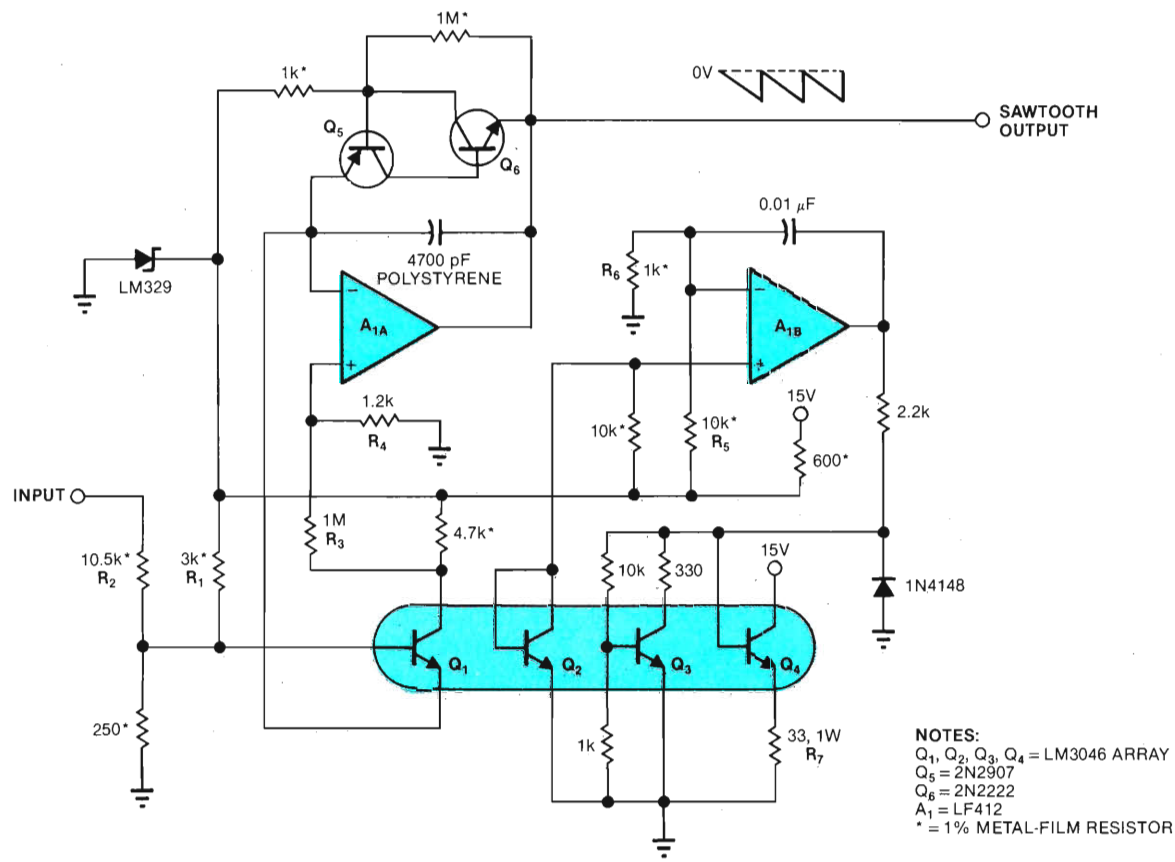


Fig 1—A temperature-compensated transistor array *stabilizes this exponential voltage-to-frequency converter. Q_2 senses the array's temperature and A_{1B} drives chip heater Q_4, maintaining a stable operating environment for logarithmic converter Q_1. The circuit's negative-going sawtooth output results from A_1's integration of Q_1's collector current until it reaches Q_5 and Q_6's threshold.*

A servo loop eliminates temperature-dependent drift

the logarithmic relationship between a transistor's base-emitter voltage and collector current. However, a unique thermal servo loop eliminates temperature-dependent transfer-function errors.

Generating the circuit's negative-going sawtooth output, op amp A_{1A} integrates Q_1's collector current until Q_5 and Q_6 turn on. These feedback transistors then discharge the integrating capacitor, the output rises to 0V and the cycle repeats.

Q_1 is a vital element in this circuit because its V_{BE}/I_C characteristics ensure that A_{1A}'s input current—and thus the output frequency—remain an exponential function of the control voltage. Assisting Q_1, transistors Q_2, Q_3, Q_4 and op amp A_{1B} form a temperature-controlled loop that stabilizes Q_1's operating point by thermally compensating the LM3046 transistor array.

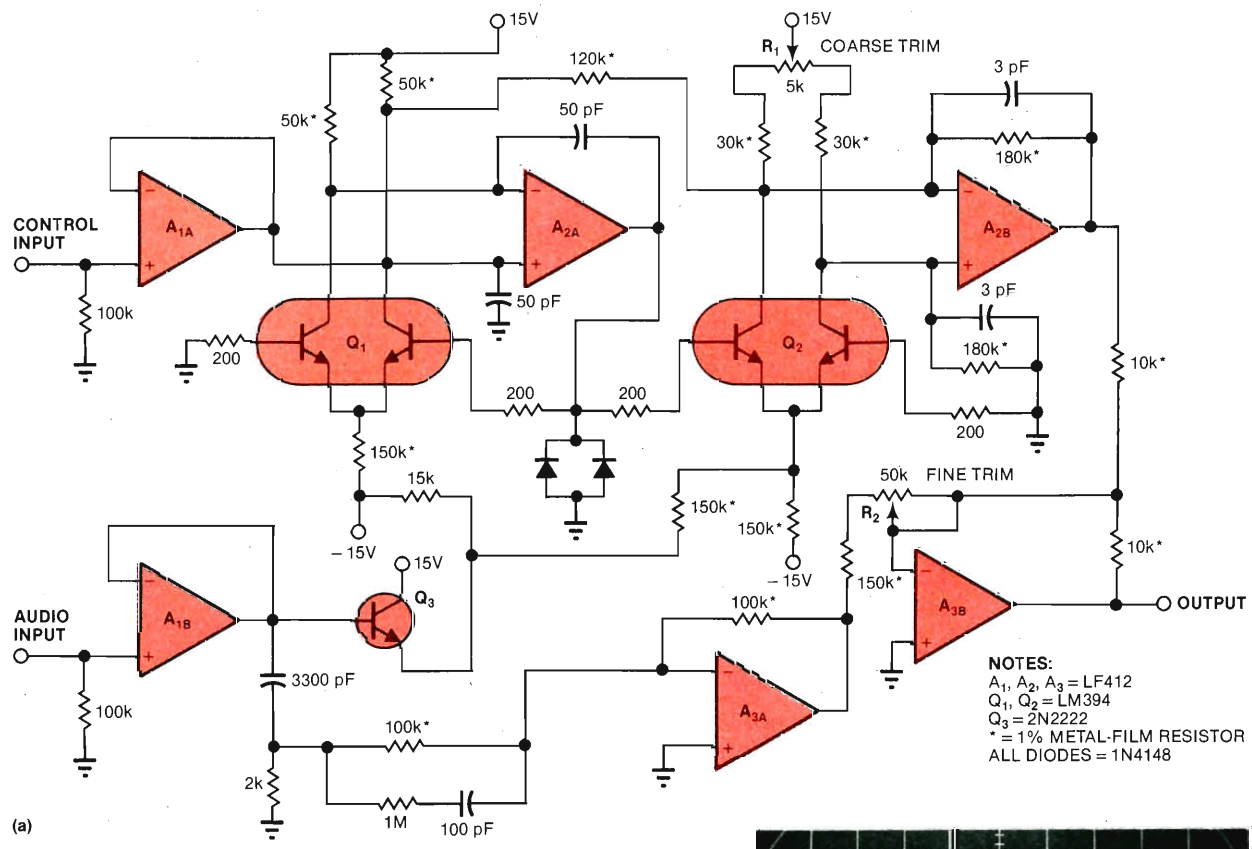
To perform this compensation, Q_2's base-emitter junction senses array temperature, and Q_4 heats the chip. A_{1B} varies this heater transistor's dissipation until Q_2's V_{BE} drop equals the reference level set by R_5 and R_6. Furthermore, Q_3 and R_7 limit Q_4's maximum operating power and ensure proper servo functioning during circuit power-up.

In addition to stabilizing Q_1's collector bias, the LM329 6.9V reference also fixes the Q_5/Q_6 firing point. These two transistors exhibit opposing temperature coefficients, so their switching threshold is compensated to approximately 100 ppm/°C. The polystyrene integrating capacitor's −120-ppm/°C TC cancels remaining firing-level uncertainty.

To establish a 20-Hz quiescent output frequency, R_1 biases the circuit's input. R_2 trims the converter's transfer gain. Op-amp input resistors R_3 and R_4 maintain exponential conformity to within 0.5% from 20 Hz to 15 kHz by providing first-order compensation for Q_1's bulk emitter resistance.

Reduce VCA feedthrough

The next circuit, a voltage-controlled amplifier (VCA), also uses a simple error-correction scheme to improve its performance (**Fig 2**). Commonly employed



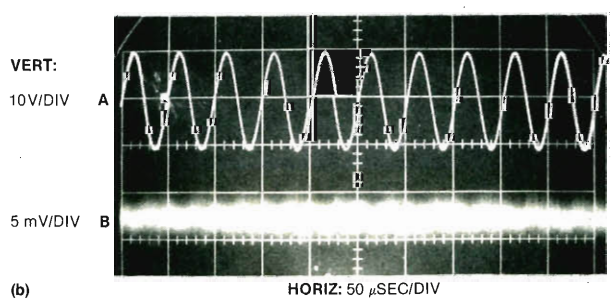


Fig 2—A voltage-controlled amplifier (a) *permits very little signal feedthrough when a nulling circuit cancels its residual output. The RC network at A_{3A}'s input provides the cancellation circuit with the same phase-shift and frequency-response characteristics as the multiplier, and R_2 affords fine feedthrough adjustment. Part* ***(b)*** *shows that 20-kHz multiplier feedthrough (trace* ***B****) is buried in the noise floor. When properly nulled, this circuit exhibits 84-dB min signal suppression referred to the input (trace* ***A****).*

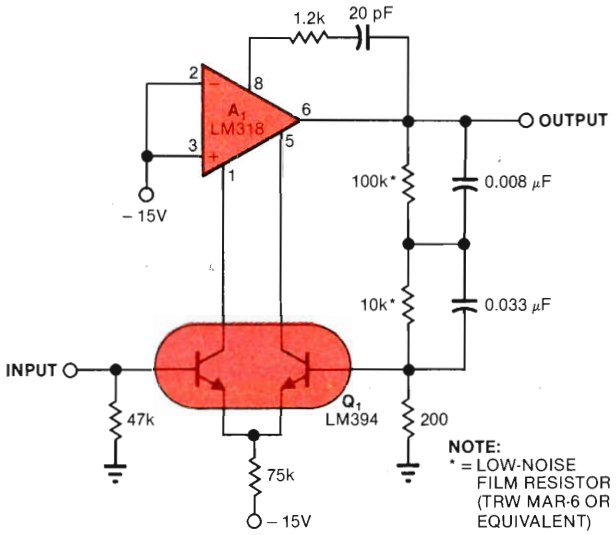


Fig 3—Lower input noise *results when an external transistor pair replaces the first stage of an op amp. This design avoids the loop-instability problems often caused by adding external stages to an op amp because the additional transistors replace rather than complement the LM318's input devices.*

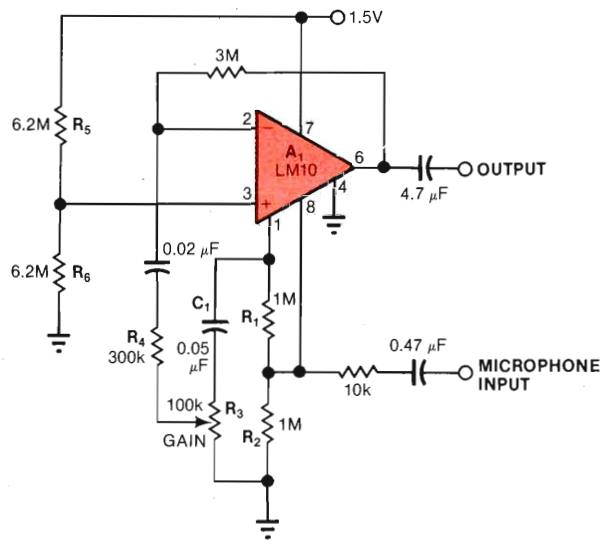


Fig 4—This microphone preamp *operates from supplies as low as 1.5V. Its LM10 reference amplifier provides a voltage gain of 100 with an input noise level of less than 50 nV/√Hz. The chip's op-amp section amplifies the reference output by an additional 20 dB.*

in recording-studio mixing consoles, VCAs must permit minimal signal feedthrough when their control inputs reach 0V. Conventional analog multipliers aren't optimal for this application; although they behave well in high-gain regions, they afford inadequate high-frequency signal suppression with their control channels off.

To reduce the feedthrough levels of its simple VCA, **Fig 2a**'s design uses a nulling technique. Op amps A_{1A} and A_{1B} and emitter-follower Q_3 buffer the circuit's control and audio inputs and then feed these signals to a transconductance multiplier composed of A_{2A}, Q_1 and Q_2. A_{2B} converts Q_2's differential collector currents to a single-ended audio output. R_1 allows coarse feedthrough trimming at 10 kHz to approximately −65 dB (relative to the input signal level).

To further reduce feedthrough, A_{3A} and A_{3B} null the multiplier's OFF-state output with the audio input. The RC network at inverter A_{3A}'s input provides phase shift and frequency response similar to the multiplier's feedthrough characteristics—thus, residual signals cancel out when A_{3B} combines the outputs from A_{3A} and A_{2B}. The nulling circuit's gain control, R_2, allows fine feedthrough trimming to −84 dB at 20 kHz.

To adjust this VCA, apply a 20V p-p, 20-kHz sine wave to the audio input, and with the control input grounded, adjust R_1 for minimum output from A_{2B}. Then trim R_2 for the lowest level at A_6's output. **Fig 2b** illustrates the circuit's typical feedthrough signal (trace **B**) for a 20-kHz input (trace **A**) when properly trimmed. Note that circuit noise almost obscures the waveform.

In addition to its excellent feedthrough suppression, this VCA exhibits only 0.05% total harmonic distortion (THD) throughout its 60-kHz power bandwidth. To obtain best circuit performance, construct it on a rigid circuit board, enclose it in a well-shielded box and employ proper grounding and noise reduction.

Replace an op amp's inputs

Instead of correcting a circuit's inherent errors as in the previous designs, you can use your knowledge of an IC's internal workings to eliminate deficiencies before they occur. For example, **Fig 3** illustrates an RIAA-equalized phono preamp with a noise figure less than 2 dB typ; it uses an LM394 ultralow-noise transistor pair at an LM318's compensation inputs instead of the device's internal input transistors.

This technique achieves lower noise than the unaltered op amp without introducing loop instability. Stability criteria become especially critical in RIAA circuits because the equalization function requires 100% feedback at high frequencies. Connecting the op amp's unused inputs to the negative supply shuts off the device's first differential pair and allows the external devices to operate into the LM318's output stages.

The distortion performance of **Fig 3**'s circuit exceeds the measurement capability of most test equipment: THD within the audio band remains less than 0.002% for outputs to 0.1V rms, and 20-kHz distortion rises only to 0.007% at 5V rms. Referred to a 10-mV input, the preamp's noise level equals −90 dB, with absolute values measuring 0.55 μV and 70 pA rms over a 20-kHz bandwidth—levels below the noise generated by most phono cartridges.

Fig 3's phono preamp also performs well in transient-intermodulation (TIM) tests. When fed with a 200-mV input—consisting of 10- and 11-kHz sine waves equally mixed—the circuit generates a 1-kHz output of only 80 μV. The TIM level, therefore, is 0.004% (or 0.0008% if you include the RIAA function's 14-dB (5:1) 10- to

An external transistor pair improves op-amp performance

1-kHz gain ratio). The preamp avoids overload-recovery problems by using only dc interstage coupling, and it generates an offset of 1V max when used with cartridges having 1-kΩ dc resistance.

Cascade two stages for high performance

The next example is also a preamp, but this time for a microphone. **Fig 4**'s preamp operates from one 1.5V battery and fits into a microphone casing.

The design uses an LM10 amplifier/reference IC, with modest voltage requirements that suit it well for such applications. The chip, however, has limited frequency response when used conventionally. **Fig 4**'s circuit extends the device's operating range by cascading its reference amplifier and op amp to form a high-gain preamp.

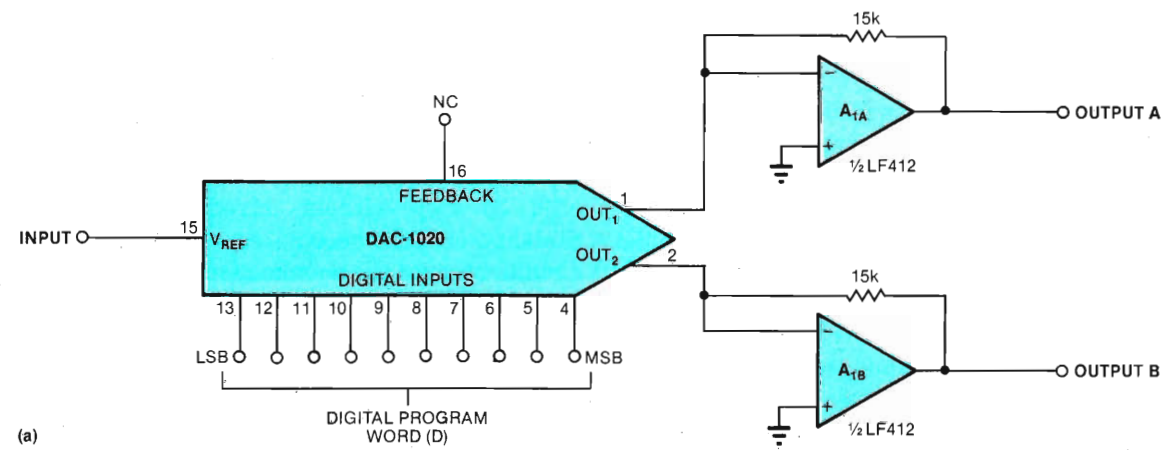
Here are the details. The microphone input drives A_1's reference amplifier, which has a unity-gain bandwidth of 500 kHz. Feedback around this stage yields an ac voltage gain of 100. The op amp, which operates more slowly than the reference amp, provides an additional 20 dB of voltage amplification, resulting in overall circuit gain of 60 dB. The preamp's bandwidth extends to 10 kHz unloaded and reaches 5 kHz with a 500Ω load.

Although using a reference amplifier as a low-level gain stage might introduce excessive noise, the LM10's reference voltage is so low that the circuit's input noise typically remains less than 50 $nV/\sqrt{Hz}$. The bias voltage generated by A_1's reference circuitry creates an offset at the reference amp's output and limits the maximum value of feedback resistor R_1. R_2 controls the amp's dc gain, thus optimizing the output offset level. Finally, the reference amp's bias characteristics introduce some minor problems: They restrict the first stage's voltage swing to between 150 mV and a V_{CC} of −800 mV (700 mV for a 1.5V supply) and cause the circuit's quiescent output to become uncertain.

To increase circuit life, C_1 couples the gain control (R_3) to the reference amplifier's output and ensures that no dc flows through the control's wiper. If this feature is unnecessary, you can reduce component count by connecting R_4 directly to the reference amplifier's output (A_1, pin 1) and using R_1 as a gain control. However, the 70-nA bias current that normally flows through the feedback resistor might increase noise.

DAC pans audio signal

Another approach to solving audio-design problems involves multiplying DACs. **Fig 5** shows a digitally programmable panning circuit that splits an input between two output channels. The DAC input code (D) determines the relative levels of the two channels, and op amps A_{1A} and A_{1B} convert the DAC's complementary current outputs into voltages. The relationship of the



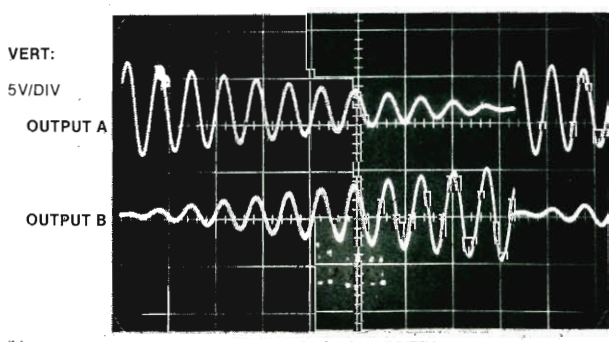


Fig 5—A DAC controls the ratio of two output signals *in the pan-pot circuit shown in* ***(a).*** *Op amps A_{1A} and A_{1B} convert the DAC's complementary output currents to voltage signals. The ratio of the pan pot's outputs* ***(b)*** *changes as a digital ramp drives the DAC input. The sum of the two signals remains constant, regardless of the digital control word.*

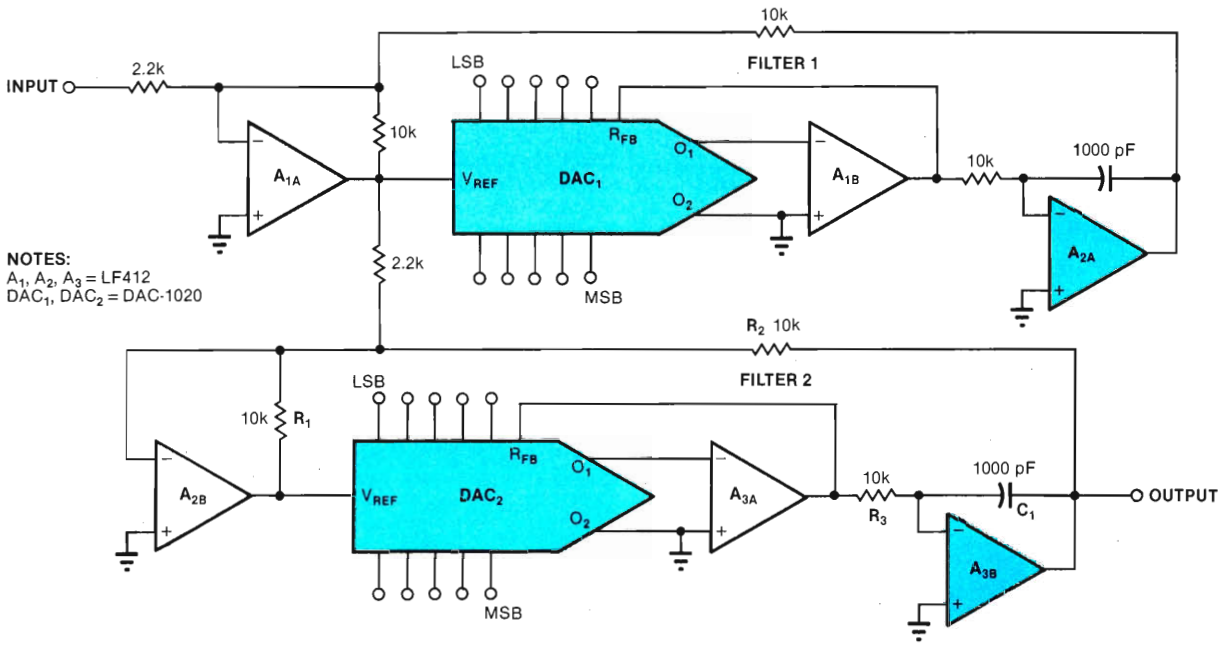


Fig 6—Two DACs control the passband *of this first-order filter. The input codes determine the gains of integrators A_{2A} and A_{3B}.*

two output signals to the digital input in **Fig 5**'s design is given by:

$$\text{OUTPUT A} = -\left[\text{INPUT} \times \left(\frac{3D}{2048}\right)\right],$$

$$\text{OUTPUT B} = -\left[\text{INPUT} \times \frac{3(1024 - D)}{2048}\right]$$

and **Fig 5b** illustrates the circuit's operation when a digital ramp controls the DAC inputs.

This circuit differs from conventional DAC applications because the converter's internal feedback resistor remains unconnected; the circuit's discrete resistors permit better matching of the output channels. Each op amp exhibits 300-ppm/°C gain drift arising from mismatches between the DAC's ladder resistors and op-amp feedback elements. You can eliminate these small errors, though, by using a separate DAC, with complementary digital inputs, for each channel.

You can also employ DACs in programmable-audio-filter designs. **Fig 6**'s circuit, a first-order bandpass network, utilizes two identical state-variable filters. The DACs control the gains of integrators A_{2A} and A_{3B} and thus determine the filters' cutoff frequencies.

You achieve a bandpass characteristic by connecting the first filter's high-pass output (taken from the output of A_{1A}) to the second filter's input. Filter 2's low-pass output then contains only those signals that lie within the passband established by the DACs' input codes.

You can determine filter 2's low-pass cutoff frequency (f_C) as a function of DAC_2's program input (D) with

$$f_C = \frac{R_1}{R_2}\left[\frac{D}{2048\pi R_3 C_1}\right].$$

For **Fig 6**'s components,

$$f_C = \frac{D}{2048\pi(10k)(1 \times 10^{-9})}.$$

Filter 1's high-pass output function equals the derivative of the low-pass expression (**reference**). EDN

Reference

Analog Devices Inc, *Application Guide to CMOS Multiplying D/A Converters*, 1978, pg 32.

Author's biography

Jim Williams, applications manager of National Semiconductor's Linear Applications Group (Santa Clara, CA), specializes in instrument development and analog circuit design. Before joining National, he served as a consultant at Arthur D Little Inc and ran the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim lists spare-time interests that include tennis, art and collecting antique scientific instruments.

Article Interest Quotient (Circle One)
***High* 473 *Medium* 474 *Low* 475**

Expand linear circuit functions with nonlinear design schemes

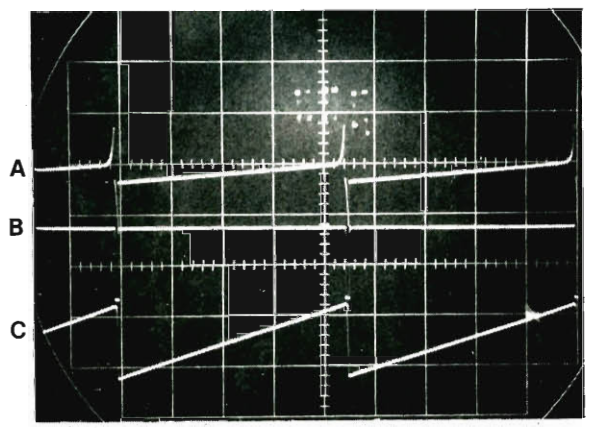
Circuits implementing logarithmic or exponential functions provide instrumentation and control designs with many features unobtainable using linear-only characteristics. Such circuits can gauge fuel level or a grape's ripeness.

Jim Williams, National Semiconductor Corp

Just because a control or instrumentation design requires a logarithmic or exponential transfer function, don't assume that it must be complex, troublesome and expensive. It needn't be if you employ the correct basic circuit (see **box,** "Straightforward nonlinear circuits"). Indeed, the same concepts apply whether you must measure a tank's contents or control a motor's speed.

Govern a pump's rate

Although peristaltic pumps are generally driven by a continuously rotating motor, this technique isn't suitable when your application requires precise delivery at low rates as well as a high-throughput capability. (This situation often occurs in chemical or biological process-



TRACE	V/DIV
A	5
B	20
C	20

(b) HORIZONTAL SWEEP = 200 μSEC/DIV

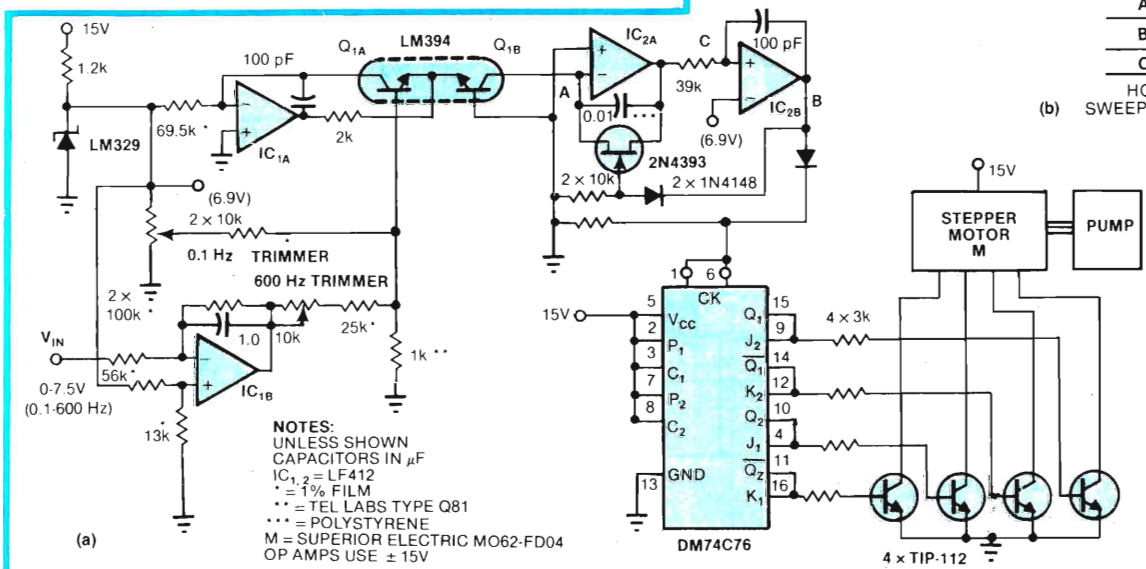


Fig 1—A stepper motor's speed varies exponentially *when driven by this voltage-to-4-phase converter. Using this approach, you can precisely govern a peristaltic pump's output flow for tight process control at low rates, yet speed it up for high throughputs. The waveforms correspond to points indicated on the schematic.*

Exponential expansion provides an 8-octave audio sweep signal

Straightforward nonlinear circuits

The theory and construction of logarithmic and exponential circuits isn't difficult, just different from what linear circuits require. By applying a few basic concepts, you can adapt the **figure**'s logarithmic **(a)** and exponential **(b)** schemes to a wide range of applications.

Capable of transforming a linear input voltage or current to a logarithmically equivalent output voltage, the design in **(a)** exhibits a 1% current-to-voltage conformity over a range of nearly six decades. This design, like most log circuits, is based on the inherently logarithmic relationship between a bipolar transistor's collector current (I_C) and base-emitter voltage (V_{BE}).

In the design, Q_{1A} functions as the "logging" device and is included within op amp A's feedback loop along with the 15.7-kΩ/1-kΩ divider. An input to A forces the amp's output to achieve the level required to maintain its summing-junction input at zero potential. But because Q_A's response is dictated by its I_C/V_{BE} ratio, A's output voltage is the log of its input.

Op amp B and Q_B provide compensation for Q_A's temperature-dependent V_{BE}. B servos Q_B's I_C to equal the 10-μA current established by the 6.9V LM329 voltage reference and its associated 700-kΩ resistor. This action fixes Q_B's collector current and therefore its V_{BE}. And under these conditions, Q_A's V_{BE} varies only as a function of the input, yielding

$$E_{OUT} = \left(\frac{15{\cdot}7k+1k}{1k}\right) \times (Q_B V_{BE} - Q_A V_{BE}).$$

With Q_A and Q_B operating at different I_Cs, the differential V_{BE}s are

$$\Delta V_{BE} = \left(\frac{KT}{q}\right) LOG_e\left(\frac{Q_A I_C}{Q_B I_C}\right),$$

where K=Boltzmann's constant, T=temperature in degrees Kelvin and q=electron charge.

To find the circuit's output, combine these equations to yield

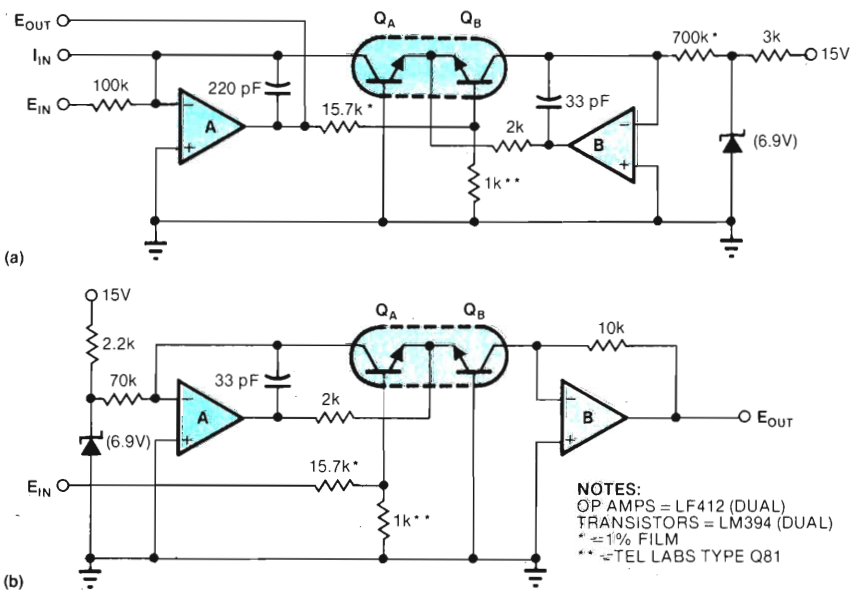
$$E_{OUT} = \left(\frac{-KT}{q}\right)\left(\frac{15{\cdot}7k+1k}{1k}\right) \times LOG_e\left(\frac{E_{IN}\ 700k}{6{\cdot}9V\ 100k}\right).$$

Here, 6.9V equals the LM329's output, 100k is the input resistor and $E_{IN}>0V$.

Although this relationship confirms the circuit's linear-to-log transfer function, it's not the whole solution; without some form of compensation, the circuit's scale factor varies with temperature. The simplest solution is to have the 1-kΩ resistor also vary with temperature; using the indicated resistor, the design is compensated to within 1% over −25 to +100°C.

If your application needs an exponential expansion instead of a logarithmic compression, just turn the circuit in **(a)** around. In the resulting exponentiator scheme **(b)**, Q_A gets driven via the 15.7-kΩ/1-kΩ divider. Here Q_B's I_C varies exponentially with its V_{BE}, and op amp B converts this current into an output voltage.

Although these circuits are easy to construct and use, you must take one precaution: Because of the devices' V_{BE} temperature dependency, you must keep the transistors and the 1-kΩ resistor at the same temperature. The transistors are a dual unit and thus track each other. The 1-kΩ resistor must be mounted as closely as possible to this unit, and the entire network must be isolated from air drafts and changing thermal currents on the pc board. The KT/q factor for which the resistor compensates varies by approximately 0.3%/°C; a few degrees difference between the components therefore introduces a significant error.



Logarithmic and exponentiating circuits *employ the inherent logarithmic relationship of a bipolar transistor's collector current to its base-emitter voltage. The logging circuit* ***(a)*** *displays an input-current-to-output-voltage transfer conformity within 1% over an input-current range of nearly six decades. Similar performance results when you reverse the circuit to form* ***(b)****'s exponentiator. A temperature-compensating resistor provides −25 to +100°C stability.*

control environments. Such applications require a high pumping rate for system flushing or process startup but a much lower, very accurate flow for maintaining the process.) Trying to meet these requirements with, say, a dc motor is difficult at best: If the motor can deliver high-speed performance, accurate control at, say, 0.1% of its maximum speed proves difficult.

Fig 1's design, however, satisfies a pump's conflicting high/low-speed drive requirements by employing an exponentially controlled stepper motor as the prime mover. In this scheme, the exponentiator—comprising IC_{1A} and Q_{1A}—gets driven by IC_{1B}. But here, unlike the version discussed in the **box,** Q_{1B}'s collector *draws* current from integrator IC_{2A}. This stage ramps up (trace **A**) until reset by level-triggered IC_{2B} (trace **B**). (Trace **C** shows how the 100-pF capacitor provides positive ac feedback to this stage's + input.) In this fashion, the oscillator's frequency follows the amount of current that Q_{1B} draws from IC_{2B}'s input. (Note that because IC_{2A}'s summing junction is always at virtual ground, this circuit is similar to the one in the **box**.)

IC_{2B}'s output clocks a dual JK flip flop that's wired to provide the 4-phase signal needed to drive the stepper motor. Using an exponentiator in this way, you achieve a very fine and predictable low-speed control (for example, 0.1 to 10 rpm), yet retain the motor's high-speed capabilities. To calibrate this circuit, ground the V_{IN} pin and adjust the 0.1-Hz trimmer until oscillation just ceases. Next, apply 7.5V to V_{IN} and adjust the 600-Hz trimmer for a 600-Hz frequency.

Sweep the audio spectrum with four ICs

By employing a more accurate voltage-to-frequency converter (VFC), you can extend **Fig 1**'s concepts to cover the complete audio spectrum **(Fig 2).** Intended for laboratory and audio-studio applications, this design provides an output frequency that varies exponentially with a linear input-voltage sweep. Because the scheme uses a VFC IC, its transfer specs remain within 0.15% from 10 Hz to 30 kHz. Thus, it's suitable for use in music synthesizers or for making swept distortion measurements. In the latter application, its output drives a sine-encoded ROM/DAC or analog shaper.

In the **Fig 2** circuit, IC_{1B} derives the voltage that drives IC_{1A}'s input and the zero trimmer from the VFC's internal reference. The exponentiator functions exactly like the design described in the **box** to convert a linear input voltage into a nonlinear collector current for driving the VFC. The VFC's direct 10-Hz to 30-kHz output also clocks a D flip flop and thus provides a 5-Hz to 15-kHz square wave. To align the circuit, ground the V_{IN} port and adjust the zero trimmer until a 2- to 3-Hz oscillation just starts. Then apply −8V and adjust the full-scale trimmer for a 30-kHz signal. For the component values shown, this process yields an exponentiator K factor of 1V/octave.

Try an electronic dipstick

Fig 3 demonstrates how an exponential measuring circuit satisfies the requirement for a noninvasive, high-reliability gasoline gauge. This scheme nonlinearly measures a fuel tank's contents to suit applications—such as remote irrigation-pump installations—that benefit from depleting the tanks as much as possible (without running out of fuel) to eliminate condensation buildup. Such performance requires a scale expansion near "empty" but not near "full."

This acoustically based design operates by bouncing

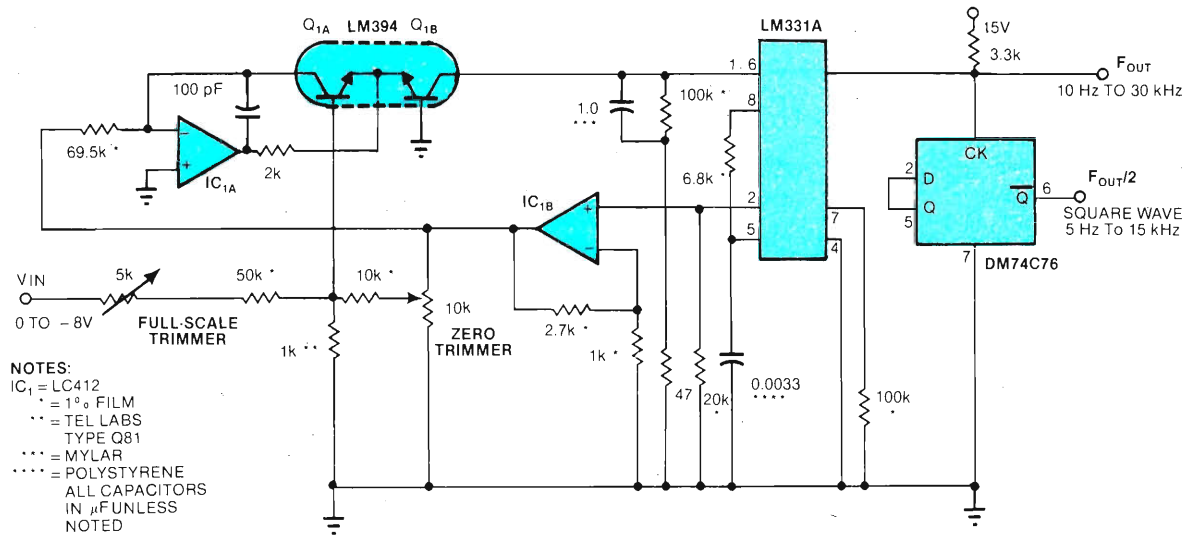
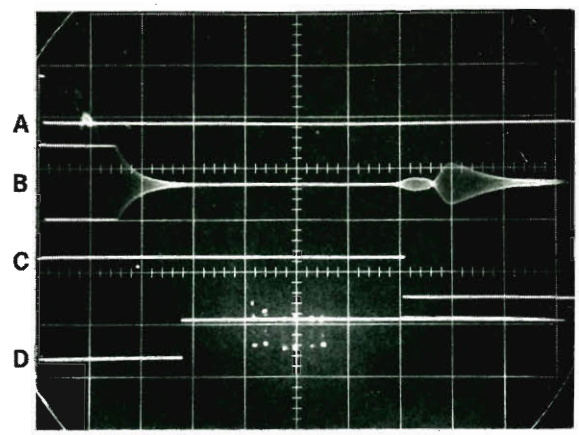


Fig 2—An exponentially swept audio spectrum *results when an input ramp voltage drives a voltage-to-frequency converter. Because the linear input is exponentiated, the circuit's output frequency varies 1V/octave.*

Ultrasonics and time expansion measure a fuel tank's contents

an ultrasonic signal off the fuel's surface and measuring the pulse's round-trip time—the longer the time, the lower the fuel level. Round-trip time gets converted to a voltage that in turn gets exponentiated to yield a high-resolution readout when the tank is nearly empty.

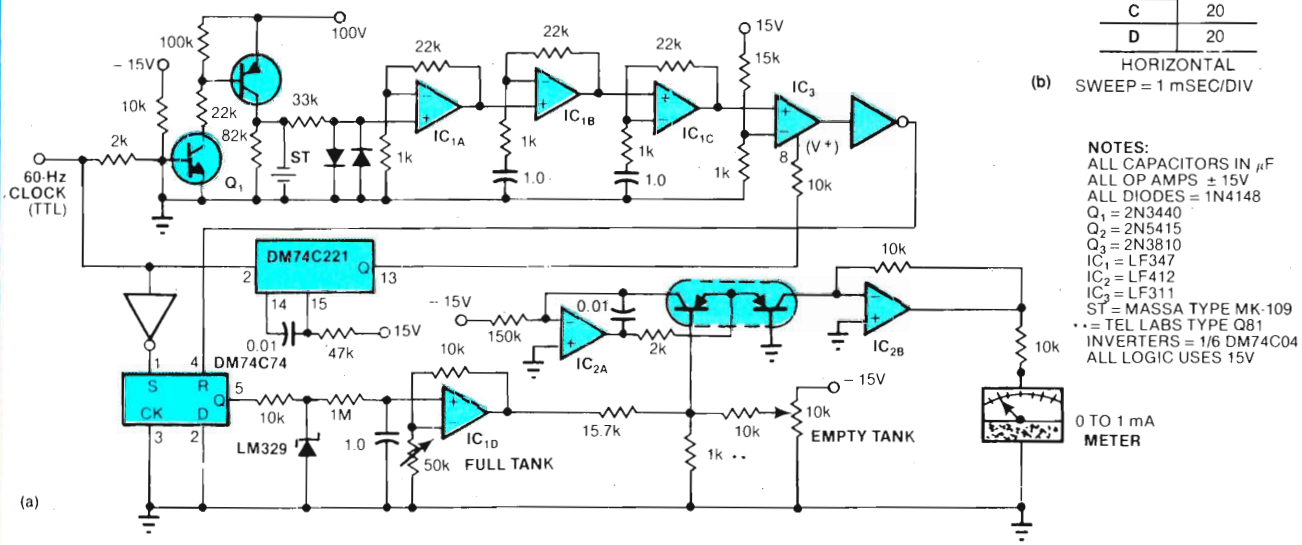
The 60-Hz-based clock pulse (trace **A**) drives a transistor pair and the sonic transducer ST with a 100V pulse. This same clock signal concurrently disables the receiver (to preclude false responses arising from noise) via a one-shot (traces **B** and **D**) and sets a flip flop (trace **C**). The one-shot then again goes HIGH (D), and the receiver (using the same sonic transducer) "hears" the echo and resets the flip flop (**C**). (This elapsed time (**C**) represents the tank's remaining fuel.) The flip flop's output gets clamped by the LM329, integrated by IC_{1D}



TRACE	V/DIV
A	10
B	20
C	20
D	20

HORIZONTAL SWEEP = 1 mSEC/DIV

(b)



NOTES:
ALL CAPACITORS IN μF
ALL OP AMPS ± 15V
ALL DIODES = 1N4148
Q_1 = 2N3440
Q_2 = 2N5415
Q_3 = 2N3810
IC_1 = LF347
IC_2 = LF412
IC_3 = LF311
ST = MASSA TYPE MK-109
•• = TEL LABS TYPE Q81
INVERTERS = 1/6 DM74C04
ALL LOGIC USES 15V

Fig 3—A sonic transducer (ST) *gauges a fuel tank's contents by transmitting a signal and measuring the echo's return time. When the 60-Hz clock fires the transducer (trace* ***A****), the receiver saturates (trace* ***B****) before it's disabled by the 221's LOW output, trace* ***D****. (Trace* ***C*** *shows the time-measuring flip flop being set HIGH by the same clock pulse.) A few milliseconds later, the 221 times out, going HIGH* ***(D)*** *and allowing the receiver to detect the echo* ***(B)*** *and reset the timing flip flop* ***(C)****.*

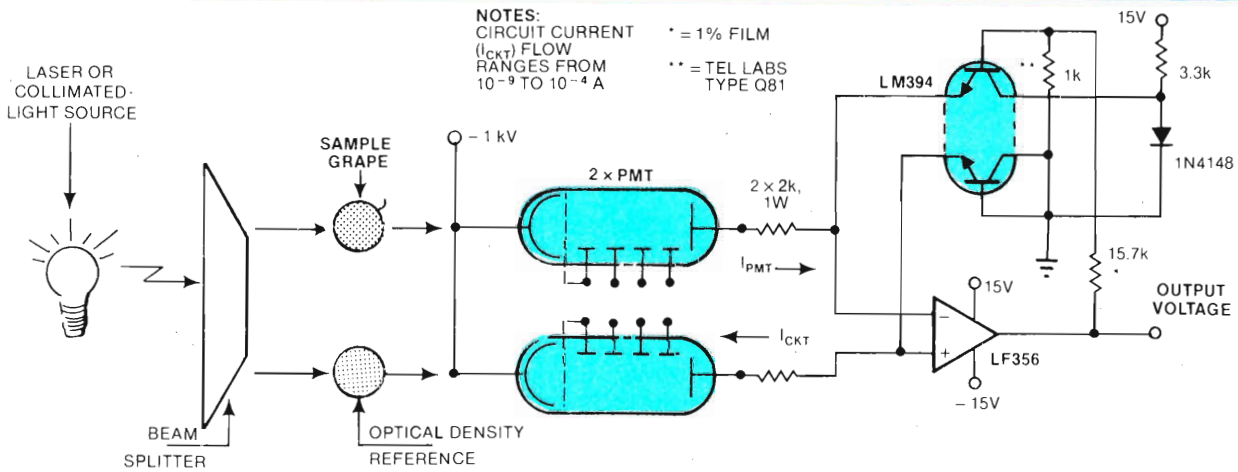


Fig 4—Photomultiplier tubes (PMTs) *determine a grape's ripeness by comparing its optical density with a reference. By using an active feedback, you can algebraically sum the PMTs' outputs in a log-ratio amplifier to yield accurate results over a 5-decade range.*

Photomultipliers determine grape ripeness, produce finer wines

and exponentiated via IC_{2A}, Q_3 and IC_{2B}. The result drives a 1-mA FS meter. The design's 1V/decade scale factor equates to a meter reading of 10% FS for an 80%-full tank; the meter's last 20% corresponds to the tank's last 2%.

Finer wines through science

Another example (**Fig 4**) demonstrates how logarithmic feedback networks can extend a photomultiplier tube's (PMT's) response range without employing complex current sources.

This design determines an object's optical density using photometric techniques. In it, a light source is optically split; one beam passes through a density reference, the other through the sample. (The sample in this case is a grape. The object of the test is to determine its ripeness.) The PMTs detect the light beams' different intensities and convert these signals to output currents. (For a discussion of a PMT's characteristics and a suitable 1-kV power-supply design, see EDN, February 3, pg 127.) The PMTs' outputs—which can range from 10^{-9} to 10^{-4}A—get summed in a log-ratio stage. This technique results in an amplifier output that's proportional to the two channels' density ratio; it's a measurement that has a wide dynamic range and isn't affected by variations in the light source's intensity. Theoretically, a less-than-perfect current-to-voltage conversion results because the log amp's inputs aren't at virtual ground. In fact, however, this error is insignificant because the PMTs' output impedance is very high. This simple circuit's most significant error results from the transistors' collectors operating at slightly different potentials. But for this application, you'll never taste the difference. **EDN**

Author's biography

Jim Williams, applications manager with National Semiconductor's Linear Applications Group (Santa Clara, CA), specializes in analog-circuit and instrumentation development. Before joining National, he served as a consultant at Arthur D Little Inc and directed the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art and collecting antique scientific instruments in his spare time.

Article Interest Quotient (Circle One)
High **470** ***Medium*** **471** ***Low*** **472**

Current-source alternatives increase design flexibility

An op amp's feedback loop is an excellent constant-current circuit. But if your requirements call for a ground-referenced load, high speed or high efficiency, consider several other approaches.

Jim Williams, National Semiconductor Corp

If traditional feedback-loop-based methods of current control aren't adequate for your needs, investigate some alternative approaches to designing constant-current sources. The circuits described here can prove useful in a variety of applications requiring current rather than voltage control—resistance-temperature-detector (RTD) and thermistor excitation, ramp generation and deflection-yoke modulation, for example.

Traditional method exhibits shortcomings

The most commonly used current source—the one most frequently encountered in op-amp cookbooks—is the feedback loop of an operational amplifier (**Fig 1**). Although the amplifier's voltage gain varies with R_{FB}, the current in the feedback loop remains fixed, assuming a fixed E_{IN} and R_{REF}. Thus, the op amp, viewed from the feedback resistor, is a constant-current source. The amplifier inputs accommodate offset and scaling.

In general, this simple op-amp-based circuit provides good results. You can increase current or voltage compliance by adding an output stage, and precision greater than 0.01% is easy to achieve. However, the approach also has limitations. The most serious is that the current-driven load isn't referred to ground. Although the amplifier junction is at 0V, it's forced there by feedback and remains sensitive to noise and lead capacitance. Thus, because remote transducers and test fixtures are often driven with respect to ground, feedback-loop designs often exhibit problems.

Providing a grounded load

The clever circuit shown in **Fig 2,** devised in 1959 by B Howland at MIT, solves this ground-reference

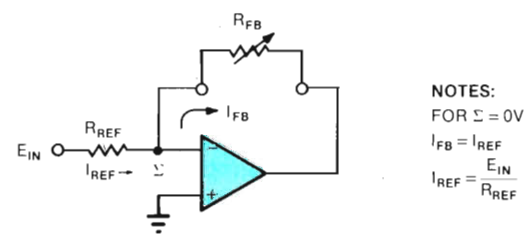


Fig 1—A feedback-loop-based current source *produces excellent results but isn't useful in applications requiring a ground-referenced load.*

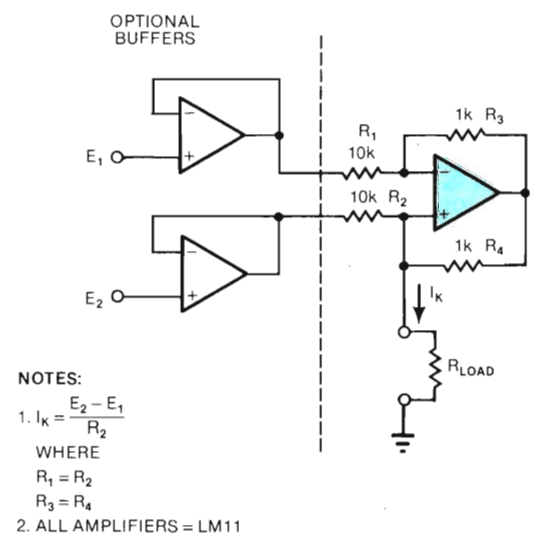


Fig 2—A Howland current-source circuit *supplies a grounded load and has differential inputs.*

problem. This single-amplifier circuit is a true instrumentation-grade current source: It supplies a grounded load and has fully differential inputs. You can delete the input followers if you don't need high input impedance.

Because positive feedback makes the circuit's output impedance appear infinite, understanding circuit operation isn't easy. To start, assume E_1 is 0V, E_2 is some positive value and the load is a short circuit. The configuration is then the well-known inverting amplifier. Because the input E_1 is at 0V, the output is also 0V, and input current E_2/R_2 is the only current flowing into the now-shorted load.

As the current-driven load's resistance increases, the voltage across the load also increases. This increasing voltage at the op amp's noninverting input forces the voltage at the inverting input to rise. As a result, the negative-feedback network causes the op-amp output to rise above the inverting-terminal potential; the op amp supplies the additional current to the load that's no longer supplied from E_2. In other words, as the load value increases, less and less current gets taken from E_2, with the op amp taking up the slack.

For precision results, this circuit demands an op amp with good common-mode rejection; in dc operation, an LM11 provides 0.01% precision without too much difficulty. *(Ed Note: A future article will examine the Howland circuit in greater detail.)*

Increasing voltage compliance

Another way to achieve grounded-load operation involves the circuit shown in **Fig 3.** Here, the op amp forces the voltage across R_1 to equal the LM385 voltage

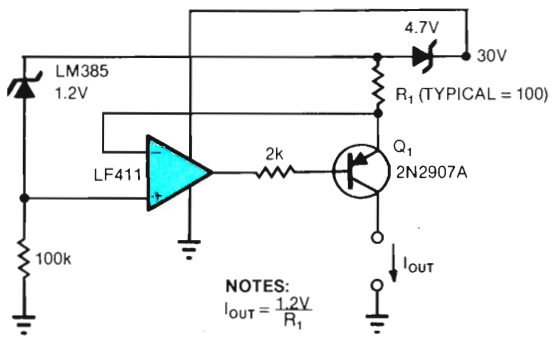


Fig 3—Another way to achieve grounded-load isolation *is to force the potential across R_1 to equal the LM385's 1.2V reference voltage. This circuit achieves higher voltage compliance than* ***Fig 2****'s.*

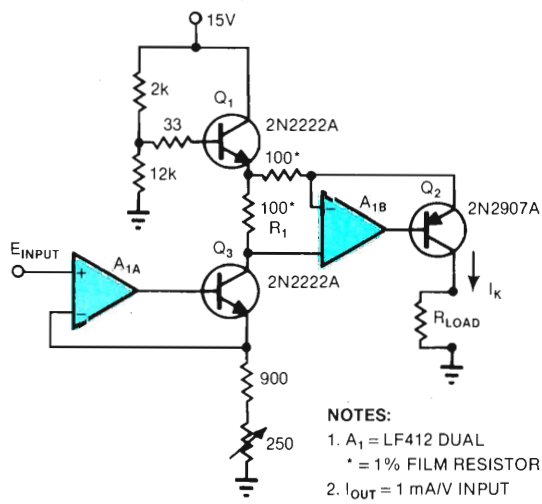


Fig 4—Achieve voltage control *by forcing the voltage drop across R_2 to equal the drop across R_1.*

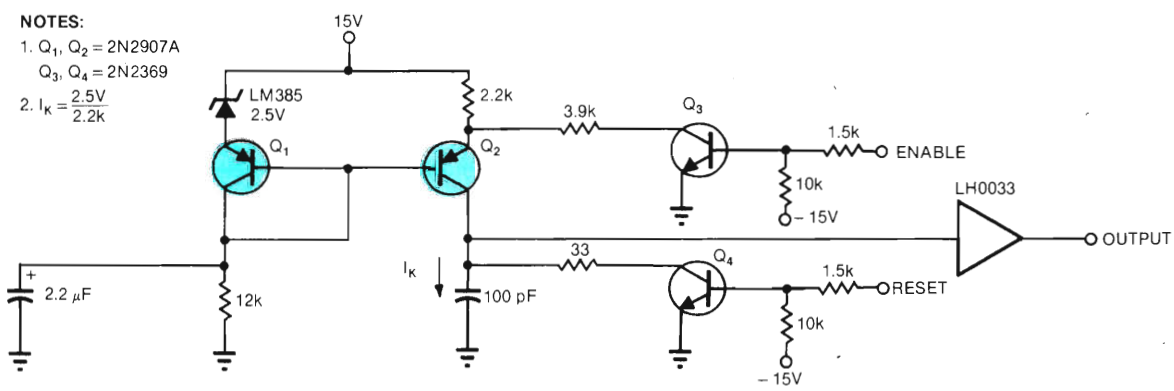


Fig 5—High-speed operation *results when you abandon feedback techniques. Obtain ramp-and-pedestal operation by gating the charging current to the loop's capacitor.*

reference's 1.2V potential, regardless of transistor Q_1's load. The 4.7V zener diode ensures that the op amp's inputs are within its common-mode range. The circuit's output current measures

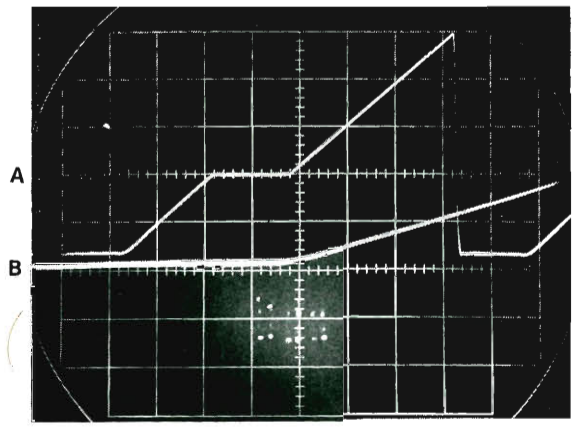
$$I = 1.2V/R_1.$$

This circuit's advantage compared with the Howland design is its greater voltage compliance. That is, it exhibits a greater ability to maintain current in high-resistance loads. (In an ideal current source, the voltage goes to infinity when you increase the load because the source tries to maintain constant current. In **Fig 3**'s circuit, the voltage output rises with increasing load resistance to a maximum value of 24V; beyond this voltage-compliance value, the output source can no longer increase the resistor's voltage, and it clips.)

Voltage-controlled source sports high impedance

If you need a voltage-controlled ground-referenced current source, consider **Fig 4**'s design. This circuit features high input impedance and noninverting operation. A_{1A} and Q_3 act as a voltage follower, producing an input-voltage-controlled drop across R_1. A_{1B} and Q_2 then force this drop to appear across R_2; Q_2's collector supplies the output current. Q_1 acts as a voltage regulator, reducing the supply voltage to 12V so that A_{1A} and A_{1B} operate within their common-mode range.

The 250Ω potentiometer provides trimming, resulting in an input/output relationship of 1 mA/V. To set the scale factor, apply 10V to the input and adjust the potentiometer for 10-mA output. You can alter the scale factor by changing R_2.



TRACE	VERTICAL	HORIZONTAL
A	2V/DIV	500 nSEC/DIV
B	0.2V/DIV	50 nSEC/DIV

Fig 6—The ramp-and-pedestal operation *of* ***Fig 5****'s circuit shows sharp transitions, with no ripple.*

Abandon feedback for high speed

In addition to lacking the ability to operate with a grounded load, feedback-loop-based circuits can't achieve accurate high-speed operation without using

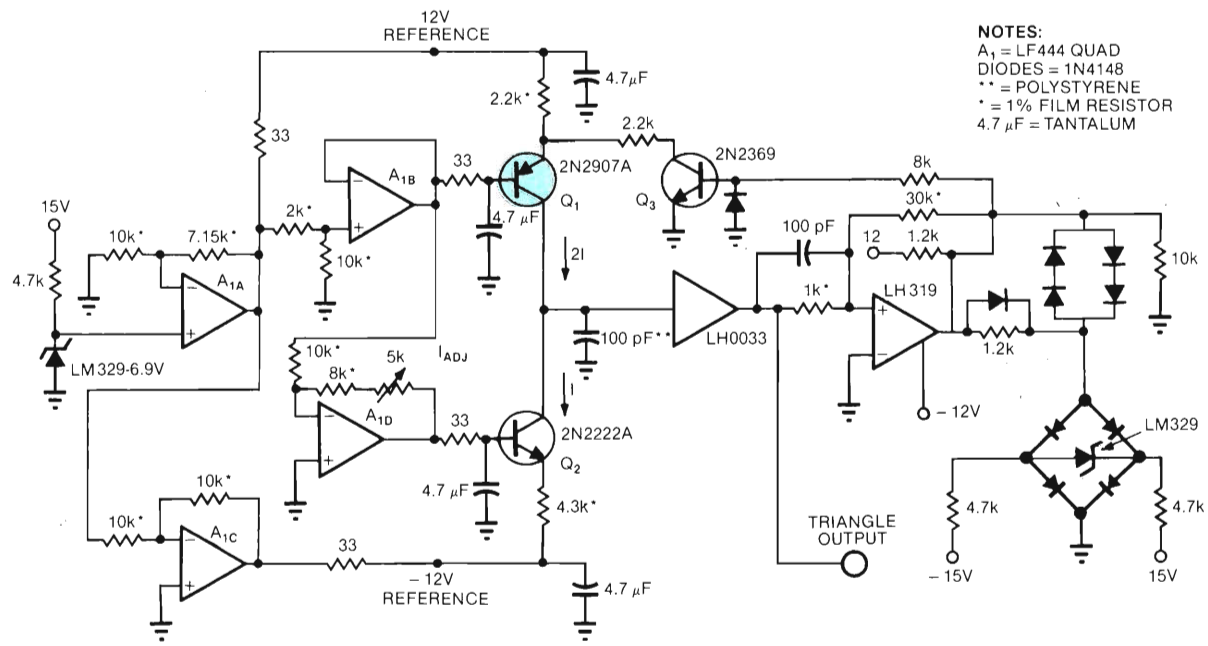
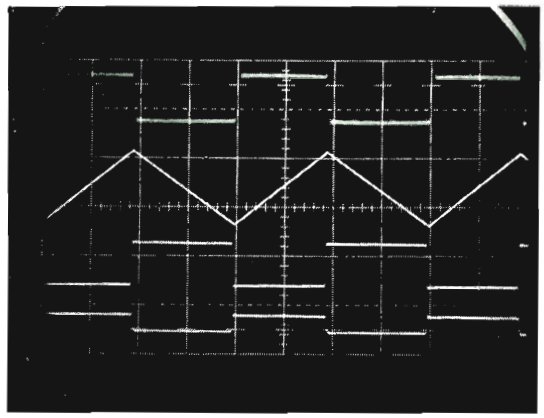


Fig 7—A bipolar current source *generates a highly linear triangular wave. It functions by alternatively charging and discharging a capacitor with positive and negative currents.*

Abandon feedback for high-speed operation



TRACE	VERTICAL	HORIZONTAL
A	2 mA/DIV	200 nSEC/DIV
B	2V/DIV	200 nSEC/DIV
C	20V/DIV	200 nSEC/DIV
D	10V/DIV	200 nSEC/DIV

Fig 8—Performance to several megahertz *characterizes* ***Fig 7****'s circuit.*

elaborate and expensive op amps. That is, the ac dynamics of maintaining accurate feedback place limitations on loop-based current sources. Fortunately, several high-speed alternatives are available.

In **Fig 5**, for example, the Q_1/Q_2 transistor current source supplies a gateable current to the 100-pF capacitor to produce a very-high-speed voltage ramp. (Q_2 is the actual current source, with Q_1 furnishing V_{BE} compensation.) The LH0033 buffer provides a low-impedance output; the LM385 reference fixes the current, which you can vary by changing the value of Q_2's emitter resistor.

Q_3 gates the current source by reverse-biasing Q_2. This procedure allows you to obtain the high-speed ramp-and-pedestal operation shown in **Fig 6**'s trace A—a common requirement in nuclear- and particle-research instrumentation. Because the design has no feedback loop, operation is quick and clean, even at high speed. **Fig 6**'s trace B shows an expanded version of the center section of trace A. Here, the pedestal begins to ramp as the source is gated ON. The transition is sharp, with no discontinuities.

Another high-speed current source appears in **Fig 7.** Here, alternately charging a capacitor with positive and negative current sources generates a high-linearity 1.5-MHz triangle wave—a capability that op-amp based circuits can't achieve. The positive current source Q_1 supplies a current of value 2I to the 100-pF capacitor, while Q_2 sinks I. The resulting charging current is I, and the capacitor charges linearly. **Fig 8**'s trace A shows the charging current, while trace B depicts the voltage across the capacitor.

When the capacitor voltage ramps sufficiently high, the LM319 comparator changes state (trace C), turning transistor Q_3 ON. This action back-biases Q_1 (trace D),

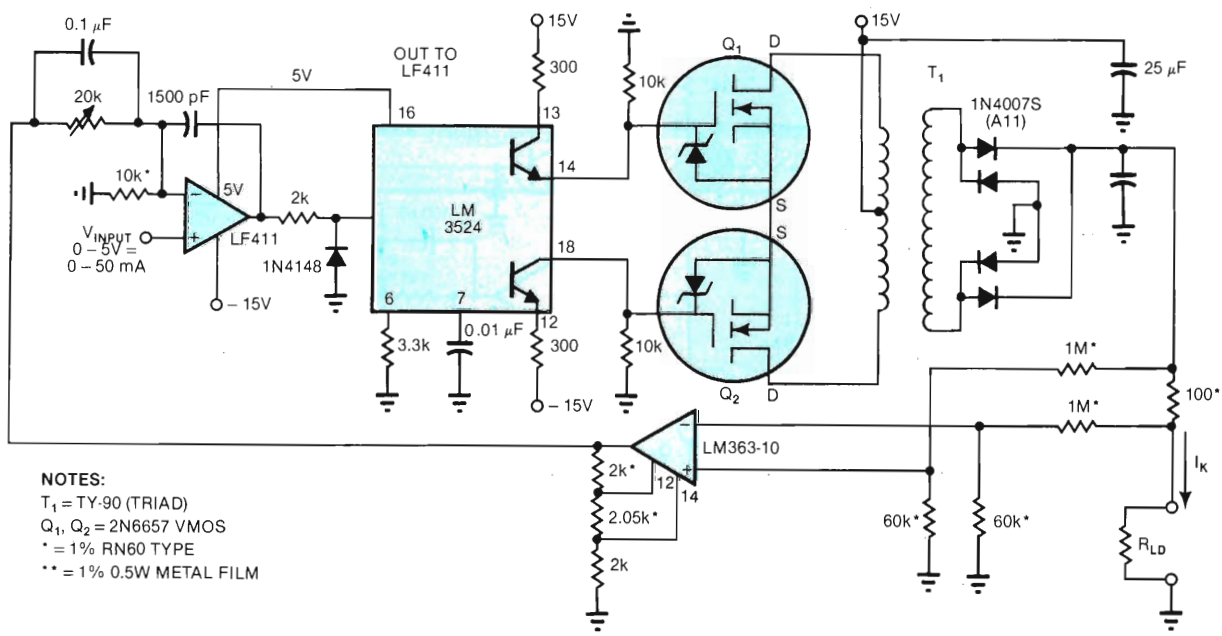


Fig 9—A switching converter *provides 0 to 50 mA into a load, with a compliance of 200V.*

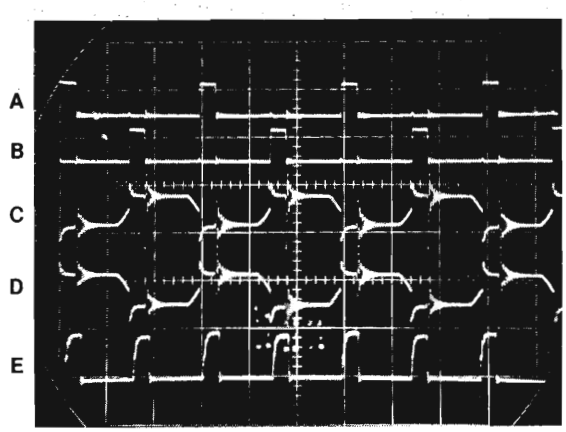
shutting off the 2I current flow. From this point on, the capacitor discharges at a rate proportional to I until the LM319 changes state again, reinitiating the cycle.

The zener bridge and associated diodes ensure a stable, bipolar comparator trip point, while the 100-pF comparator input capacitor compensates for propagation delay. The LH0033 unloads this capacitor, and the quad op amp sets the bias points for the current sources, using the LM329 as the master reference. A_{1A} and A_{1C} generate ±12V for the Q_1 and Q_2 emitters, while A_{1B} and A_{1D} bias the transistors' bases. The 33Ω/4.7-μF combinations furnish decoupling, and the ±12V emitter voltage also biases the comparator's output stage.

You can vary the triangle-wave frequency by driving A_{1B} directly, changing the current sources' base bias. With a good ground plane and a low-capacitance wiring technique, the current sources can generate good triangle waveforms out to several megahertz. To adjust the circuit, trim the I_{ADJ} potentiometer until the triangle waveform is symmetrical. This action essentially adjusts the I/2I ratio and also corrects for propagation-delay-induced errors.

Use a switched-mode source for efficiency

Some current-source applications require high current or high compliance voltage, and in these cases, efficiency suffers. The source shown in **Fig 9,** however, operates in switched mode to achieve low losses.



TRACE	VERTICAL	HORIZONTAL
A	20V/DIV	20 μSEC/DIV
B	20V/DIV	20 μSEC/DIV
C	20V/DIV	20 μSEC/DIV
D	20V/DIV	20 μSEC/DIV
E	2A/DIV	20 μSEC/DIV

Fig 10—Because the pulse drive of Fig 9's switching converter *is not a square wave, the waveforms appear distorted. But the current in the transformer primary is clean and distortion free.*

This current source provides 0 to 50 mA into a load with a compliance limit of 200V. The LF411 receives the control-voltage input and biases the LM3524 pulse-width modulator. The complementary LM3524 outputs (**Fig 10,** traces A and B) drive the VMOS transistors at 30 kHz. The toroidal transformer provides a voltage step-up when excited by these VMOS transistors (drain waveforms appear in traces C and D). Because the pulse drive is not a square wave, the drain-voltage waveforms appear distorted. But the current in the transformer primary is clean and orderly (trace E). The transformer output gets rectified and filtered to produce the current output.

The LM363 divides down the voltage across the 100Ω shunt resistor to a usable level; it also transforms the voltage to single-ended form. The LM363 is trimmed to

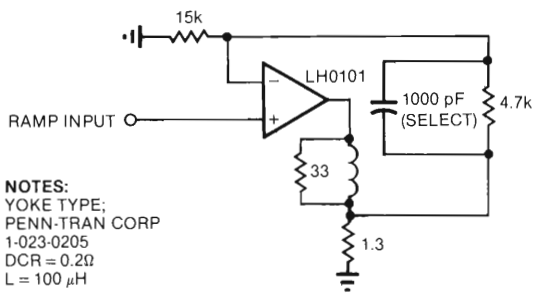


Fig 11—A deflection-yoke driver *achieves precision current drive, avoiding display distortion.*

a gain of 30; its output returns to the LF411, completing a loop that forces the pulse-width modulator to run at whatever duty cycle is required to keep the current through the 100Ω shunt constant, regardless of loading conditions. Although the pulsed transformer can develop a 200V output, it's loop-limited to produce only the voltage required to satisfy the circuit's current output. The result? High efficiency.

The VMOS devices permit high-speed operation while requiring little drive. The LF411 gets driven from the LM3524's internal 5V regulator, ensuring that the LM3524 input can't be overdriven during startup or transients. The capacitors at the op amp ensure loop stability, and the 20-kΩ potentiometer trims the circuit's 100-mA/V scale factor.

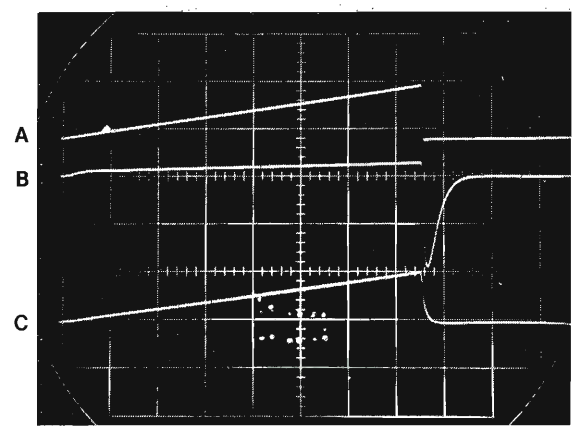
Deflection yokes require current drive

As a final example of a constant-current source, consider the circuit shown in **Fig 11.** It provides a carefully controlled current drive—useful in a precision display's deflection yoke, whose magnetic field is proportional to the current through it.

The LH0101 power op amp provides a current-controlled drive to the yoke at a scale factor of 1V/A.

Obtain high efficiency with a switching converter

The 33Ω resistor furnishes yoke damping; without it, a high inductive flyback voltage would be produced at a step discontinuity. The 1000-pF capacitor trims the circuit. For a ramp input (**Fig 12,** trace A), the yoke

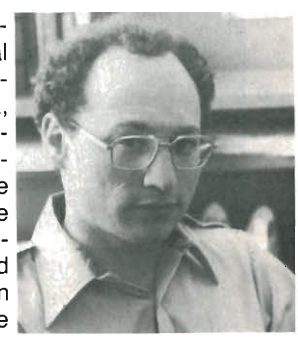


TRACE	VERTICAL	HORIZONTAL
A	2V/DIV	20 μSEC/DIV
B	5V/DIV	20 μSEC/DIV
C	2A/DIV	20 μSEC/DIV

Fig 12—Clean-rising waveforms *and the absence of unruly dynamics characterize* ***Fig 11****'s circuit.*

input current (trace C) rises cleanly with no ripple or discontinuities. When the ramp resets, the inductor current falls to zero, and the op-amp output (trace B) must swing sharply negative to compensate for the inductive flyback. Because damping is optimized, the yoke-current sweep reset is clean and doesn't cause display distortion. EDN

Author's biography



Jim Williams was applications manager in National Semiconductor's Linear Applications Group (Santa Clara, CA), specializing in analog-circuit and instrumentation development, when this article was written. Before joining the firm, he served as a consultant at Arthur D Little Inc and directed the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art and collecting antique scientific instruments in his spare time.

Article Interest Quotient (Circle One)
High **473** ***Medium*** **474** ***Low*** **475**

Analog design techniques suit process-control needs

Although analog circuits are relatively inflexible, they can furnish process-control systems with operational features comparable to those attainable using digital methods. A stepper-motor pump-drive application illustrates the techniques involved.

Jim Williams, National Semiconductor Corp

For many process-control applications, analog control circuits prove a better choice than their digital counterparts, especially when you expect low product volumes and when fast design time and high noise immunity are design priorities. In fact, if you're working with well-defined operational specifications and don't anticipate having to make major modifications, analog methods serve as viable alternatives to intelligent but dedicated and expensive hardware/software approaches.

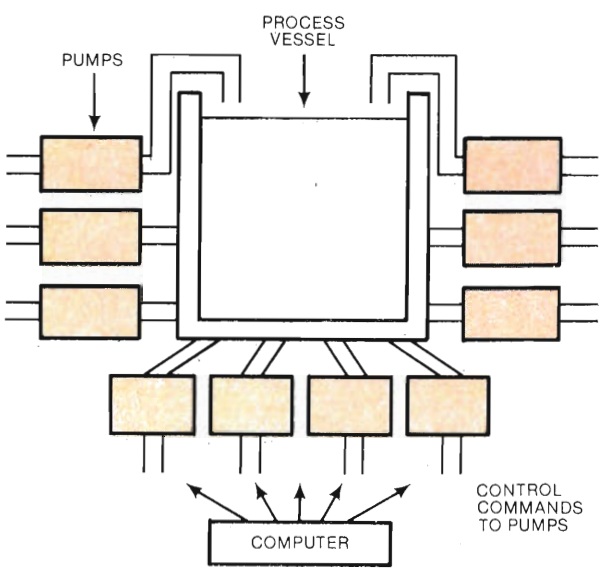


Fig 1—In this conceptual computer-controlled chemical-mixing system, *the computer governs several pumps delivering chemicals to the process mixing vessel by periodically sending updated pulse-width-modulated commands that control the pumps' speeds.*

Controlling a pump's speed

To demonstrate, this article describes the design of an analog pump controller that manipulates computer-generated command pulses to regulate stepper-motor-driven pumps in a critical chemical-mixing process. The controller/pump system furnishes precise fluid delivery at both fast and slow rates, a requirement often arising in chemical and biological process-control systems, which demand high pumping rates for flushing or process startup and slow but accurate flow rates for mixing precise amounts of liquid. Although dc motors can deliver adequate high-speed performance, they often need complex and expensive digital control to perform well at very slow speeds. In contrast, exponentially driven stepper motors can easily handle a pump's conflicting high- and low-speed drive requirements.

Fig 1 diagrams a computer-driven system that governs several pumps feeding an intricate chemical process. The computer controls each pump's speed by periodically sending a pulse-width-modulated control command. Because the computer runs in a time-shared manner, each pump controller must retain the last received pulse width's value.

In this application, each pump gets speed-updated every 30 sec by a 50- to 1000-msec pulse. The pump drive must provide optimum speed-setting resolution for the low-speed ranges to provide increasingly slower

flow rates as the system approaches crucial mixing conditions. And the controller must possess a high degree of noise immunity to prevent spurious noise-induced responses from degrading process quality.

Fig 2 illustrates a μP-based-controller scheme. In this arrangement, the computer delivers an input pulse that gates a clock. The clock in turn serially loads a bank of parallel counters that determine the input pulse width. The counters address a processor section that converts input data to a frequency output, using an exponential transfer function—a nonlinear response that achieves the required high resolution (precise liquid delivery) at slow pump speeds. Finally, the frequency output activates a stepping-motor driver that runs the pump.

On the surface, this digital controller's operation appears relatively simple. However, the application masks some tricky design problems. For example, the lengthy period between speed updates, coupled with the need to avoid erroneous pump responses, mandates careful power-supply design, including provision of such functions as RFI filtering, memory battery backup and self-checking software.

In addition, the need for a high-resolution, smoothly varying frequency-output function demands careful design attention to how the processor synthesizes its

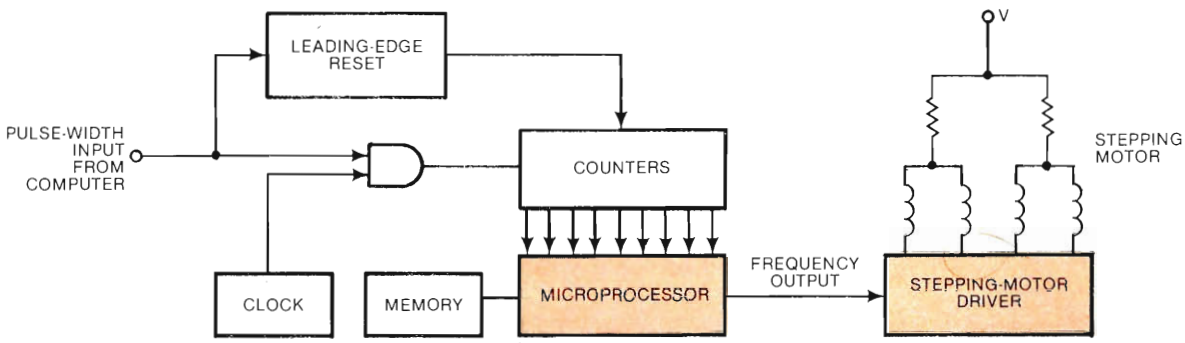


Fig 2—Upon receiving gated pulses, *a μP converts timed computer data into a frequency output, using an exponential transfer function. This nonlinear response results in the necessary high-resolution-at-low-speed characteristics for accurately controlling pump operation with a stepper-motor driver. The problems that can arise with this digital approach to controlling* ***Fig 1****'s mixing system include noise sensitivity, memory-retention difficulties and an undesirable quantized frequency-shift characteristic.*

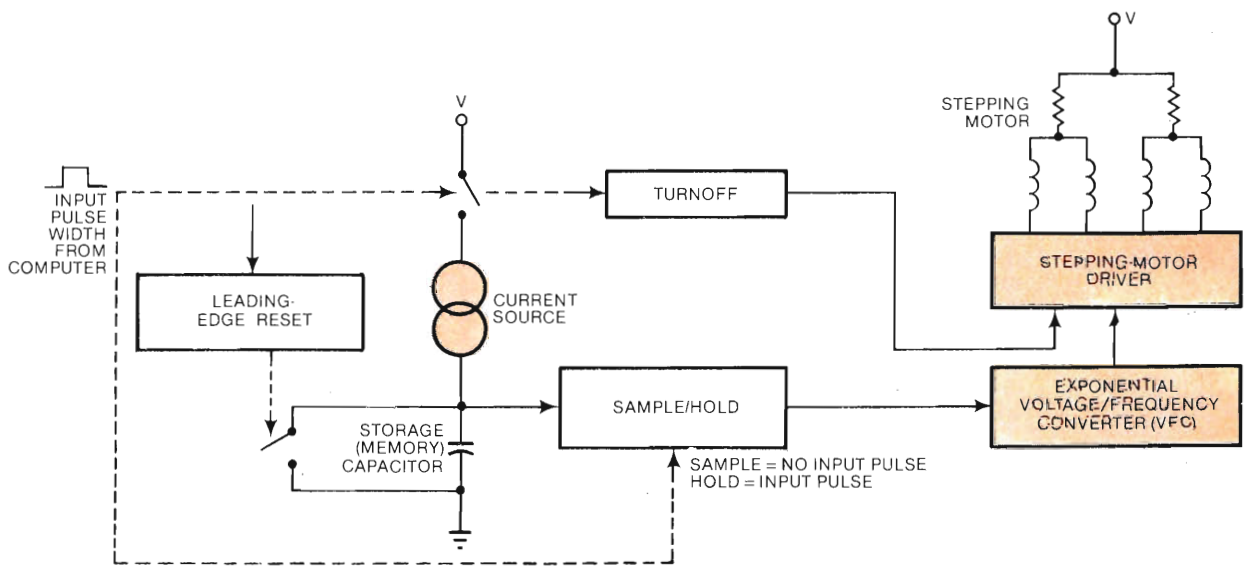


Fig 3—In this analog-pump-controller approach, *a computer's command pulses direct a current source, which in turn charges a storage capacitor that provides noise-immune analog-data retention. When the command pulse ceases, the sample/hold amp receives the capacitor's stored voltage and delivers it to the exponential voltage-to-frequency converter (VFC). The VFC activates the stepper-motor driver in a continuous, smooth manner; the turn-off stage deactivates the motor driver.*

output. Although these problems are amenable to solution, they complicate the controller's design and entail lengthy development time and high cost.

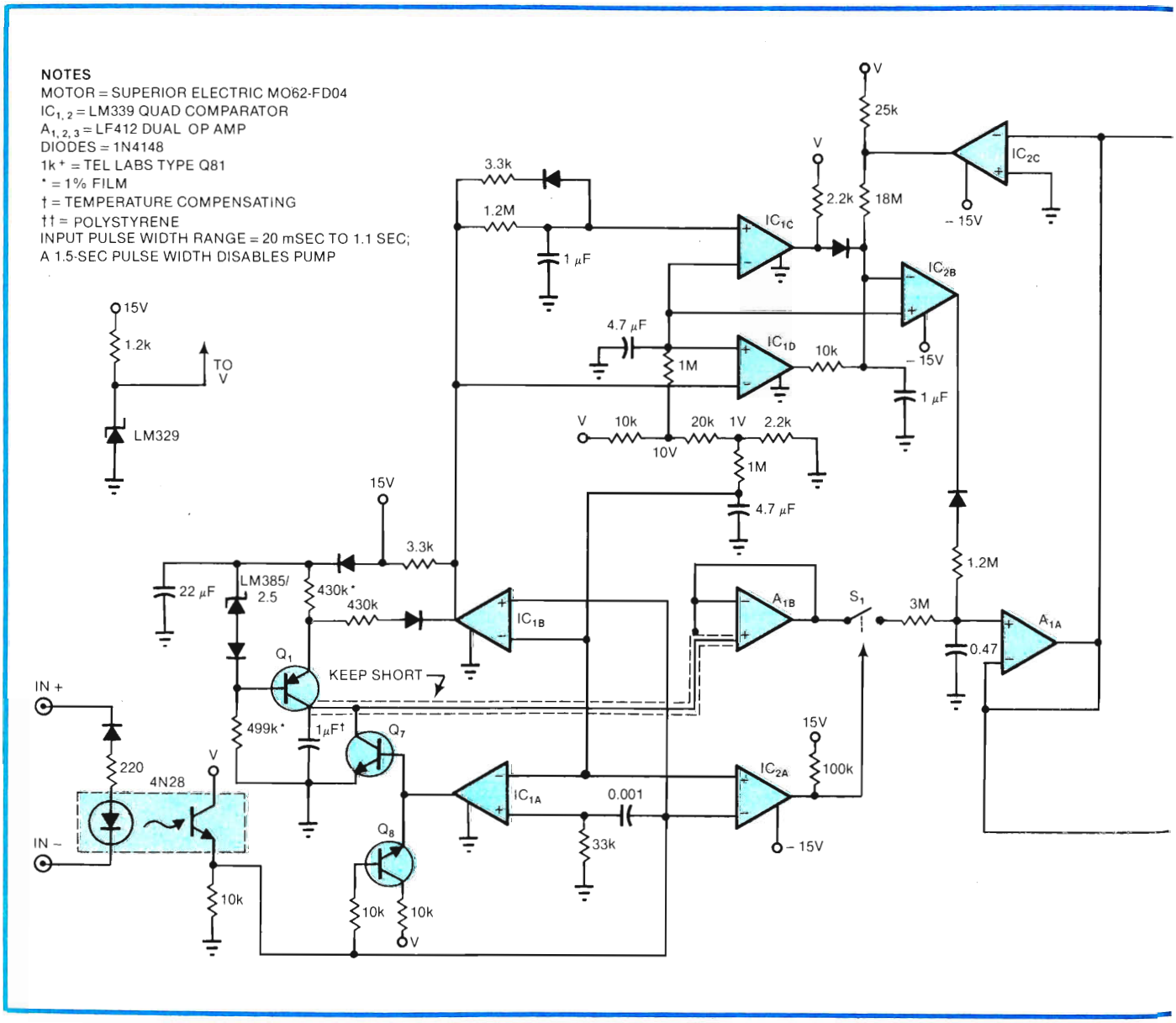
Take the analog route

Considering the task's conceptual simplicity, however, reveals a clear edge for an analog-control approach to satisfying this application's critical requirements. A turnkey system, it needs little intelligence or flexibility and can employ a straightforward data-retention structure. And although the digital μP-based approach can also meet these requirements, it involves substantial hardware and software overhead to overcome noise-immunity and frequency-shift-resolution problems.

The analog-based design surmounts these obstacles, providing inherent noise immunity and superior frequency-vernier capability. More important, though, an analog approach eliminates the intensive software effort required by μP-based methods. As a matter of record, the analog pump-controller design was conceived, breadboarded and released for production in just 4 wks—and at a cost competitive with an alternative μP-based method.

Fig 3 depicts the analog system. In this scheme, a capacitor furnishes memory storage. An exponentially responding voltage-to-frequency converter (VFC) fulfills the function of **Fig 2**'s processor. In operation, the computer's command pulse gates a current source that linearly charges the storage capacitor. While the capacitor is charging, the sample/hold stage enters Hold mode, blocking the capacitor's ramping action from the VFC.

When the command pulse just ceases, the capacitor achieves a voltage level that the sample/hold accepts



and feeds to the VFC. By issuing an extremely wide pulse, the computer actuates the turn-off stage, which deactivates the stepper-motor drive.

Optoisolation eliminates noise

Fig 4 shows the analog pump controller's schematic diagram. To initiate circuit action, the computer sends an input pulse to the 4N28 optoisolator, which eliminates noise-pickup-induced ground-loop and data-line problems. Appearing at its emitter, the optoisolator's output (**Fig 5,** waveform A) goes to IC_{1A} and IC_{1B}. IC_{1A}'s differentiator setup—a 0.001-μF/33-kΩ combination—generates a short pulse (**Fig 5,** waveform B) that biases Q_7. This transistor in turn resets its associated 1-μF capacitor (**Fig 5,** waveform C).

Note that Q_8's emitter supplies the current to base-bias Q_7 ON because IC_{1A} is an open-collector device. In turn, Q_8 receives its base bias from the optoisolator, which provides a drive output only when a command pulse appears at the controller circuit's input. Consequently, in the highly unlikely event that a severe noise disturbance causes IC_{1A}'s output to rise, Q_7 still doesn't receive a drive pulse, and its 1-μF capacitor does not get reset.

The 1-MΩ/4.7-μF filter, which feeds IC_{1A}'s minus input, provides additional noise immunity by ensuring a stable trip point during noise disturbances. The optoisolator's output also goes to IC_{1B}, which gates the Q_1 current source. When Q_7 turns off, its 1-μF capacitor immediately starts to ramp up (**Fig 5,** waveform C). (Circuit-operation speed in **Fig 5** has been increased to provide optimum waveform photographs.) Then, the A_{1B} follower unloads the capacitor.

Diode/capacitor decoupling of Q_1 assures high noise

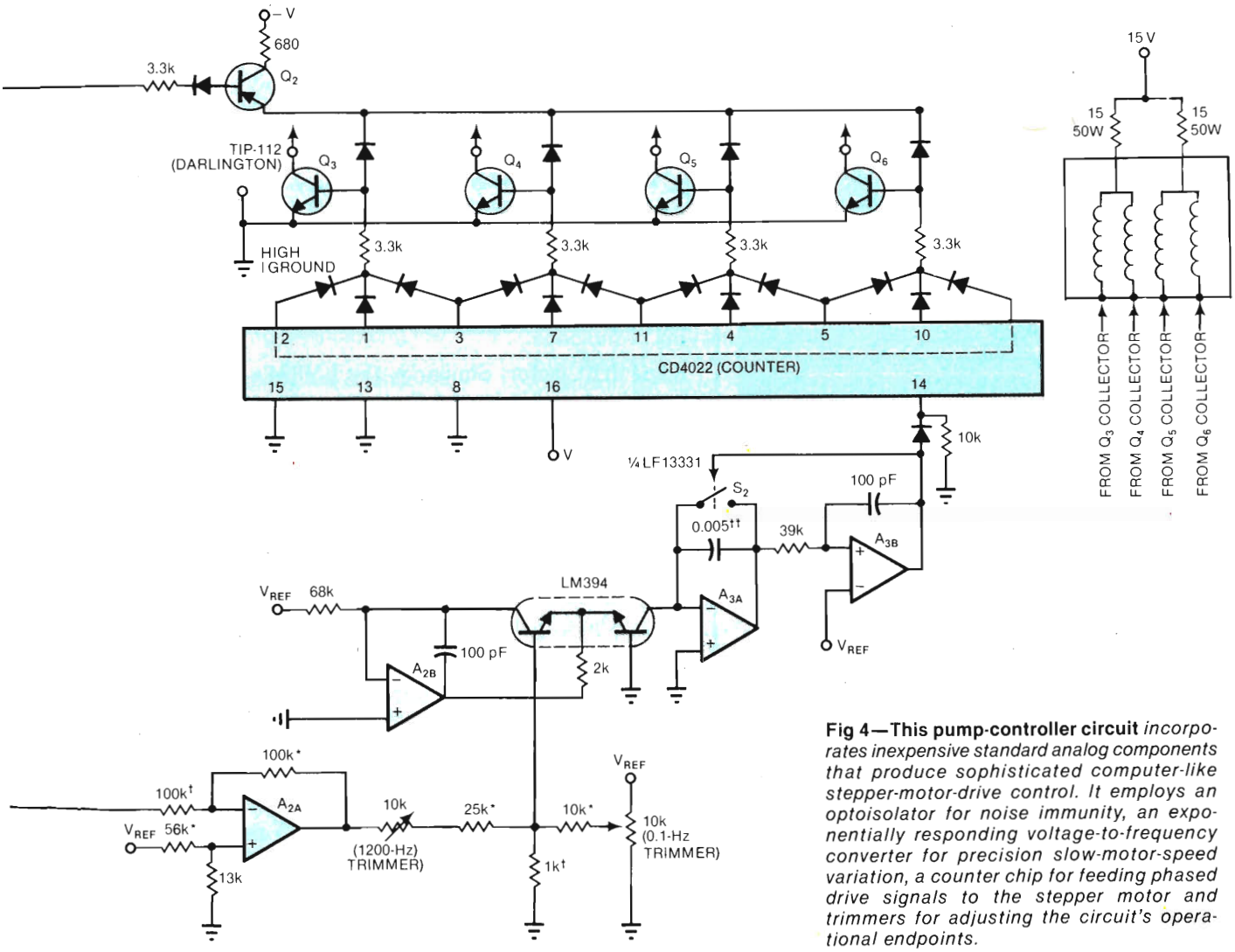


Fig 4—This pump-controller circuit *incorporates inexpensive standard analog components that produce sophisticated computer-like stepper-motor-drive control. It employs an optoisolator for noise immunity, an exponentially responding voltage-to-frequency converter for precision slow-motor-speed variation, a counter chip for feeding phased drive signals to the stepper motor and trimmers for adjusting the circuit's operational endpoints.*

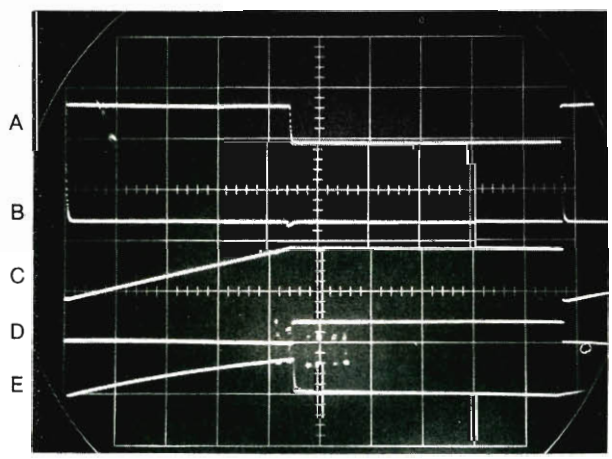
rejection, even for supply dropouts, during the capacitor's ramp time. During ramping, IC_{2A}'s output stays LOW and shuts off S_1. This switch maintains A_{1A}'s output at a dc level. When the controller's input pulse ceases, IC_{1B}'s output goes LOW and disables Q_1. The integrating 1-μF capacitor therefore stops charging. Concurrently, IC_{2A}'s output goes HIGH and closes S_1. As a result, A_{1A}'s output changes to the capacitor's newly acquired level. Located in A_{1A}'s input section, the 3-MΩ/0.47-μF filter provides a time constant that limits the stepper motor's acceleration rate, thereby preventing stalling.

Try an exponentiator

Op amp A_{1A}'s output feeds the A_2-A_3 configuration, which forms an exponentially responding VFC that controls the input current to the A_{3A}-A_{3B} integrator-comparator-type oscillator stage. To accomplish this function, A_{2B} and the LM394's dual transistors constitute a voltage-input, current-output exponentiator in accordance with transistor V_{BE}-vs-I_C characteristics.

The 1-kΩ temperature-compensating resistor connected to the LM394 thermally compensates for the KT/Q drift factor. Similarly, the LM394's dual transistors suppress V_{BE}'s contribution to temperature error. A_{2A} biases the exponential converter's input range by combining A_{1A}'s output with the necessary offset term for proper exponentiator operation. Trimmers allow you to adjust the 1200- and 0.2-Hz endpoints.

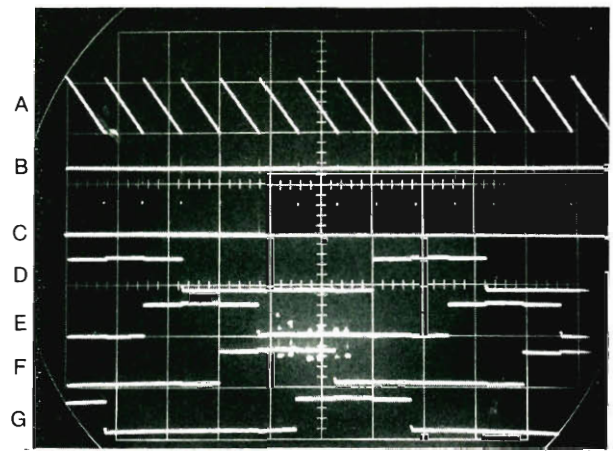
A_{3B}'s pulse-train output contains frequency components that relate exponentially to the controller circuit's most recently received input-pulse width. It drives the CD4022 counter chip, which generates four properly phased signals (**Fig 6**) for driving the stepper.



TRACE	V/DIV
A	20
B	10
C	5
D	50
E	10

HORIZONTAL SWEEP-
1 mSEC/DIV

Fig 5—Important waveforms *found in the analog pump controller's input section include the 4N28 optoisolator's pulsed emitter output* ***(A)****, IC_{1A}'s plus input or memory-reset spike for biasing Q_7* ***(B)****, Q_7's output or current-source-driven ramp for resetting the 1-μF memory capacitor* ***(C)****, IC_{1D}'s output pulse for shutting down the stepper-motor driver via IC_{2B} and IC_{2C}* ***(D)*** *and IC_{1C}'s plus input, which never charges above 10V for the normal range of incoming pulse widths* ***(E)****.*



TRACE	V/DIV
A	5
B	50
C	20
D	20
E	20
F	20
G	20

HORIZONTAL SWEEP-
1 mSEC/DIV

Fig 6—The CD4022 counter chip *in* ***Fig 4****'s pump-controller circuit sends properly phased frequency-modulated drive signals to the pump motor. Waveform* ***A****, for example, represents A_{3A}'s ramp output; waveform* ***B*** *shows A_{3B}'s positive input reset signal; waveform* ***C*** *details A_{3B}'s output pulse; and waveforms* ***D*** *through* ***G*** *depict the four phase-drive signals to Q_3 through Q_6 via diode-ANDed outputs.*

Driving the pump

The additional sections of IC_1 and IC_2 allow the computer's command pulse to shut down the pump. For the normal range of input widths, the 1-μF capacitor at IC_{1C}'s plus input (**Fig 5**, waveform E) never charges above 10V. Under these conditions, IC_{1C}'s output always stays LOW. The only source available to charge the 1-μF capacitor tied to IC_{2B}'s minus input thus comes through the 18-MΩ resistor.

However, during normal operation, A_{1A}'s output remains positive, ensuring that IC_{2B}'s negative input

stays that way. This condition forces IC_{2B}'s open-collector output to float. If the controller circuit receives an input pulse substantially wider than the normal maximum, therefore, IC_{1C}'s input charges above 10V. This action quickly dumps a large charge into IC_{2B}'s 1-μF capacitor, forcing its voltage level to rise to the negative rail. This value pulls A_{1A}'s input negative, turns on Q_2 and cuts off all drive signals to the output transistors (Q_3 to Q_6).

A_{1A}'s negative output also feeds back to IC_{2C}, driving that device's output positive. This output supplies a continuous topping-off current to IC_{2B}'s input capacitor. The connection completes a positive feedback latch, which prevents the pump from operating until the counter receives a pulse width within the controller circuit's normal range. IC_{1D} functions to clear out the IC_{2B} capacitor's charging action (**Fig 5,** waveform D) as each new command pulse arrives.

The time constant associated with A_{1A}'s input section lets the controller circuit examine each received pulse and never disables this clamping performance unless the pulse width resides within established limits. Although the latch's positive feedback doesn't require the computer to send successive shutdown instructions to the pump, the controller circuit ensures that the pump's motor can't be energized, even briefly, if successive turn-off-length pulses appear. **EDN**

Author's biography

Jim Williams, now a consultant, was applications manager with National Semiconductor's Linear Applications Group (Santa Clara, CA) when he wrote this article. Before working at National, he was employed by Arthur D Little Inc and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art and collecting antique scientific instruments in his spare time.

Article Interest Quotient (Circle One)
High **473** ***Medium*** **474** ***Low*** **475**

Conversion techniques adapt voltages to your needs

Different parts of your system often need specialized voltages. A variety of conversion techniques can help you obtain these voltages from the main supply.

Jim Williams, National Semiconductor Corp

Need more than one voltage in a single-supply system design? You can tailor the main system supply by using a variety of techniques; understanding how each works lets you choose the one most appropriate to producing the levels—and characteristics—you need.

Analog circuits need ±15V

Specifically, note that if you have a 5V logic rail available in your system but need ±15V, it's easy to construct a dc/dc converter with an oscillator, a transformer and a rectifier circuit. However, most dc/dc converters suffer from large noise spikes generated by the fast-switching oscillator. So if the analog circuitry is especially sensitive to power-supply noise, you can eliminate or minimize the switching noise by using an interrupt-driven converter or a full-duty-cycle, low-noise converter.

Fig 1 shows an interrupt-driven circuit. The LM3524 switching regulator runs open-loop; its Q_1-Q_2 output pair drives the step-up transformer. Unlike a standard

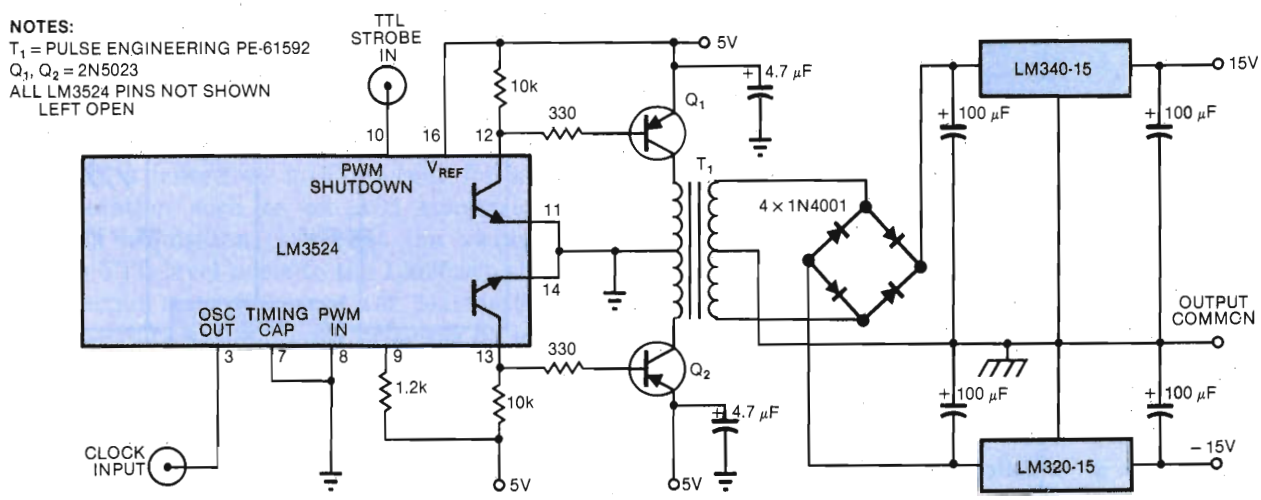
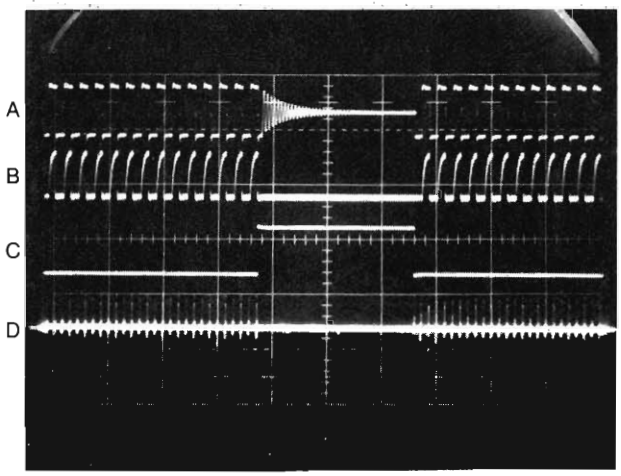


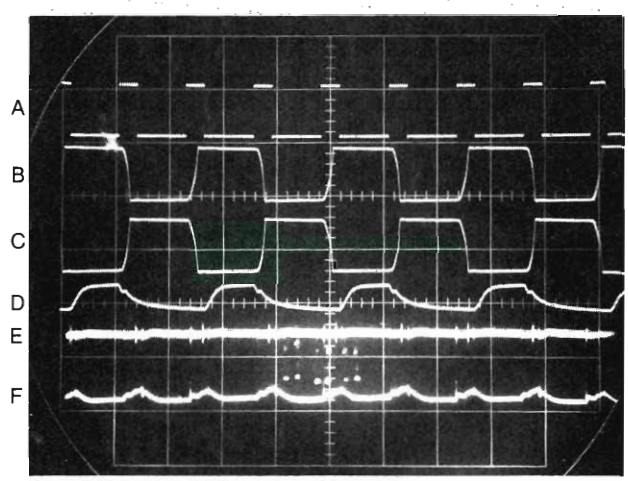
Fig 1—Totally noise free, *this 5V to ±15V converter stops running when you supply a TTL shutdown pulse. The 100-µF output capacitors provide voltage hold-up while your circuit operates.*

Interrupt switching for noise-free operation



TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	200 μSEC/DIV
B	1A/DIV	200 μSEC/DIV
C	5V/DIV	200 μSEC/DIV
D	20 mV/DIV (AC COUPLED)	200 μSEC/DIV

Fig 2—The center portion *of this scope photo shows the drop in output noise (trace D) that occurs when* ***Fig 1****'s converter shuts down.*



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	20 μSEC/DIV
B	10V/DIV	20 μSEC/DIV
C	10V/DIV	20 μSEC/DIV
D	500 mA/DIV	20 μSEC/DIV
E	2 mV/DIV (AC COUPLED)	20 μSEC/DIV
F	100 mV/DIV	20 μSEC/DIV

Fig 4—Barely discernible spikiness *is visible in the output (trace E) of* ***Fig 3****'s low-noise converter.*

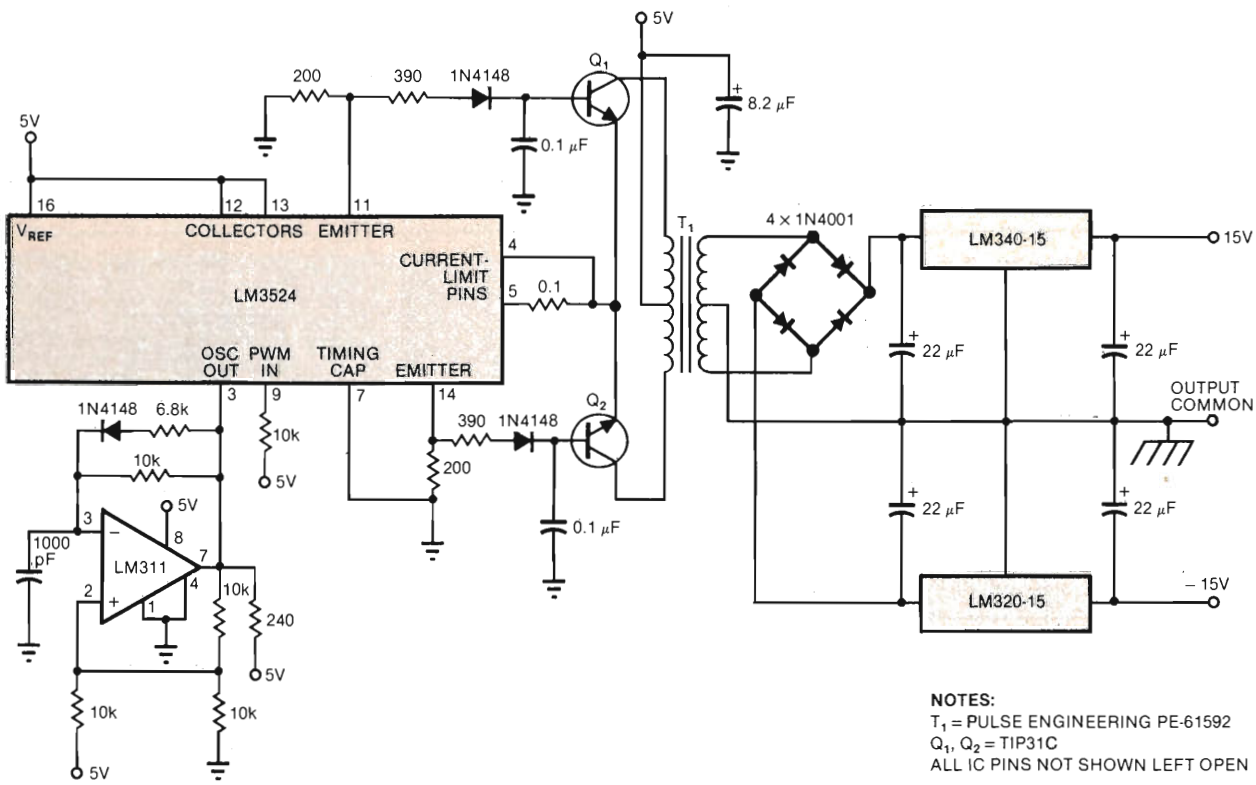


Fig 3—A low-noise converter, *this 5V to ±15V circuit runs continuously, but the output transistors' controlled turn-on and turn-off minimize spikes.*

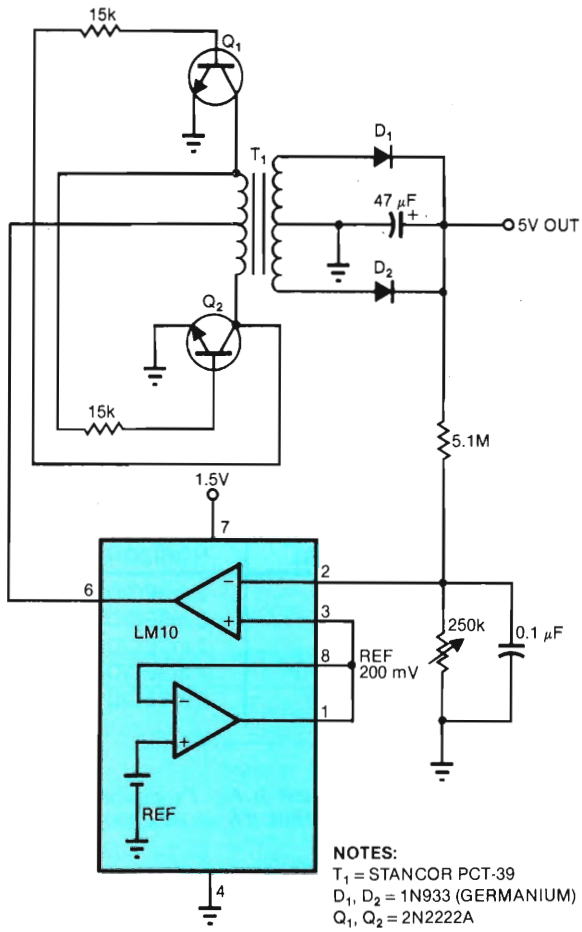


Fig 5—Powered by a 1.5V battery, *this 5V-output design can drive low-power circuitry for months from one cell.*

dc/dc converter, this circuit uses an external clocked oscillator, allowing you to synchronize the converter to the host system. To use this feature, you disable the LM3524's internal oscillator by grounding the capacitor timing pin and apply the system clock to the oscillator output, yielding a 50% switching duty cycle.

To obtain a noise-free ±15V output for a critical circuit operation such as an A/D conversion or a sample/hold acquisition, interrupt the switching by applying a TTL-level pulse to the LM3524's shutdown pin. This action stops the converter, leaving the large output capacitors as a virtually noiseless dc source to power the output regulators.

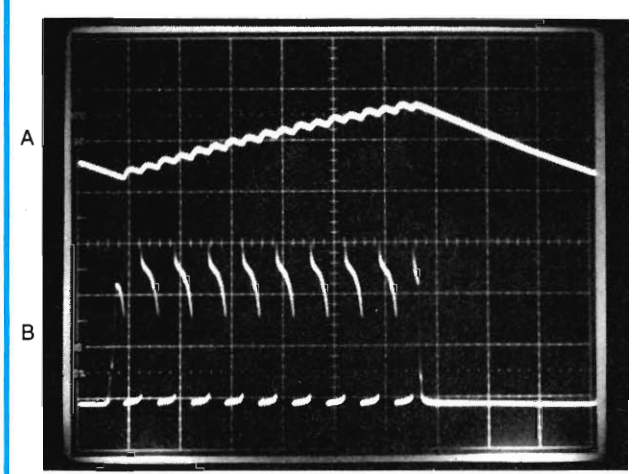
Fig 2 details the circuit's performance; traces A and B show Q_1's voltage and current waveforms, respectively (Q_2's waveforms are similar). Trace D depicts the 15V output line (the −15V line is similar): The noise pulses caused by the switching circuitry are clearly visible. When the interrupt pulse is applied (trace C), the noise disappears. The large output filter capacitors provide adequate ±15V holdup time for the critical operation required while the interrupt pulse is HIGH.

Don't interrupt—just quiet down

If you need a 5V to ±15V converter with low (but not necessarily zero) noise, consider the continuously running circuit shown in **Fig 3.** Here, the LM311 multivibrator clocks the LM3524 (**Fig 4,** trace A), whose internal oscillator is again disabled by grounding the timing-capacitor pin. While the LM311's output is HIGH, the LM3524 cuts the drive to Q_1 and Q_2, helping to minimize switching noise.

The main contributor to low-noise performance is the base-drive slowdown network used with Q_1 and Q_2: The 390Ω/0.1-μF time constant slows turn-on, and the diode forces base-emitter charge trapping to delay turn-off.

The effect of these components is evident in the Q_1-Q_2 collector-voltage waveforms (**Fig 4,** traces B and C) and Q_2's current waveform (**Fig 4,** trace D). Note that the LM311's long ON time permits no current to flow in Q_2 until well after Q_1 has turned off. Moreover, the current's rise and fall times are smoothly controlled and long, unlike those of the more common fast-switching converters. Therefore, very little harmonic content appears in the transformer drive, so converter output noise (**Fig 4,** trace E) is exceptionally low. In addition,



TRACE	VERTICAL	HORIZONTAL
A	0.1V/DIV (AC COUPLED)	10 mSEC/DIV
B	1V/DIV	10 mSEC/DIV

Fig 6—The on-demand operation *of* ***Fig 5****'s 1.5V to 5V converter is evident in this scope photo. The converter turns on when the output drops to approximately 4.93V and off when it rises to roughly 5.07V.*

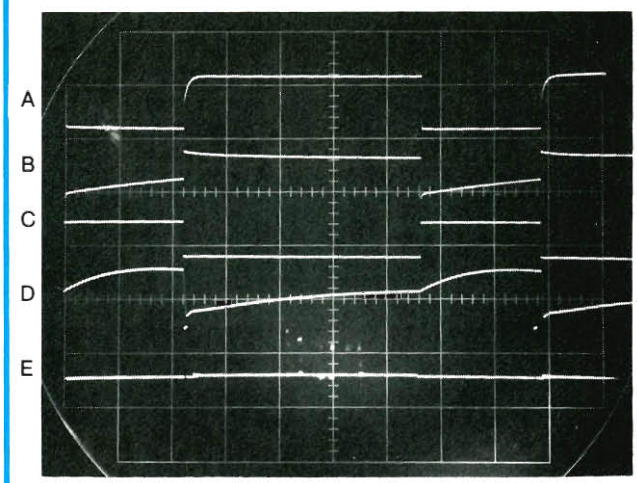
the disturbance to the 5V rail (**Fig 4,** trace F) is small compared with standard designs.

This circuit's low noise comes at the expense of efficiency and available output power, though: During the slow base transitions, Q_1 and Q_2 dissipate power, reducing efficiency to about 50% and available output to approximately 50 mA. Heat-sinking Q_1 and Q_2 won't help, either, because it involves the risk of secondary breakdown. The circuit is, however, short-circuit protected by the 0.1Ω emitter resistor and the LM3524's current-limiting circuitry.

Power circuits from a battery

What if your basic system supply is a battery? The circuit depicted in **Fig 5** supplies 5V from a 1.5V source—such as a battery, saltwater cells or a solar-cell stack. With 125-μA load current (typically 20 CMOS ICs), it runs for 3 months on one D cell.

The circuit is unusual because the amount of time required for Q_1 and Q_2 to drive the transformer is directly related to the load resistance. The LM10 op-amp/reference IC compares the converter's output with its own internal 200-mV reference via the 5.1-MΩ/250-kΩ voltage divider. Whenever the converter's output drops below 5V, the LM10 output goes HIGH, driving the Q_1-Q_2-T_1 oscillator circuit. The rectified transformer output then charges the 47-μF



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	2 mSEC/DIV
B	5V/DIV	2 mSEC/DIV
C	5V/DIV	2 mSEC/DIV
D	50 mA/DIV	2 mSEC/DIV
E	200V/DIV	2 mSEC/DIV

Fig 8—The inductor current *in* ***Fig 7****'s design (trace D) supplies the energy to generate the circuit's 200V output.*

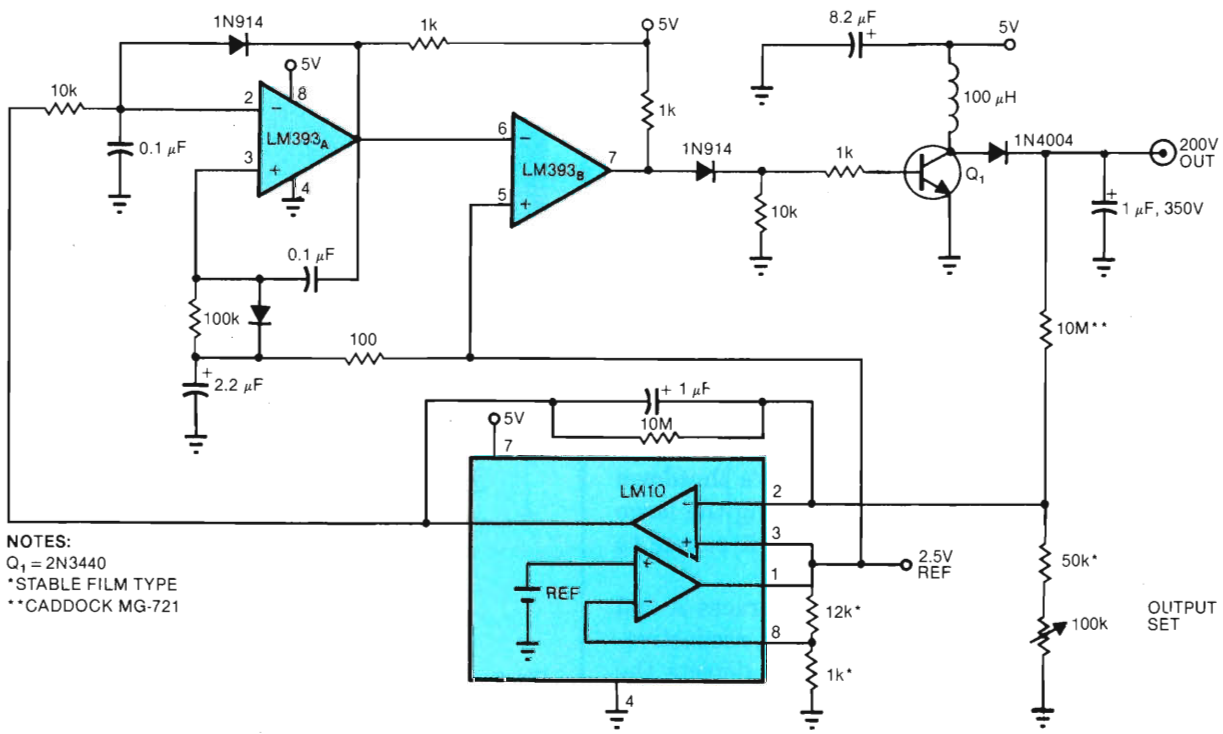


Fig 7—A 40-fold multiplication *of the 5V supply results with this flyback-type converter. It furnishes 200V into a 500-μA load.*

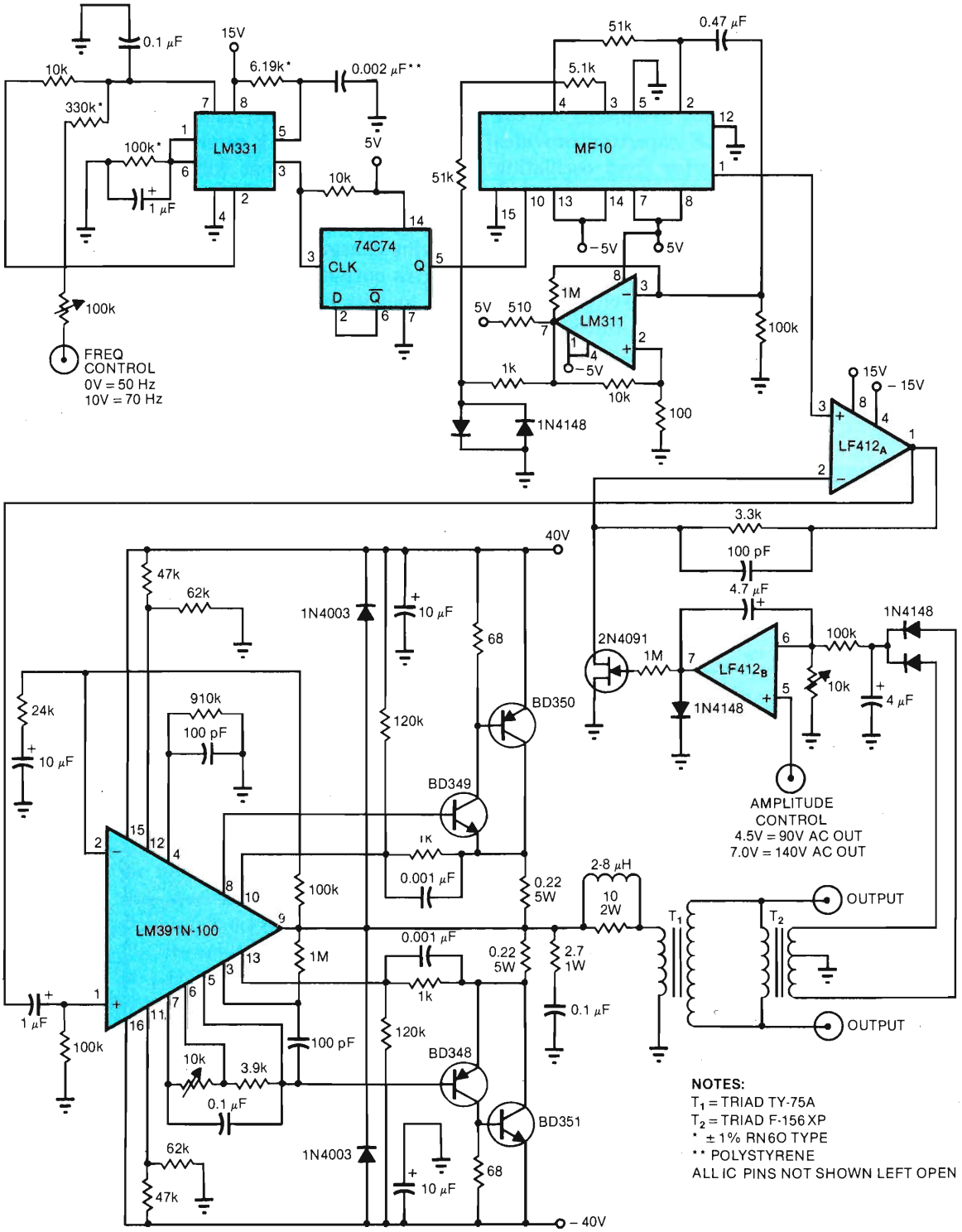


Fig 9—Test line-operated devices *with this variable-voltage and -frequency converter. From a 40V dc input, you can get 90 to 140V ac at 50 to 70 Hz.*

Use a flyback circuit to obtain high voltages

capacitor to a value high enough to cause the LM10 output to go LOW, thereby cutting off the oscillation.

In **Fig 6,** trace B shows the collector voltage of Q_1; trace A shows the converter's output voltage (ac coupled). Note that each time the output voltage drops a certain amount, the LM10 drives the oscillator, causing the output voltage to rise until it's sufficiently high to switch the LM10 to its LOW state.

The output load determines the frequency of the regulating action, and the 0.1-μF capacitor provides hysteresis, preventing the converter from oscillating around the trip point. Very low loading of the converter results in virtually zero oscillator ON time, while large loads cause the oscillator to run almost constantly (typical operating frequencies are between 0.1 and 40 Hz). The germanium rectifiers minimize voltage drop.

If you need a very high voltage, consider the flyback-type converter shown in **Fig 7.** It generates 200V (regulated) into a 500-μA load from a 5V supply and thus serves applications such as gas-discharge displays, piezoelectric transducers and strobe lamps. Half of the LM393 op amp ($LM393_A$) functions as a constant-width-output voltage-to-pulse-rate clock. The 0.1-μF/100-kΩ combination, together with the 2.5V from the LM10 op-amp/reference IC, fixes the output width at about 4 msec. The 100Ω/2.2-μF pair provides bypassing for the 2.5V reference, and the 0.1-μF/10-kΩ constant and the input voltage set clock frequency.

Each time $LM393_A$'s minus input charges above its plus input, its output goes LOW (**Fig 8,** trace A), drawing charge from both 0.1-μF capacitors. When the device's output is LOW, its minus input is clamped at 0.6V and its plus input (**Fig 8,** trace B) rises until it exceeds that level. Then the output goes HIGH, ending

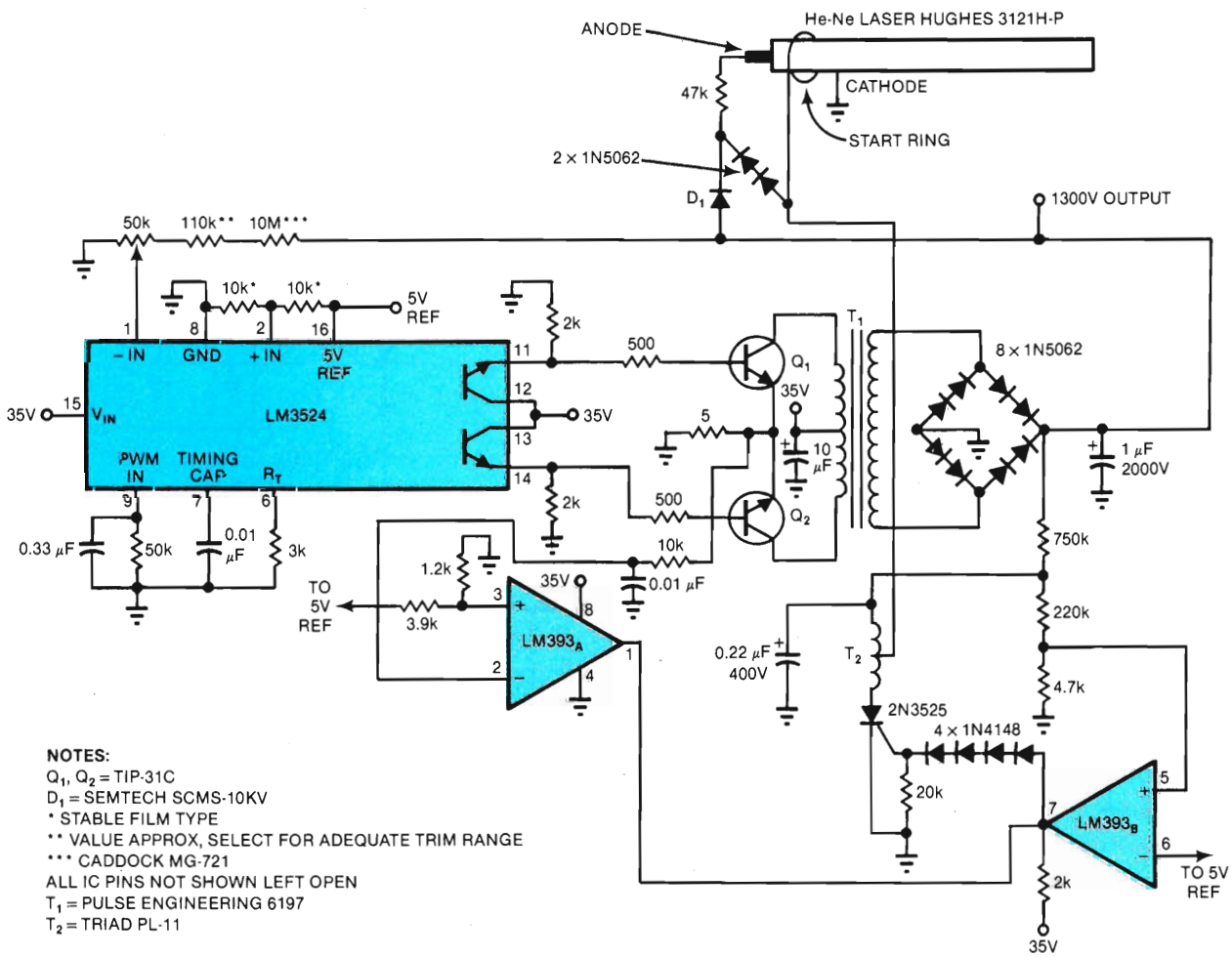


Fig 10—Start and run a laser *with this 35V to 1300V converter. It furnishes an 8000V pulse that repeats as often as needed until the laser starts.*

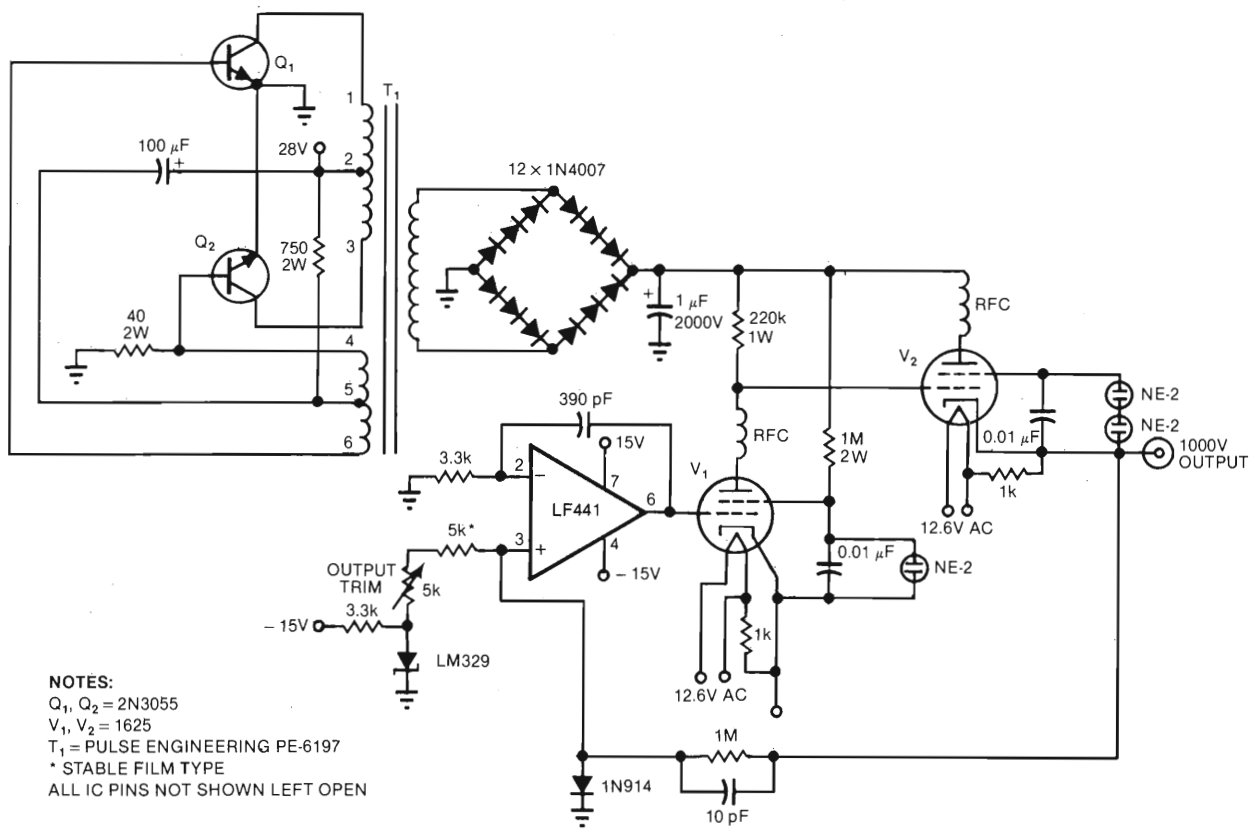


Fig 11—Using tried-and-true technology, *this ±15V to 1000V hybrid-semiconductor/vacuum-tube converter incorporates inexpensive components and is very forgiving of overloads.*

the timing cycle and reinitializing the entire process. The 1N914 diode prevents a differentiated positive response at LM393$_A$'s plus input, allowing the circuit to recover quickly for the next cycle.

LM393$_B$, meanwhile, inverts the clock's output and drives Q_1. When this op amp's output goes HIGH (**Fig 8**, trace C), Q_1 turns on, its collector current rises (**Fig 8**, trace D) and the 100-μH inductor stores energy. *(Ed Note: The current probe is ac coupled—the long tail is actually flat.)* When LM393$_B$'s output goes LOW, the magnetic field in the inductor collapses and Q_1's collector voltage rises to about 200V (**Fig 8**, trace E). This high-voltage spike gets clamped and stored by the 1N4004/1-μF combination at the circuit's output.

The LM10 compares a divided-down portion of the output with its 2.5V internal reference. The difference voltage at the LM10 output then closes the loop at LM393$_A$'s clock. The 10-MΩ/1-μF feedback components set loop gain and frequency compensation.

Vary voltage, frequency with ac line converter

If you must generate a variable-frequency and -amplitude ac supply from a 40V source, consider **Fig 9**'s circuit. This arrangement is ideal for testing 115V ac, 60-Hz line-powered loads for sensitivity to amplitude and frequency variations. The frequency of its sinusoidal output is voltage controllable from 50 to 90 Hz; output amplitude is also voltage controllable over a 90 to 140V ac range.

In the circuit, the LM331 V/F converter and flip flop form a voltage-controlled square-wave clock that drives the MF10 filter. That device, together with an LM311 comparator, forms a resonator that generates stable-amplitude sine outputs without using AGC circuitry. The MF10 operates as a Q-of-10 bandpass filter that rings at its resonant frequency in response to a step input. The LM311, upon receipt of this ringing signal, creates a square-wave input signal for the bandpass to regenerate the oscillation.

The bandpass output is the filtered fundamental frequency of a 50%-duty cycle square wave. The clock controls the filter's center frequency, in turn setting the oscillation frequency. The peak-to-peak swing of the MF10's square-wave input (defined by the back-to-

back diode clamps at the LM311 output) determines the circuit's output amplitude.

The LM331 is biased so that a 0 to 10V input yields a 50- to 70-Hz sine-wave output at the MF10. This output goes to $LF412_A$, whose output biases the LM391 circuit, a gain-of-5 power amplifier that drives step-up transformer T_1. A portion of T_1's output—fed back to $LF412_B$ via T_2 and its rectifier/filter network—gets compared at $LF412_B$ with the amplitude control voltage. $LF412_B$'s output then biases the 2N4091 FET, which controls $LF412_A$'s gain, closing the amplitude control loop.

This circuit achieves a fully isolated output because of the galvanic isolation provided by T_1 and T_2. It sources 10W of sine-wave power over a controllable range of 90 to 140V ac and 50 to 70 Hz.

Make a laser run with only 35V

A laser is a good example of a component that forms part of a larger system and has special voltage requirements. The He-Ne laser shown in **Fig 10,** for example, requires 1300V operating and an 8000V start pulse. You can meet both of these requirements by up-converting the system's 35V supply.

The LM3524 pulse-width-modulator IC, in conjunction with Q_1 and Q_2, drives T_1 to provide a stepped-up voltage. T_1's rectified and filtered output, via feedback to the LM3524, is a regulated 1300V. C_T and R_T set the 20-kHz switching frequency; the 50-kΩ/0.33-μF pair controls the loop's gain-rolloff characteristics. You trim the 1300V output (applied to the laser's anode) with the 50-kΩ Output Set potentiometer.

When you first apply power to the circuit, the 1300V is insufficient to start the laser; hence, very little current is drawn from the 1300V supply. The low supply current results in a small average current through Q_1 and Q_2, in turn resulting in a small voltage drop across the 50Ω emitter resistor. This voltage is below the threshold at $LM393_A$'s plus input, so the amplifier's open collector unclamps.

When the 0.22-μF capacitor at T_2 charges, the voltage at $LM393_B$'s plus input exceeds 5V, and its output goes HIGH, allowing gate current to flow into the SCR. The SCR then fires, dumping the 0.22-μF capacitor's energy through T_2, a flyback photoflash unit. This action causes an 8-kV spike to appear at the laser's start ring, normally causing gas breakdown and starting the laser. Diode steering prevents the spike from affecting the normal 1300V output.

When the laser starts, the Q_1-Q_2 emitter current increases enough so that $LM393_A$ is forced LOW, cutting off drive to the SCR and disabling the start circuitry. But if the laser does not start, $LM393_A$

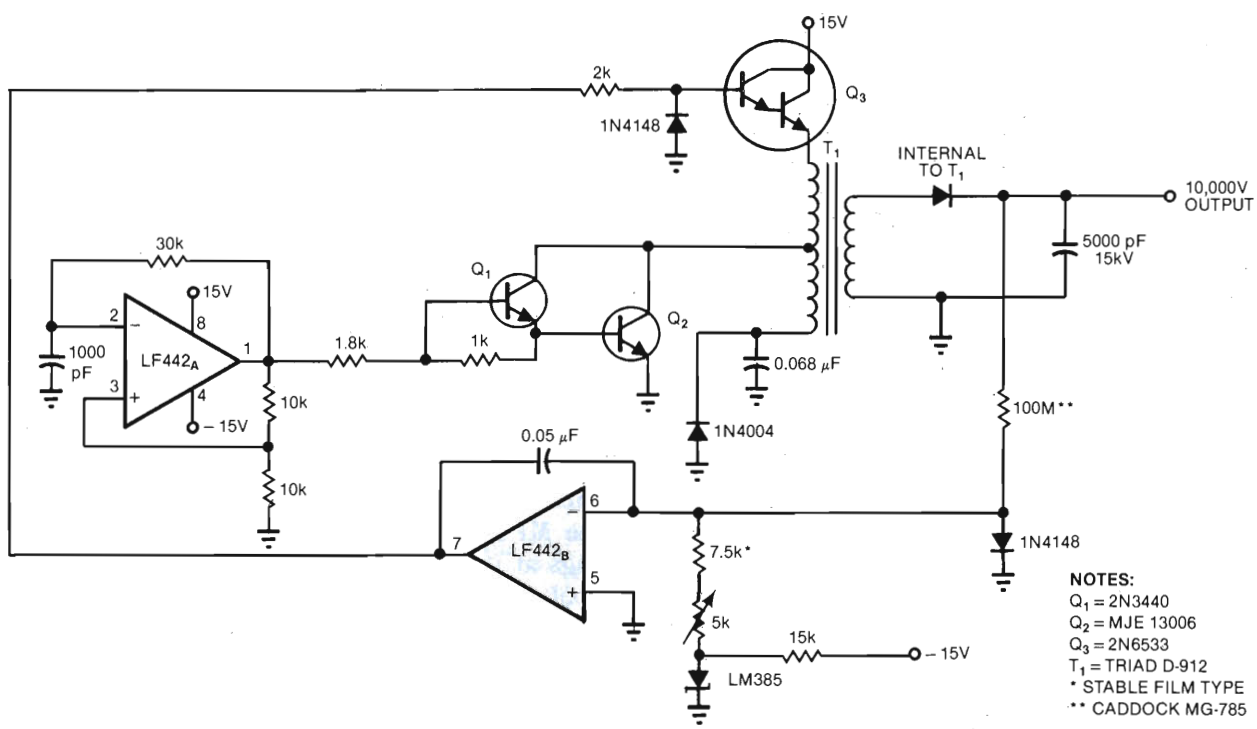


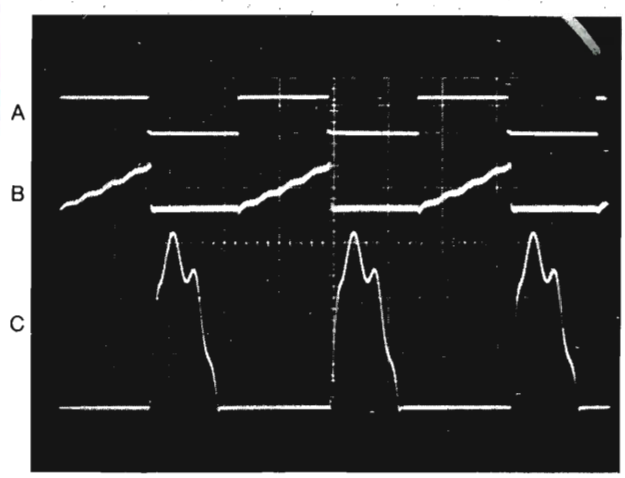
Fig 12—Accelerate electrons in a CRT *with this ±15V to 10-kV flyback-type converter; its servo loop ensures output stability.*

Meet lasers' special needs with a PWM IC

remains unclamped. When the 0.22-μF capacitor charges fully, $LM393_B$'s plus input exceeds 5V, and the SCR again drives T_2, producing the 8-kV start pulse. This action continues until the laser runs.

Don't write off vacuum tubes

Fig 10's laser supply achieves its 1300V output through servo control around a transformer. A potential problem with this type of converter is that its transient response is limited by the modulation frequency applied to the transformer. The best way to avoid the problem is to regulate with a series-pass



TRACE	VERTICAL	HORIZONTAL
A	50V/DIV	20 μSEC/DIV
B	4A/DIV	20 μSEC/DIV
C	50V/DIV	20 μSEC/DIV

Fig 13—Magnetic-field collapse *in* ***Fig 12****'s* T_1 *primary produces the high* Q_2 *collector-voltage pulses in trace C.*

element on the transformer's high-voltage side. But this action usually implies the use of expensive high-voltage transistors and a substantial amount of protective circuitry. **Fig 11** shows a converter that deals with these problems. It's inexpensive, provides the fast transient response of a series regulator and requires no output protection. Moreover, it withstands short circuits and output-current or -voltage reversals arising from reactive loads.

The self-exciting dc/dc converter composed of T_1, Q_1, Q_2 and their associated components generates the unregulated high voltage from a 28V supply. This converter's rectified and filtered output is applied to the plates of the two 1625 vacuum tubes, which are configured in a common-cathode-driven cathode-

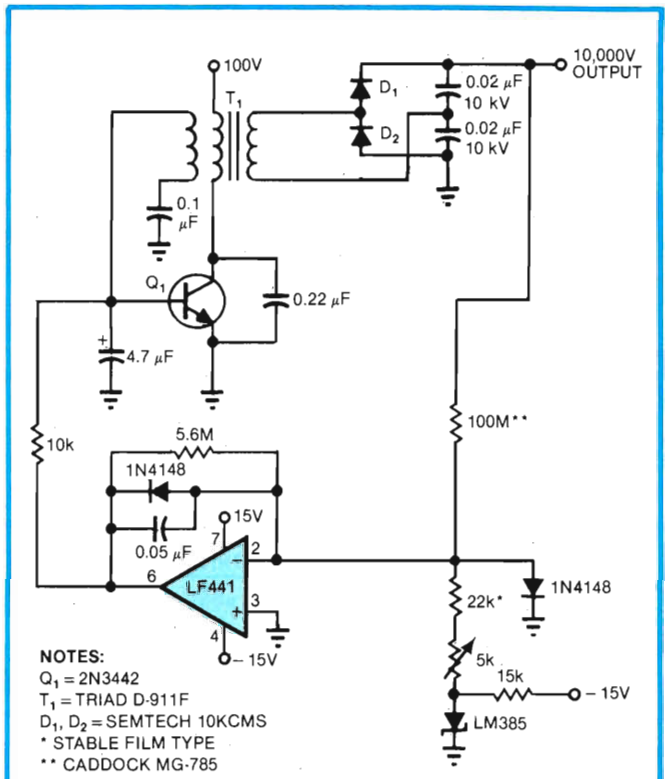


Fig 14—Using sinusoidal signals, *this converter supplies 10 kV with no radiated noise or spikiness.*

follower arrangement, with NE-2 neon-lamp screen-to-cathode clamps. Feedback from V_2 to the LF441 provides overall loop stabilization. The 390-pF/3.3-kΩ pair provides local rolloff at the LF441; overall compensation comes from the 10-pF/1-MΩ network. The 1N914 prevents capacitively coupled transients from appearing at the LF441's input.

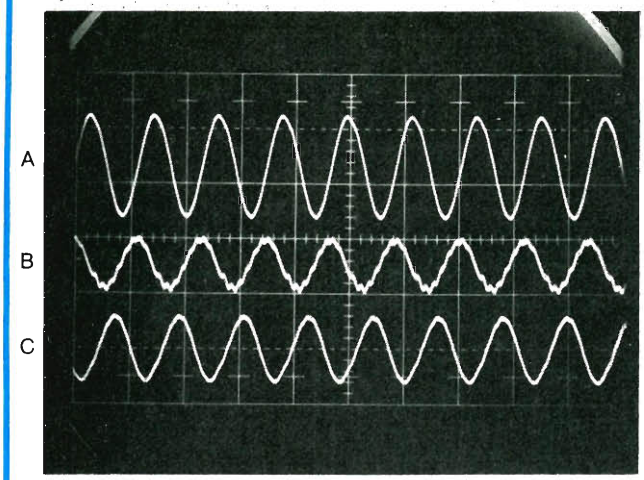
Set the output voltage with the 5-kΩ potentiometer at the LM329 reference. The power-handling capability of T_1 limits the circuit's output to 10W at 1000V—a chore that V_2 can perform effortlessly. If you anticipate extended (greater than 5 min) short circuits at the output, consider fusing V_2's plate circuit.

Multiply ±15V for voltage-hungry CRTs

In data-terminal designs, you must often convert the supply rails to the high voltage needed for CRT electron-beam acceleration. You can use a flyback approach for this task, but for more demanding applications (such as oscilloscopes), you might have to use a sine-wave conversion technique. So consider examples of conversion circuits that use each method.

In **Fig 12**'s flyback circuit, $LF442_A$ functions as an oscillator whose output (**Fig 13,** trace A) drives the Q_1-Q_2 Darlington pair. When the output is HIGH, Q_1 and Q_2 conduct and the current through T_1's primary

Use vacuum tubes for a low-cost high-voltage supply



TRACE	VERTICAL	HORIZONTAL
A	100V/DIV	50 μSEC/DIV
B	5A/DIV	50 μSEC/DIV
C	100 mV/DIV (AC COUPLED)	50 μSEC/DIV

Fig 15—The linear nature *of* ***Fig 14****'s converter is evident in this scope photo.*

builds up (**Fig 13,** trace B). When $LF442_A$ goes LOW, however, the field in T_1's primary collapses and a large flyback voltage appears at Q_2's collector (**Fig 13,** trace C). This field collapse also appears at T_1's secondary and produces a very-high-voltage output, which is rectified and filtered and fed back to $LF442_B$ via a divider. $LF442_B$'s output then servo-controls Q_3, which determines the amount of drive available to T_1. The 0.05-μF capacitor provides stable loop compensation; the LM385 and the 5-kΩ pot set the output voltage.

Although effective, this circuit produces unavoidable radiated noise and supply spiking—which some sensitive data terminals and oscilloscopes can't tolerate. **Fig 14**'s sine-wave-based high-voltage converter eliminates these problems.

When you apply power to this circuit, the LM385 reference pulls the LF441's minus input LOW, causing the LF441's output to rise. This action in turn causes Q_1's collector voltage to drop (**Fig 15,** trace A) and its collector current to rise (**Fig 15,** trace B). Concurrently, the 0.1-μF capacitor in T_1's feedback winding charges to a negative voltage. When the current in T_1 stops building, T_1's feedback winding pulls Q_1's base negative (**Fig 15,** trace C), cutting off Q_1 and causing its collector voltage to rise.

When the voltage on the 0.1-μF capacitor becomes positive, Q_1 starts to conduct, its collector voltage drops and the cycle repeats. The 0.22- and 4.7-μF capacitors provide stabilization, and the high-voltage output is current-summed with the LM385's negative reference current at the LF441 servo amplifier.

The LF441's output servo-controls the drive to Q_1,

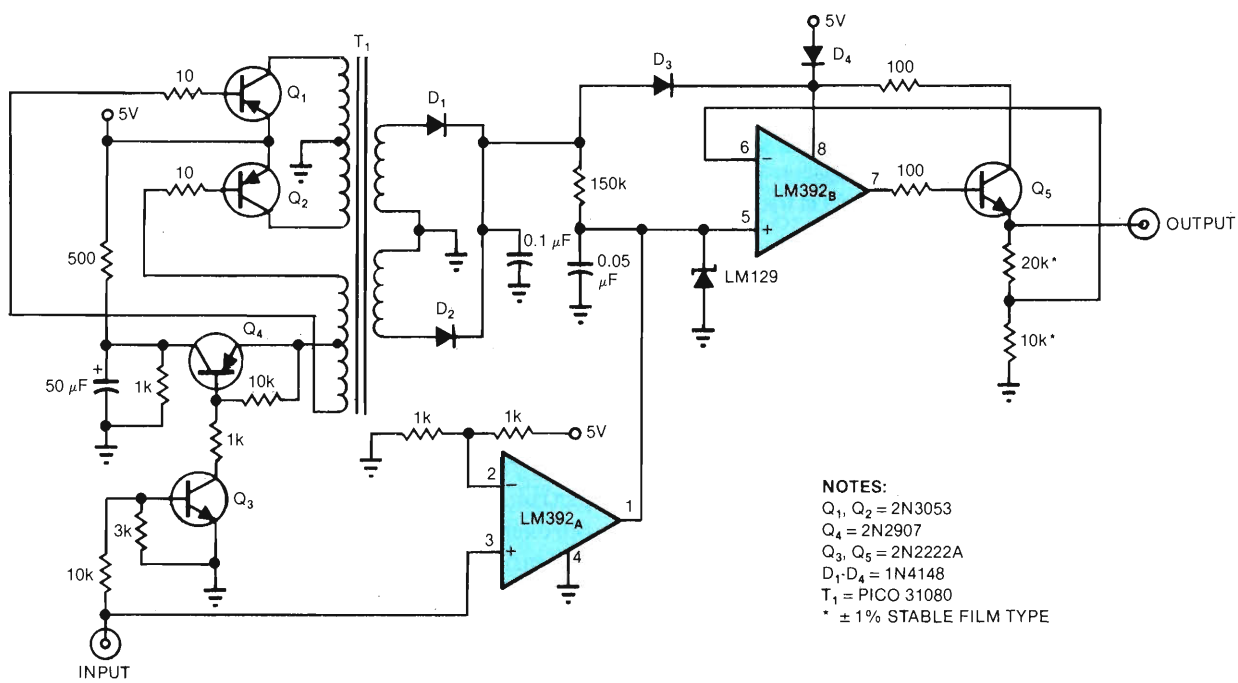


Fig 16—Memories are made of this—*a converter that supplies the 21V pulses for EEPROM programming. It achieves controlled rise time; you determine the pulse's width with a TTL command.*

closing the feedback loop around the transformer. Because the transformer isn't used in the flyback mode, the voltage step-up ratio is smaller than in **Fig 12**'s design, so you need higher initial input voltages. Alternatively, you could use a voltage-doubler network at the transformer output.

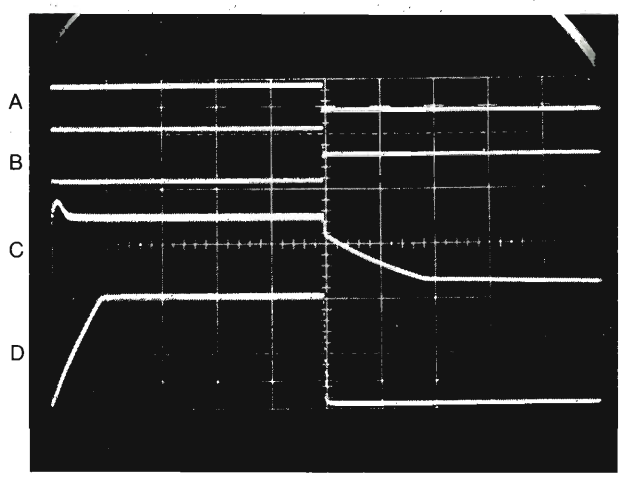
An easy way to power memory programming

What about the voltage required by programmable memories? Widely used EEPROM types such as the 2816 require controlled-rise-time 21V pulses for programming. **Fig 16** shows a converter that generates the necessary high-voltage pulses from the 5V rail.

T_1, in conjunction with Q_1 and Q_2, forms a self-driven 5 to 30V dc/dc converter. Q_3 and Q_4 serve as a strobe for this converter, allowing it to draw power and run only when a TTL signal is present at the circuit's input. When you apply a signal to the input (**Fig 17,** trace A), the Q_3-Q_4 pair conducts, biasing Q_1 and Q_2 so the converter runs (Q_2's collector waveform appears in **Fig 17,** trace B). The converter's output (**Fig 17,** trace C) is very lightly filtered by the 0.1-μF capacitor, allowing it to rise quickly. This output charges the 0.05-μF/150-kΩ combination.

The gain-of-3 $LM392_B$ amplifies the 0.05-μF capacitor voltage; Q_5 serves as an output-current booster. As the 0.05-μF capacitor charges, Q_5's emitter voltage rises, providing the leading edge of the programming pulse (**Fig 17,** trace D). When the capacitor voltage reaches 7V, the LM129 clamps, charging ceases and the output remains at 21V.

When you switch the TTL input pulse LOW, the $LM392_A$'s open-collector output clamps LOW, discharging the 0.05-μF capacitor and readying the circuit for the next pulse. You can satisfy any EEPROM's programming requirement by varying the gain of $LM392_B$, the time constant at its input or the zener clamp across the 0.05-μF capacitor. **EDN**



TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	2 mSEC/DIV
B	10V/DIV	2 mSEC/DIV
C	20V/DIV	2 mSEC/DIV
D	10V/DIV	2 mSEC/DIV

Fig 17—The programming pulse *of* ***Fig 16****'s circuit appears in trace D. Note the cleanly rising leading edge.*

Author's biography

Jim Williams, now a consultant, was applications manager in National Semiconductor's Linear Applications Group (Santa Clara, CA), specializing in analog-circuit and instrumentation development, when he wrote this article. Before joining the firm, he served as a consultant at Arthur D Little Inc and directed the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art and collecting antique scientific instruments in his spare time.

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Article Interest Quotient (Circle One)
High **476** ***Medium*** **477** ***Low*** **478**

Try a different configuration

Dear Editor:
As much as I appreciated Jim Williams's article on current-source circuits (EDN, September 1, pg 169), I feel that some errors and omissions need rectifying. Jim failed to alert users of the circuits detailed in **Figs** 3 and 4 to the errors arising from changes in transis-

Continued on pg 40

tor h_{FE} with temperature; it's much better to use an FET for Q_1 in **Fig 3** and Q_2 and Q_3 in **Fig 4**. In addition, the circuit in **Fig 5** exhibits a large time-constant increase in charging current when Q_3 is turned off, because of thermal effects in Q_2.

My main criticism, however, pertains to **Fig 9**. Apart from the obvious pinout errors and misconnections to the LM3524, VMOS transistors and LM363, what astounds me is the use of a precision high-CMRR instrumentation amplifier (such as the LM363) with such an appalling input circuit. At least Jim might have consulted National Semiconductor's *Linear Applications Handbook AN29-14* and reminded readers of the need to match the 60-kΩ and 1-MΩ resistors. This circuit's output resistance could be as low as 2700Ω—hardly a 200V-compliance current source!

An improved current-monitoring configuration would include the 100Ω sampling resistor in the negative output from the bridge rectifier and smoothing capacitor. It would eliminate any common-mode effects arising from load-resistance changes. Provided the input signal could be changed to 0 to −5V, the feedback from the 100Ω resistor could be directly connected to the LF411.

Yours truly,
Peter M Clare
Principal Electronic Engineer
Bell & Howell Ltd
Basingstoke, Hampshire, UK

Author's reply

It's true that h_{FE} vs temperature will affect operation, but in many (most) applications, the relatively small I_C/I_B effect is not objectionable—to attain the most precise operation, an FET or FET/transistor combination is a better refinement of the basic circuits.

Quite frankly, Mr Clare's current-sensing scheme, which uses the fully floating transformer secondary, is a vastly superior method—even if the 163's input resistors are ratio matched (which I neglected to mention). I'm a little embarrased that I didn't see it myself, and I unhesitatingly recommend it over my original approach. LM163s are cheap—but not *that* cheap.

Sincerely,
Jim Williams
Palo Alto, CA

Use comparator ICs in new and useful ways

You can use the unique differential-input/digital-output characteristics of comparators to implement a wide range of circuit functions.

Jim Williams, National Semiconductor Corp

Perhaps the most underrated and underutilized of monolithic ICs, comparators are among the most flexible and universally applicable components in your design arsenal. With their differential linear inputs and very-fast-switching digital outputs, these devices can help you implement unusual circuit functions at favorable cost and low component count compared with other approaches. Examples ranging from a shaft-angle encoder to a V/F converter show how you can exploit comparators' unique abilities.

Variable capacitor makes shaft-angle encoder

If, for example, you need to convert a shaft angle to a digital bit stream, you can employ **Fig 1**'s comparator-

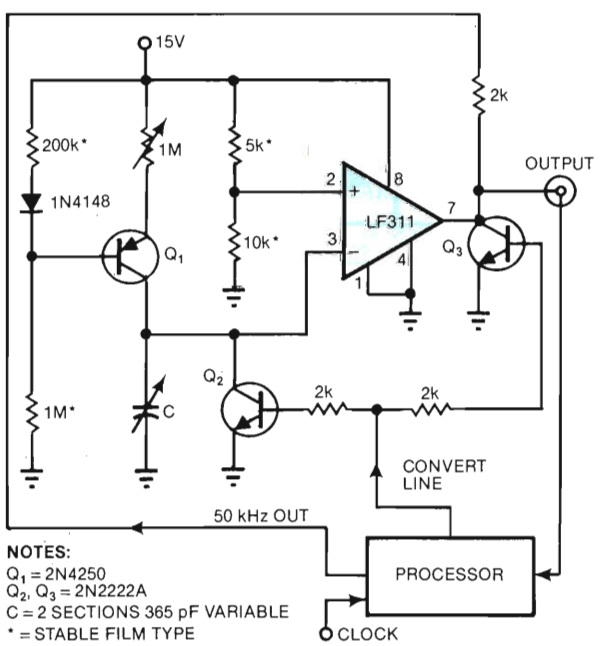
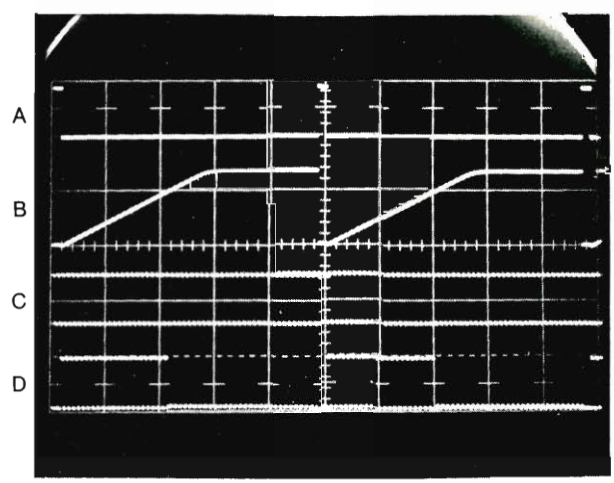


Fig 1—Employing a variable capacitor and a comparator, *a single-supply circuit yields a pulse burst—triggered by a Convert-line HIGH-to-LOW transition—whose duration is a ±0.1% linear function of the capacitor's shaft angle.*



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	200 μSEC/DIV
B	10V/DIV	200 μSEC/DIV
C	5V/DIV	200 μSEC/DIV
D	5V/DIV	200 μSEC/DIV

Fig 2—When the linear charging ramp *(trace B) of* ***Fig 1****'s variable capacitor reaches 10V, it signals a comparator to shut off the trace D output pulse burst.*

Obtain shaft-angle readings with a comparator-based circuit

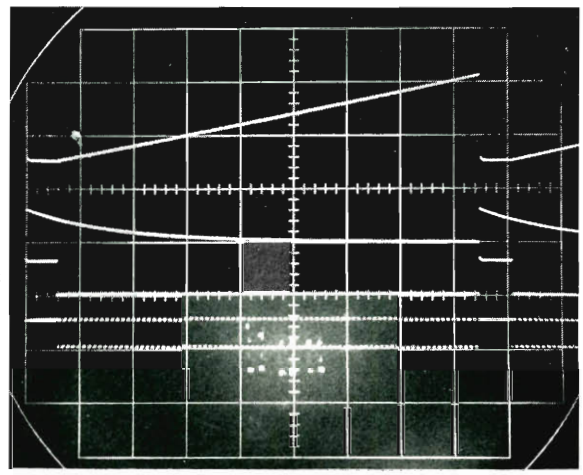
based circuit. It uses a standard AM-radio dual 365-pF variable air capacitor to generate a controlling-processor-triggered constant-frequency pulse burst. The burst's duration—or the number of pulses it contains—indicates shaft position to within a ±0.1% typ accuracy. Moreover, the capacitor has essentially infinite life—unlike potentiometers, which can wear quickly and require frequent replacement in high-usage applications such as video arcade games.

In operation, transistor Q_1 and associated components form a ground-referred current source that linearly charges the variable capacitor. When the controlling processor needs a shaft-angle conversion, it drives the Convert line HIGH (**Fig 2,** trace A), turning Q_2 on and discharging the capacitor. Concurrently, Q_3 turns on, forcing the circuit output to zero.

To continue the conversion, the processor pulls the Convert line LOW, and the constant-current-source-driven capacitor voltage begins to ramp linearly toward the 15V supply (**Fig 2,** trace B). This Convert-line HIGH-to-LOW transition simultaneously unclamps the LF311's output, thus triggering a pulse burst by causing the processor's clock (**Fig 2,** trace C) to appear as a serial bit stream at the output (**Fig 2,** trace D).

The circuit continues to transmit this bit stream until the capacitor's voltage crosses the level established by the 5-kΩ/10-kΩ resistor divider; at that point the comparator output clamps, inhibiting pulses. Note that each Convert-line HIGH-to-LOW transition initiates an updated bit-stream output.

The circuit is insensitive to supply shifts because the resistor-divider trip point and the current-source reference are ratiometrically related. The FET-input comparator does not appreciably load other circuit components, so linearity is excellent. With a standard variable air capacitor (General Radio Type 722) substi-



TRACE	VERTICAL	HORIZONTAL
A	0.5V/DIV	1 mSEC/DIV
B	0.1V/DIV	1 mSEC/DIV
C	5V/DIV	1 mSEC/DIV
D	10V/DIV	1 mSEC/DIV

Fig 4—The number of pulses *between bit-stream gaps in the* ***Fig 3*** *circuit's output (trace D) is a linear function of temperature.*

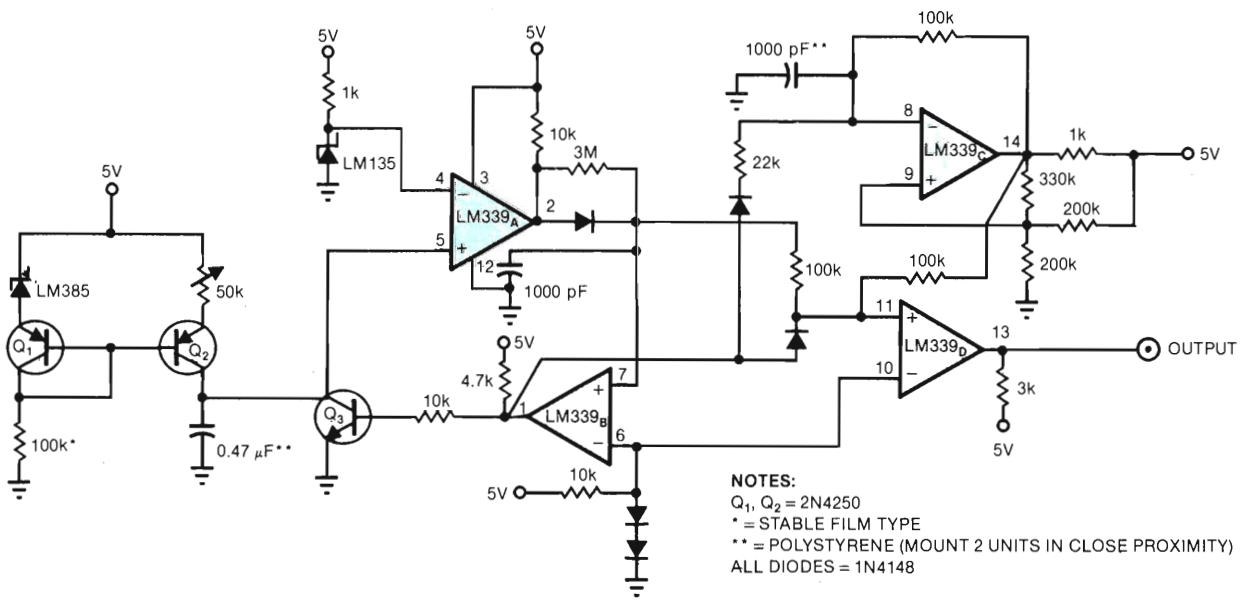


Fig 3—Furnishing an output pulse count proportional to temperature, *this LM135-sensor-based circuit requires no external clock. A gap in the output bit stream indicates the end of conversion.*

tuted for the dual 365-pF unit, linearity is well within ±0.1%. Use the 1-MΩ potentiometer to set the desired scale factor.

Convert temperatures to bit streams

Fig 3 shows another serial-output converter, one that requires only a 5V supply. Generating this circuit's output, which indicates the temperature at the LM135 sensor, doesn't require an external command—instead, the circuit clocks itself continuously and inserts gaps in the output stream to indicate the end of one conversion and the beginning of a new one.

Q_1 and Q_2 form a temperature-compensated current source whose output is referenced to the LM385. Q_2's collector current linearly charges the 0.47-μF capacitor (**Fig 4**, trace A) until the ramp voltage exceeds the LM135's voltage. Then, $LM339_A$'s output goes HIGH, dumping charge into the 1000-pF capacitor and forcing $LM339_B$'s positive input (**Fig 4**, trace B) and output (**Fig 4**, trace C) HIGH. This action turns on Q_3, resetting the ramp capacitor.

The 1000-pF capacitor can discharge only through the 3-MΩ resistor paralleling the diode at $LM339_A$'s pin 2. Therefore, the waveform at $LM339_B$'s positive input decays slowly, and the ramp capacitor stays off for an extended period of time. When the 1000-pF capacitor's

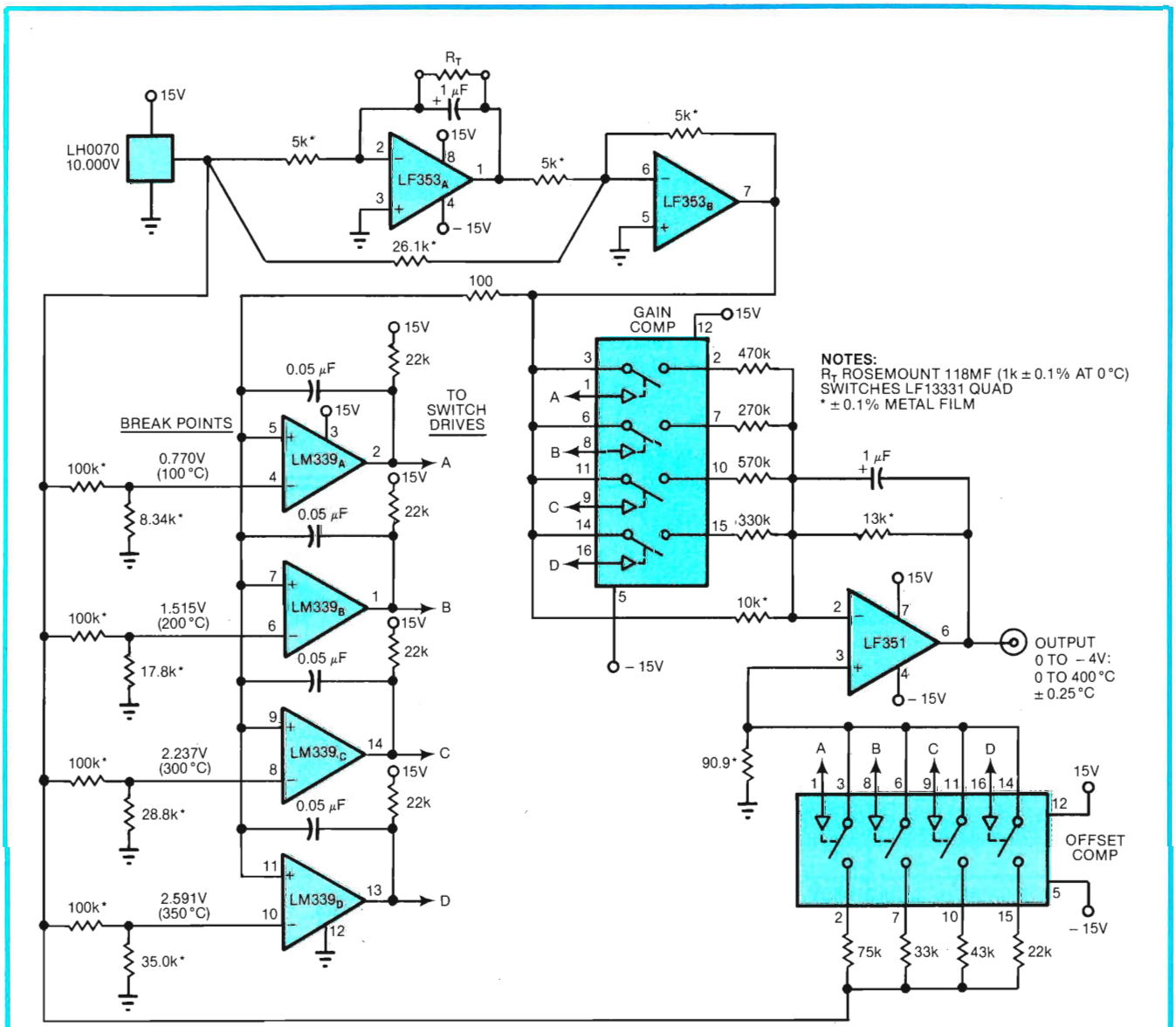


Fig 5—Using breakpoint corrections *at four temperatures and requiring no trimming, this circuit compensates for a platinum RTD sensor's nonlinearity.*

Temperature-sensing scheme uses a 4-comparator IC

voltage finally decays below the 2-diode-drop value at $LM339_B$'s negative input, Q_3 turns off, ramping begins and the cycle repeats.

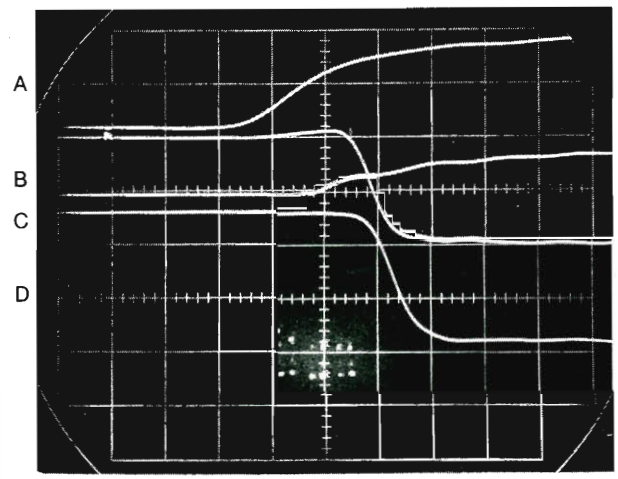
The oscillation frequency varies inversely with the LM135's output voltage. The ramping time, however, is directly—and linearly—proportional to the LM135's output. While the ramp is running, $LM339_B$'s output is LOW, and $LM339_C$, which functions as a 10-kHz clock, biases $LM339_D$, providing the circuit's output. When $LM339_A$'s output goes HIGH, the 100-kΩ resistor path from $LM339_A$ to $LM339_D$'s positive input in turn forces $LM339_D$'s output HIGH (**Fig 4**, trace D).

Reinforcing feedback results when $LM339_B$'s output goes HIGH and applies bias through the diode path to $LM339_D$'s positive input. This condition lasts until the 1000-pF-capacitor voltage decays to a value sufficiently low for the cycle to repeat. The 22-kΩ resistor/diode path from $LM339_B$'s output to $LM339_C$'s negative input synchronizes the 10-kHz clock to the circuit's ramp-reset sequence, thereby averting a ±1-count uncertainty in the output data.

A monitoring processor can use the gap in the circuit's output bit stream to synchronize itself to the temperature data. To calibrate the circuit, measure the voltage at the LM135 and adjust the 50-kΩ potentiometer so that the number of bits in each burst relates numerically to this voltage (eg, 2.98V=298 bits).

Linearize a platinum RTD with comparators

If, instead of an LM135 sensor, you're using platinum RTDs (resistance temperature detectors) to take advantage of their extremely wide operating-temperature ranges and their long-term stability under adverse environmental conditions, consider the **Fig 5** linearizing



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	10 nSEC/DIV
B	50 mA/DIV	10 nSEC/DIV
C	5V/DIV	10 nSEC/DIV
D	10V/DIV	10 nSEC/DIV

Fig 7—The fast shutdown action *of* ***Fig 6****'s circuit results in power cutoff (trace D) within 30 nsec of an overload occurrence. Note the beginning of the overload (trace B) at about four horizontal divisions from the left of the screen.*

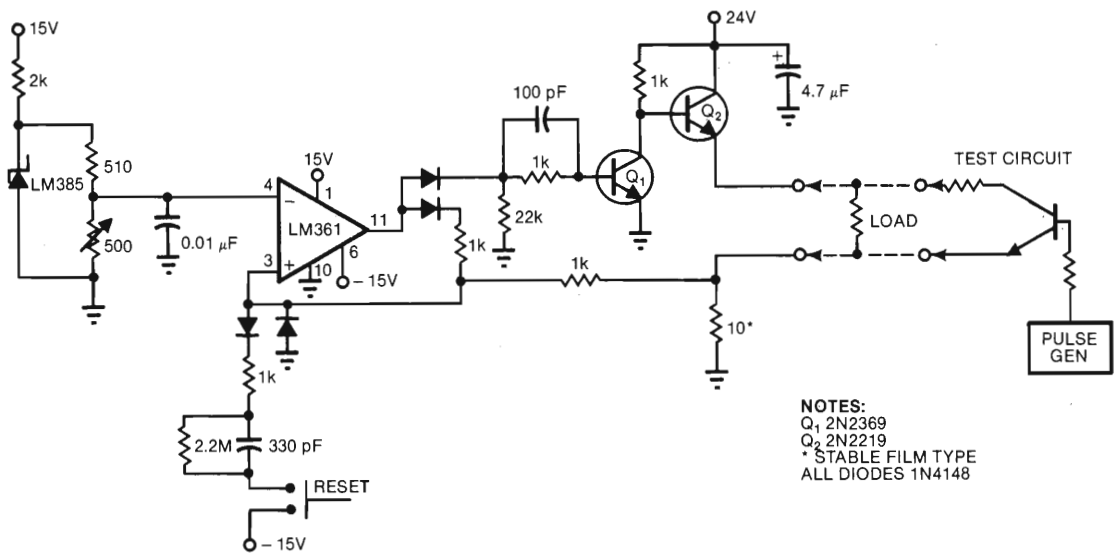


Fig 6—A fast-acting power-shutdown circuit can protect sensitive components. *The one shown here employs a comparator and a 10Ω sense resistor to establish a 100-mA trip point.*

circuit. It overcomes an RTD's inherent nonlinearity (>6° error from 0 to 400°C) by using an LM339 quad comparator to apply a 4-section breakpoint correction. In contrast to other RTD-linearizing circuits, **Fig 5**'s design needs no calibration.

Because of the RTD sensor's positive temperature coefficient, op amp $LF353_A$'s output rises with increasing temperature. Summing the output with a constant current at $LF353_B$'s negative input results in a 0V $LF353_B$ output at 0°C; this output increases as a direct but nonlinear function of the RTD's temperature.

$LF353_B$'s temperature-dependent output drives the positive inputs of the LM339 comparators and provides the input to the output gain stage, $LF351_C$. The threshold voltages at the LM339 negative inputs cause the respective comparators to switch at the $LM353_B$ voltages corresponding to 100, 200, 300 and 350°C.

When a comparator output switches HIGH, it switches in gain- and offset-changing resistors via the LF13331 JFET switches. The four slight gain adjustments compensate for the RTD's nonlinearity, and the introduced offsets ensure a monotonic increase in output as temperature rises. The 0.05-μF capacitors at the LM339 outputs prevent chattering at the trip points; the 1-μF capacitor in the LF351's feedback loop eliminates transient switching signals from the output.

If you use the **Fig 5** circuit values and RTD sensor, you can obtain ±0.15°C accuracy over 0 to 400°C with no trimming of any kind.

Do you have need to protect expensive components in a system—perhaps, for example, during the final phases of trimming and calibration? If so, consider the **Fig 6** circuit—it shuts down power within 30 nsec of an overload occurrence (in this case, for load currents greater than 100 mA).

When the current is less than or equal to 100 mA, the LM361's output is LOW, Q_1 is OFF and emitter follower

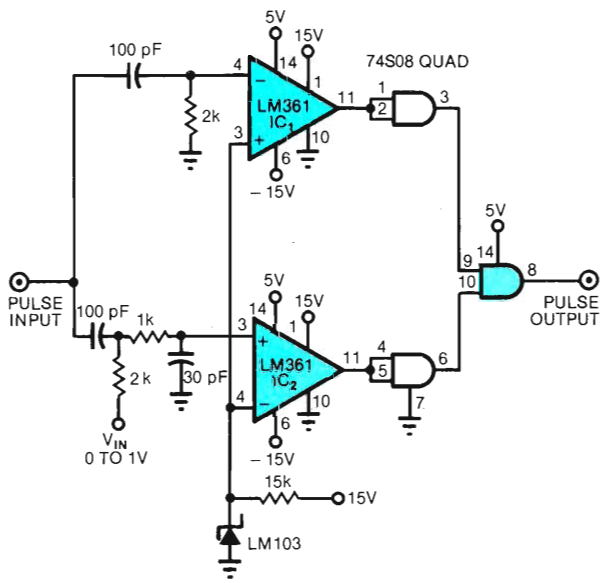
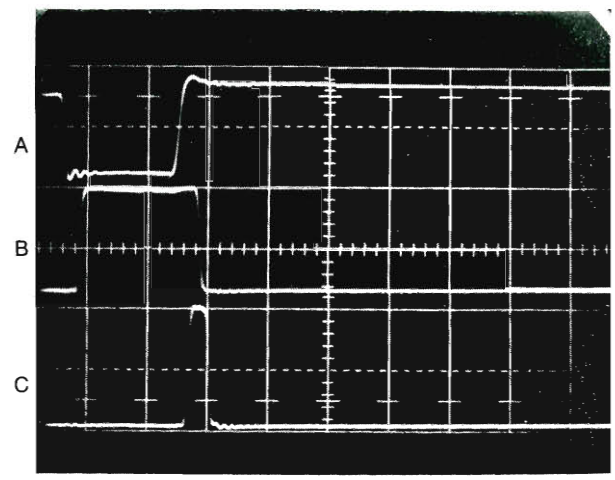
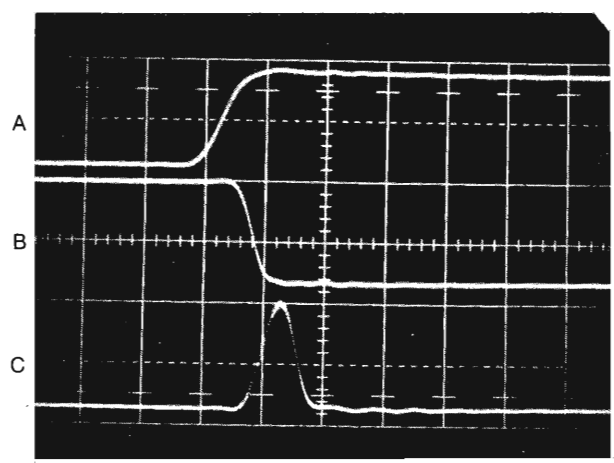


Fig 8—A circuit based on two comparators *and an AND gate can generate 6-nsec-wide pulses with 2-nsec rise and fall times. The V_{IN} level determines pulse width.*



TRACE	VERTICAL	HORIZONTAL
A	2V/DIV	200 nSEC/DIV
B	2V/DIV	200 nSEC/DIV
C	2V/DIV	200 nSEC/DIV



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	10 nSEC/DIV
B	5V/DIV	10 nSEC/DIV
C	5V/DIV	10 nSEC/DIV

Fig 9—The ANDing action *of* ***Fig 8****'s 74S08 gate yields a narrow pulse (**(a)**, trace C) because of time displacement between comparator outputs (traces A and B). The traces in **(b)** show the signals at these same circuit nodes for a 100-mV V_{IN}.*

Comparator high-speed switching eases pulse-generation tasks

Q_2 sources power to the load and the 10Ω sense resistor. When an overload occurs (in this case via the test circuit, whose output appears in **Fig 7,** trace A), the current through the 10Ω sense resistor begins to increase. (Note the slight load-current rise in **Fig 7,** trace B.)

This rise in current produces a corresponding voltage increase at the LM361's positive input. The comparator's output then rises (**Fig 7,** trace C) and drives Q_1 through a heavy feedforward network. Although this network degrades the LM361's output rise time somewhat, Q_1 responds very quickly and clamps Q_2's base to ground, causing load voltage (**Fig 7,** trace D) to immediately decay to zero.

As noted, the total elapsed time from overload onset to circuit shutdown is 30 nsec. Once the shutdown has occurred, the resistor-diode network from the LM361's pin 11 to pin 3 provides latching feedback to keep power

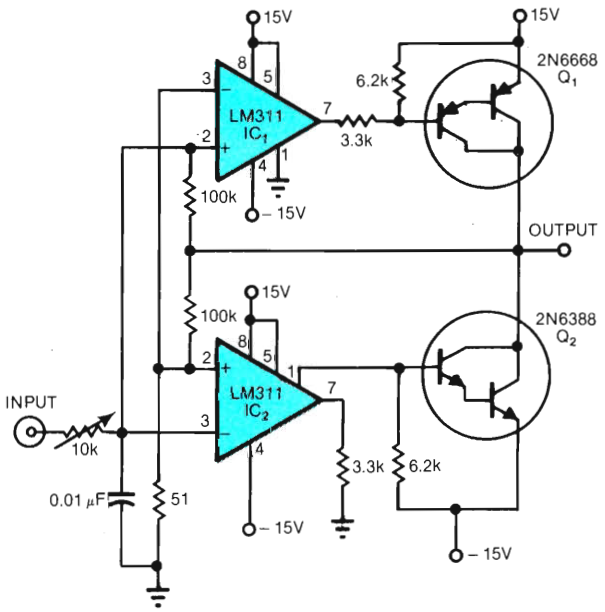


Fig 10—A comparator-based 400-Hz switching amplifier *is inexpensive, requires few components and can provide a 6A output.*

off the load. The reset pushbutton causes a negative spike to appear at the LM361's positive input, breaking the latching feedback and allowing the loop to function normally again. Use the 500Ω potentiometer to set the trip point at the desired value (for the **Fig 6** circuit, 1V=100 mA).

Comparators make 2-nsec pulse generator

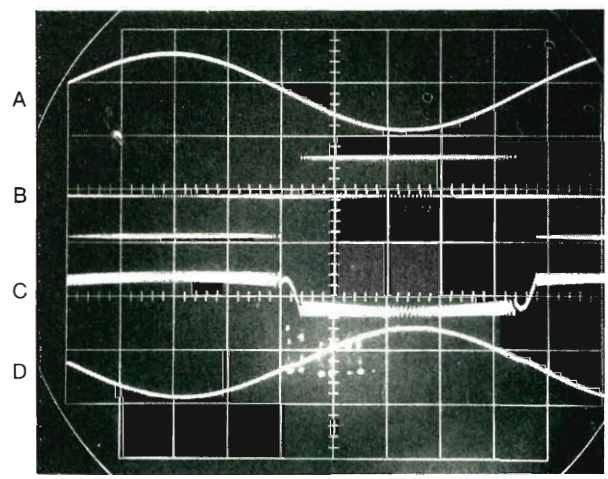
Similarly benefiting from the LM361's high-speed performance, the **Fig 8** ultra-high-speed pulse generator furnishes voltage-controllable pulse widths. Its differentiator networks generate a pair of pulses with slightly different durations; the comparators and a Schottky TTL gate extract the difference between two widths and present it as a single fast-rise-time pulse at the circuit output.

When you apply a positive input pulse, the two 100-pF/2-kΩ differentiator networks yield positive outputs. When the positive-going steps exceed the 2V threshold established by the LM103, both LM361s switch output states. For a 0V control input, the differentiator networks and the LM361s respond simultaneously, and both output transitions line up.

As you increase the control voltage, however, the spike produced by IC_2's differentiator arrives at the 2V threshold earlier than does that of IC_1. IC_2 also normally takes longer to decay through the 2V threshold, appearing to lead to a situation in which IC_2's output would remain HIGH longer and switch earlier than would IC_1's.

IC_2's 30-pF/1-kΩ network, however, provides a delay that shifts the IC_2 output so that IC_1's leading and trailing edges occur first (**Fig 9a,** traces A and B). The length of time between the comparator outputs' edges depends on the input control voltage.

For the **Fig 8** circuit, a 0 to 1V control range produces a trailing-edge timing difference of 0 to 100 nsec. The



TRACE	VERTICAL	HORIZONTAL
A	2V/DIV	200 μSEC/DIV
B	20V/DIV	200 μSEC/DIV
C	100 mV/DIV	200 μSEC/DIV
D	20V/DIV	200 μSEC/DIV

Fig 11—The power envelope *of the* ***Fig 10*** *switching amplifier's output (trace D) is sinusoidal when the circuit is driven by a sine-wave input (trace A). Note the high-frequency charging and discharging of the circuit's 0.01-μF capacitor (trace C).*

Comparator circuit handles frequency-division chores

DM74S08 ANDs the two comparators' outputs to obtain the single-pulse circuit output (**Fig 9a,** trace C).

The gate and comparator switching speeds limit the minimum pulse width to 6 nsec; rise and fall times are approximately 2 nsec. **Fig 9b** shows an example of the high-speed operation that the **Fig 8** circuit can achieve (control input=100 mV). Traces A and B represent IC_1 and IC_2 outputs, respectively; trace C is the circuit's output pulse.

If you need a simple, inexpensive 400-Hz amplifier, consider the **Fig 10** circuit. It uses ±15V supplies,

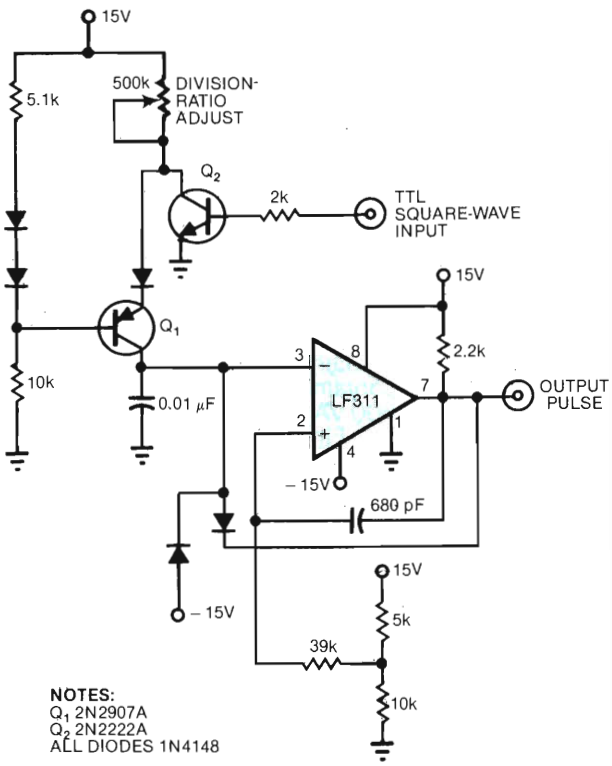


Fig 12—Divide and conquer *your frequency-reduction problems with this synchronous circuit. You can vary the division ratio over a 1:1,000,000 range.*

provides full bipolar swing and has a 1.5-kHz full-power bandwidth with a 6A pk output capability.

If the input voltage is negative, IC_2's output is LOW (note that IC_2 operates in an emitter-follower mode, so its output is in phase with its negative input), cutting Q_2 off. Concurrently, IC_1's output goes LOW, turning Q_1 on and thereby driving the load and the 100-kΩ resistors connected to the comparators' positive inputs. This feedback produces a small voltage at IC_1's negative input.

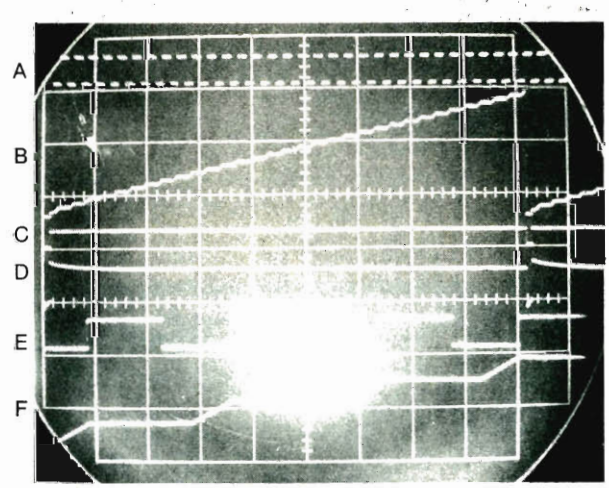
When the 0.01-μF capacitor charges to a level high enough to offset the negative input, IC_1's output changes state, turning Q_1 off. At this point, the input draws current from the capacitor, forcing IC_1's positive input to a lower state and consequently driving IC_1's output LOW again, turning Q_1 on.

The switching action occurs continuously; repetition rate depends on the input voltage. For positive inputs, IC_2 and Q_2 perform similar action. To avoid cross-current conduction in the output transistors, tie the comparators' offset-adjust terminals to the 15V supply.

Fig 11 trace B shows the circuit output resulting from the trace A input; the trace C waveform represents current flow in and out of the capacitor. (Think of the IC_2 pin 3 point as a digitally driven summing junction.) Trace D is a lightly filtered version of trace B; it clearly shows that the circuit output has a sinusoidal power envelope. You can vary the amplifier gain with the 10-kΩ input potentiometer.

Divide frequencies over a 1:1,000,000 range

Using the **Fig 12** circuit, you can divide a frequency over a $1:10^6$ range, adjustable via a single potentiometer. Moreover, the output frequency you obtain is synchronously related to the input frequency. You can use this circuit to obtain simultaneous oscilloscope observations of low-frequency signals and the fast clock



TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	100 μSEC/DIV
B	5V/DIV	100 μSEC/DIV
C	50V/DIV	100 μSEC/DIV
D	20V/DIV	100 μSEC/DIV
E	10V/DIV	10 μSEC/DIV
F	0.2V/DIV	10 μSEC/DIV

Fig 13—Using a step-charging technique *that results in the trace B capacitor voltage,* ***Fig 12****'s circuit yields an output frequency proportional to and synchronized with an input signal's frequency (trace A). In the example shown here, the output (trace C) contains a pulse after 32 input pulses.*

Manipulate pulses with comparator-based circuits

from which they're derived or to synchronously trigger an A/D converter at a variable rate.

The circuit functions by step-charging a capacitor with a switched current source and using a comparator to determine when to reset the capacitor. **Fig 13,** trace B, shows the step-charging waveform; each time the pulse input (**Fig 13,** trace A) goes LOW, a current-source pulse causes a capacitor-voltage positive step. You can control the step height—and therefore the division ratio—with the 50-kΩ potentiometer.

When the staircase waveform reaches the voltage at the LF311's positive input, the comparator output goes LOW (**Fig 13,** trace C) and stays LOW until the positive feedback through the 680-pF capacitor ceases. The delay produced by this feedback ensures a complete reset for the 0.01-μF capacitor, which discharges through the steering diode into the comparator output.

The diode connected from LF311 pin 3 to −15V provides first-order compensation for the steering diode's leakage effects during the charge cycle. **Fig 13,** trace D, shows the waveform at the LF311's positive input. Traces E and F show in an expanded time scale the relationship between the input waveforms and the step-charged ramp.

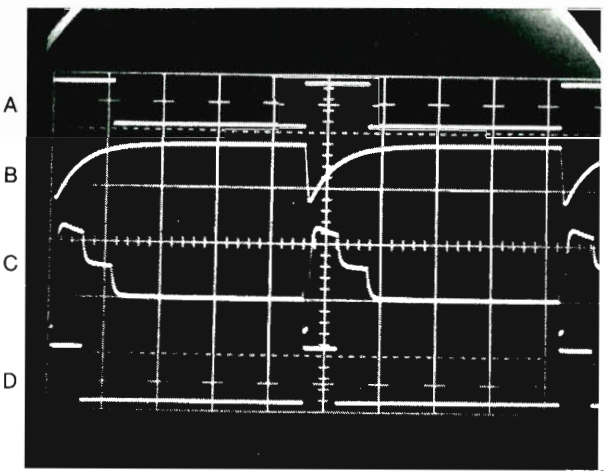
When using this circuit, remember that although the output frequency is always synchronously related to the input frequency, its absolute value can vary with time and temperature. Typically, the trip point—hence, the output frequency—moves back and forth along the horizontal portion of a step at low division ratios and changes from step to step at high ratios.

Overcome TTL multivibrators' shortcomings

If you've used TTL monostables, you've undoubtedly noticed their poor input triggering characteristics and limited dynamic range with a given timing capacitor. The **Fig 14** circuit surmounts these limitations to provide a true level-triggered input and a single-resistor-programmable 10,000:1 output-pulse range. It delivers a preprogrammed output pulse width regardless of the input pulse duration. (The minimum input trigger-pulse width is, however, 3 μsec.)

When you apply an input pulse (**Fig 15,** trace A) to the circuit, $LM393_A$'s output goes LOW (**Fig 15,** trace B), producing reinforcing feedback for its own positive input (**Fig 15,** trace C). This causes $LM393_B$'s output to go HIGH, providing additional feedback to $LM393_A$'s positive input via the 1-MΩ resistor.

When the 50-pF capacitor ceases to provide feedback



TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	200 μSEC/DIV
B	5V/DIV	200 μSEC/DIV
C	1V/DIV	200 μSEC/DIV
D	5V/DIV	200 μSEC/DIV

Fig 15—The output pulse width *(trace D) of* ***Fig 14****'s monostable circuit is insensitive to the input width (trace A).*

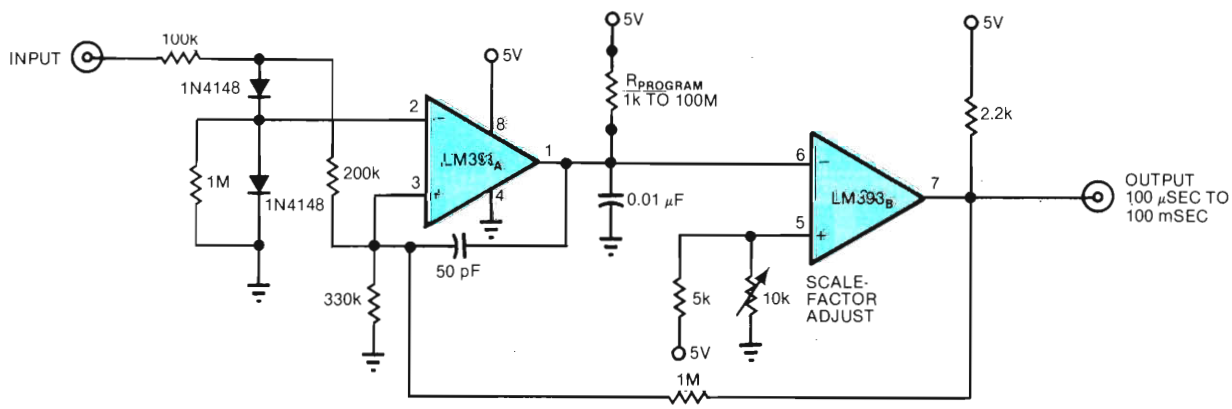


Fig 14—Better than a multivibrator, *this monostable circuit provides a true level-triggered input and a 10,000:1 output pulse range. You program the output pulse width with one resistor.*

to $LM393_A$'s positive input, this comparator's output goes HIGH, allowing the 0.01-μF timing capacitor to charge (**Fig 15,** trace B). When the capacitor voltage exceeds $LM393_B$'s positive input voltage, $LM393_B$'s output (**Fig 15,** trace D) goes LOW, terminating the output pulse.

With the 0.01-μF timing capacitor, you can obtain output pulse widths of 10 μsec to 100 msec, with a scale factor (trimmable with the 10-kΩ potentiometer) of 100Ω/μsec.

Get variable width and delay with one IC

If you need a known-width pulse that's delayed with respect to another pulse, consider the **Fig 16** circuit. It works from one 5V supply and requires only one dual-comparator IC.

When you apply a TTL input (**Fig 17,** trace A), $LM319_A$'s output stays LOW until the 1500-pF capacitor at its positive input charges beyond the negative input's 1.2V level. The resistor-diode clamp from the circuit input to $LM319_A$'s pin 5 provides immunity to input-amplitude variations.

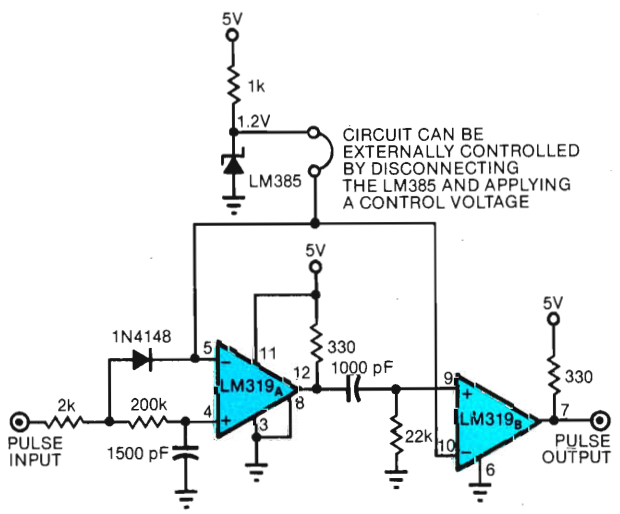


Fig 16—Form a pulse *having the parameters you need from this simple 1-IC circuit. The 1500-pF/200-kΩ network determines delay relative to a triggering pulse; the 1000-pF/22-kΩ differentiator sets the width.*

When $LM319_A$'s output goes HIGH (**Fig 17,** trace B), the transition is coupled via the 1000-pF/22-kΩ differentiator to $LM319_B$'s positive input (**Fig 17,** trace C), causing $LM319_B$'s output to rise and stay HIGH (**Fig 17,** trace D) until the differentiator output drops below the 1.2V level at $LM319_B$'s negative input.

You can tailor both the delay time and the output pulse width to your requirements by altering the values of the RC networks. Alternatively, you can control these parameters externally by applying variable voltages to the comparators' negative inputs.

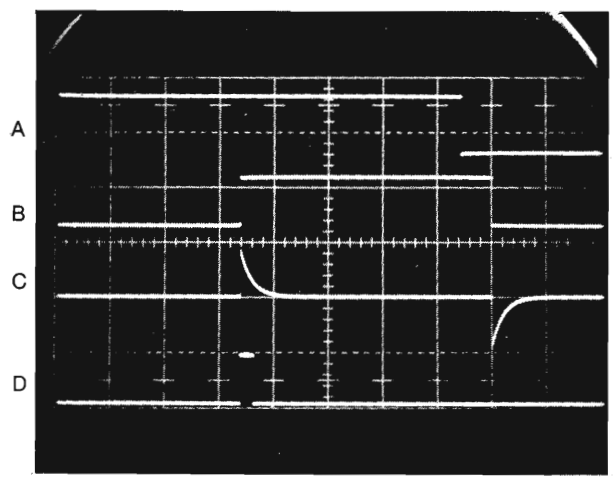
Make an ultrafast V/F converter

Using two comparator ICs, you can build a V/F converter that yields a 5-kHz to 10-MHz output, with better than ±1% linearity, from a 0 to 5V input. The LM160's 20-nsec propagation delay allows **Fig 18**'s circuit to run much faster than monolithic VFCs.

The LM160's output switches the 50-pF capacitor between a reference voltage (furnished by the LM385) and the comparator's negative input. The comparator's output pulse width is unimportant so long as it permits complete charging and discharging of the capacitor. The LM160 also drives the 5-pF/510Ω network, providing regenerative feedback to reinforce its output transitions.

When this positive feedback decays, any negative-going LM160 output is followed by a positive-going edge after an interval determined by the 5-pF/510Ω time constant (**Fig 19,** traces A and B).

The actual integration capacitor—the 0.01-μF unit—never charges beyond 100 mV because it's constantly reset by charge dispensed from the switched 50-pF capacitor (**Fig 19,** trace C). When the LM160's output goes negative, the 50-pF capacitor takes charge from



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	100 μSEC/DIV
B	5V/DIV	100 μSEC/DIV
C	5V/DIV	100 μSEC/DIV
D	5V/DIV	100 μSEC/DIV

Fig 17—A delayed narrow pulse *(trace D) from* ***Fig 16****'s 1-IC circuit specs delay and width of 340 and 30 μsec, respectively.*

Two comparator ICs yield a fast, linear VFC

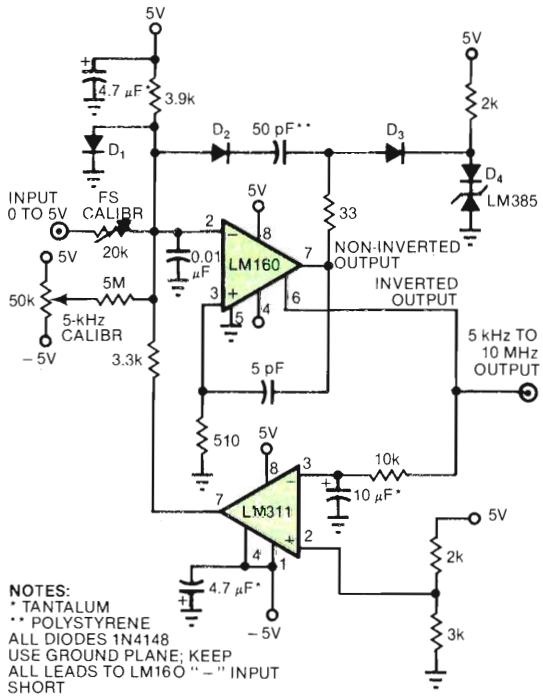
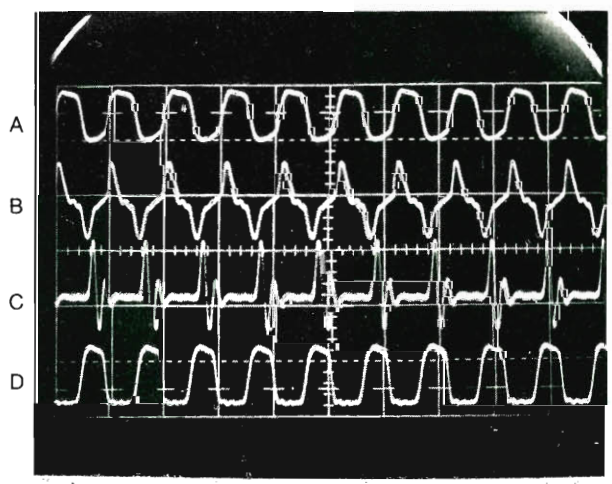


Fig 18—Producing 5-kHz to 10-MHz output, *this V/F-converter circuit uses two comparator ICs and features ±1% linearity. The LM160 is the heart of the converter; the LM311 prevents lockup.*



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	100 μSEC/DIV
B	0.5V/DIV	100 μSEC/DIV
C	10 mA/DIV	100 μSEC/DIV
D	5V/DIV	100 μSEC/DIV

Fig 19—A clean 10-MHz output *(trace D) results from an LM160's action in* **Fig 18***'s V/F converter. Trace C shows the charge-dispensing current from* **Fig 18***'s 50-pF capacitor.*

the 0.01-μF capacitor, resulting in a lower voltage.

The LM160's negative-going output also produces a short negative pulse—via the 5-pF/510Ω feedback—at its positive input. When this negative pulse decays to a point where the positive input is just higher than the negative input, the 50-pF capacitor again receives a charge, and the entire cycle repeats. Diodes D_1 and D_2 compensate for diodes D_3 and D_4, minimizing temperature drift.

The LM160's inverted output (**Fig 19,** trace D) serves as circuit output and also drives the LM311 comparator circuit to prevent LM160 lockup. Without it, any condition (such as startup and input overdrive) that allows the 0.01-μF capacitor to charge beyond its normal operating point could cause the LM160's output to go to the −5V rail and stay there.

The LM311 prevents lockup by pulling the LM160's negative input toward −5V. The 10-μF/10-kΩ network determines when the LM311 switches on. When the VFC runs normally, the 10-μF capacitor charges to a negligibly small voltage, holding the LM311 off. The LM160's inverted output stays HIGH if the VFC stops running (if lockup occurs), forcing the LM311 to turn on and restarting the circuit.

To calibrate the circuit, apply a 5V input and adjust the 20-kΩ potentiometer for a 10-MHz output. Then apply 2.5 mV and adjust the 50-kΩ potentiometer for a 5-kHz output. When building this circuit, use a ground plane and good grounding techniques and locate the components associated with the LM160 inputs as close as possible to the inputs. **EDN**

Author's biography

Jim Williams, now a consultant, was applications manager in National Semiconductor's Linear Applications Group (Santa Clara, CA), specializing in analog-circuit and instrumentation development, when this article was written. Before joining the firm, he served as a consultant at Arthur D Little Inc and directed the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art and collecting antique scientific instruments in his spare time.

Article Interest Quotient (Circle One)
High **479** ***Medium*** **480** ***Low*** **481**

Use motor-drive IC to solve tricky design problems

An IC driver's logic-control features and high output capability suggest elegant ways to handle a variety of difficult-to-drive loads.

Jim Williams, Consultant,
and **Stan Dendinger,** Silicon General Corp

You can use the SG3635 driver IC in a wide range of applications, ranging from a switched-mode motor-speed controller to a data-communications line driver. The device's input configuration simplifies interfacing between low-level circuitry (eg, a μP or logic blocks) and the high-power load. And its output stage (see **box,** "Anatomy of a driver IC"), capable of driving 40V, 2A loads with peaks as high as 5A (including reactive loads), provides sinking and sourcing capability as well as commutation diodes.

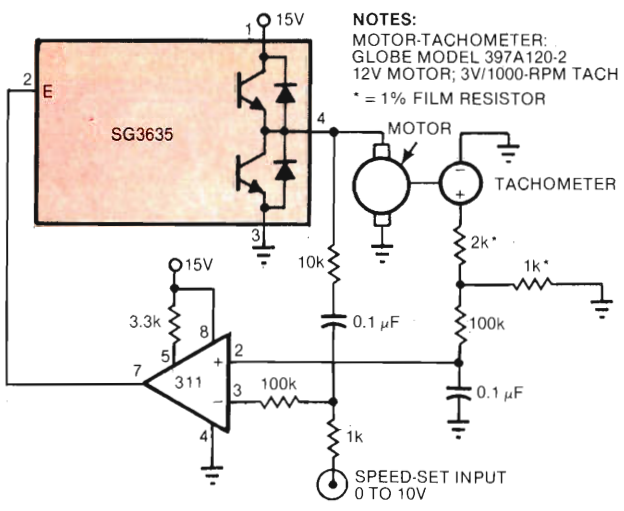
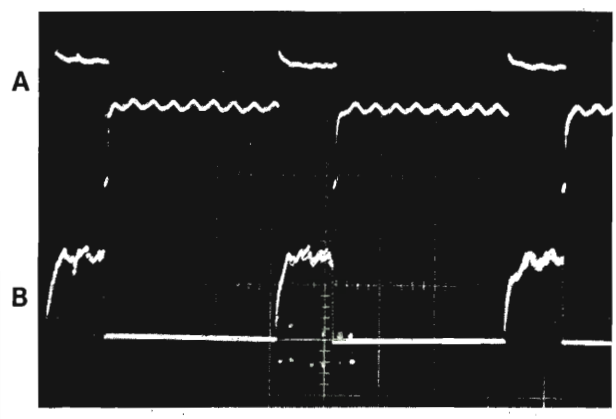


Fig 1—Used in a closed-loop configuration, *the SG3635 self-clocking driver IC controls motor speed in proportion to 0 to 10V input. The comparator weighs the tachometer's output against the input setting, then commands the SG3635 to either speed up or slow down the motor.*



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	5 mSEC/DIV
B	0.5V/DIV	5 mSEC/DIV

Fig 2—Switching on in discrete increments (trace A), *Fig 1's driver IC forces current (trace B) into the motor to speed it up. Upon reaching equilibrium, the circuit oscillates around the setpoint.*

Fig 1 shows one application of the device in a self-clocking switched-mode speed-control loop. The mechanically coupled tachometer detects the motor's speed; its output, scaled and filtered by the RC network, drives the 311 comparator, which compares the output with the speed-setting input and biases the SG3635 to complete the loop.

When the motor slows down, the SG3635's output switches on (**Fig 2,** trace A), forcing current into the motor (trace B) until the comparator's inputs balance. Under these conditions, the circuit oscillates in a controlled manner around the setpoint. The 10-kΩ, 0.1-μF pair provides positive ac feedback to ensure clean transitions.

Control motor speed with minimum parts count

The 3.3-kΩ resistor from the comparator's offset pin to the 15V supply provides enough offset to prevent motor turn-on with a 0V speed setting. In this application the driver only sources current: The sink transistor is never enabled. You could turn the sink device on to dynamically brake the motor, but the motor's back EMF would cause considerable power dissipation. The back EMF appears after the initial inductive spike (clamped by the internal commutation diode), which appears when the IC's output switches LOW.

What about motor-reversing capability? **Fig 3**'s single-supply circuit uses two SG3635s in a bridge configuration. The flip flop generates the necessary complementary instructions to the ICs' Enable inputs. In this example, the SG3635s' Pulse inputs are grounded; you could instead pulse-width-modulate

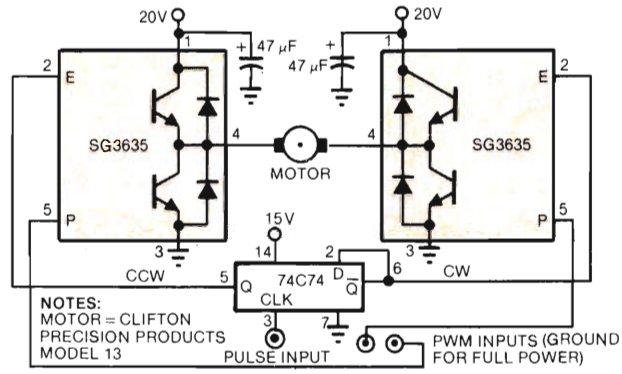


Fig 3—This push/pull bridge configuration *allows two driver ICs to provide bidirectional motor drive. A command to the flip flop's clock input causes instantaneous reversal. Ground the SG3635's Pulse inputs for full speed; apply a pulse-width-modulated input to control the speed.*

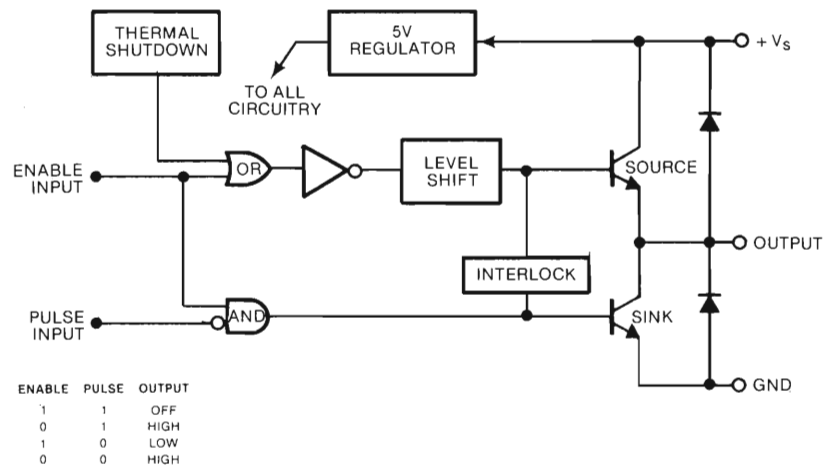
Anatomy of a driver IC

The nearby **figure (a)** shows the SG3635 driver IC's internal organization. The main consideration in the IC's design is to make logic-level/power-load interfacing as straightforward as possible. The logic-compatible Enable and Pulse inputs operate according to the truth table shown: Accepting drive from 74C Series circuits operating at 10V or more, they're compatible with all TTL forms except 54L. You can allow the inputs to float to the HIGH state, but you must force them to ground to produce a ZERO.

Negative supply voltages are permissible at the ground pin, but you must restrict the chip's total rail-to-rail voltage to 40V. The internal regulator stabilizes the IC against supply variations; the level-shift and interlock features provide proper drive levels and prevent simultaneous output-device conduction. The output sinks or sources 2A continuously (5A pk) with ±40V output swing; the commutating diodes handle 5A pk. Finally, the thermal-shutdown circuit disables the upper output device if chip temperature exceeds 160°C.

Why the interlock circuitry? It's important to prevent simultaneous conduction of a source/sink pair's devices **(b)**. This condition usually arises during switching, when the respective devices are interchanging OFF and ON states. During this interval, substantial

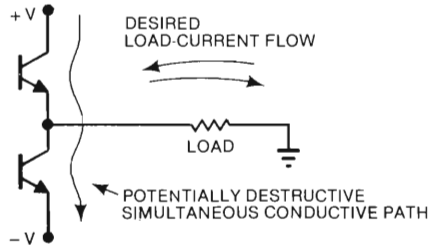
(a)

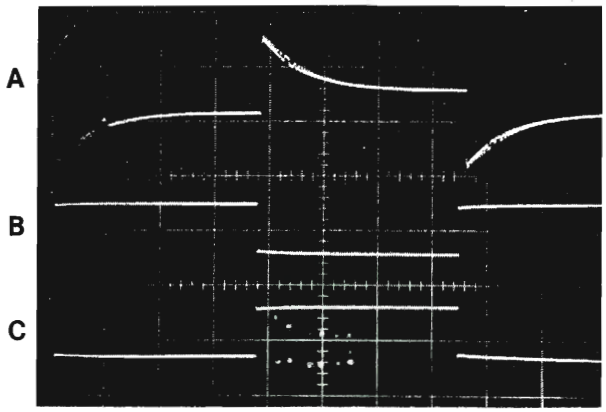


ENABLE	PULSE	OUTPUT
1	1	OFF
0	1	HIGH
1	0	LOW
0	0	HIGH

Providing logic-to-power-drive translation, *the SG3635* ***(a)*** *contains both low- and high-level circuitry. The interlock circuit—an important feature—allows only one power device to conduct at a time, thus avoiding transitional power-supply short circuits* ***(b)****. An IC without the interlock can produce large current pulses* ***(c)*** *during switching. A test circuit* ***(d)*** *verifies the IC's interlock circuitry;* ***(e)*** *shows no common current flows in the output devices during switching.*

(b)





TRACE	VERTICAL	HORIZONTAL
A	2A/DIV	50 mSEC/DIV
B	20V/DIV	50 mSEC/DIV
C	20V/DIV	50 mSEC/DIV

them to control motor speed.

Fig 3's circuit is a good test of the IC's peak current capabilities, because motors present a very difficult load during instantaneous reversal. **Fig 4,** trace A shows the motor current; traces B and C represent the SG3635's voltage outputs. The motor draws 200 mA in normal mode but requires more than 3A during a reversal because of the armature's stored energy.

Servoed motor makes position clear

In addition to controlling speed and direction, you can use the SG3635 in a simple circuit to control a shaft's position **(Fig 5).** In this configuration, the motor drives

Fig 4—Large peak-reversal current in Fig 3's motor *is evident in trace A. Traces B and C show the drivers' output reversal; the outputs handle the 3A motor peaks cleanly.*

supply current flows through both devices, effectively shorting the supplies. A common approach to alleviating the problem is to make the stage switch quickly, minimizing concurrent ON time.

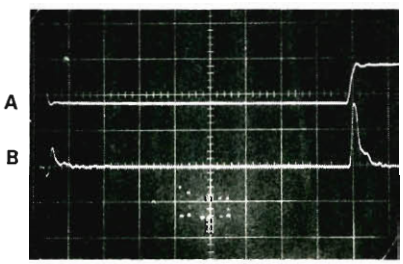
The widely used 555 timer furnishes this simple solution. However, it still generates considerable supply glitches **(c).** Trace B shows the large supply-current spike the IC's output pair produces when switching (trace A). Such a current spike, in conjunction with a supply bus's impedance, can result in unacceptable system noise or device destruction.

The SG3635's interlock circuitry ensures complete turn-off of one output device before the other begins to turn on. This provision eliminates supply shorts during switching, even when controlling high power. To verify this action, use the **figure**'s test circuit **(d).** Part **(e),** trace A shows one phase (Q) of the 74C74's output; trace B depicts the driver's output.

When Q switches LOW, the SG3635 unclamps its sink transistor, then allows the source device to turn on. The reverse holds true when Q switches HIGH. These intentional turn-on delays account for the 200-nsec output-timing skew. Note in trace C—the ground-pin-current—that no current ever flows directly through the source/sink pair.

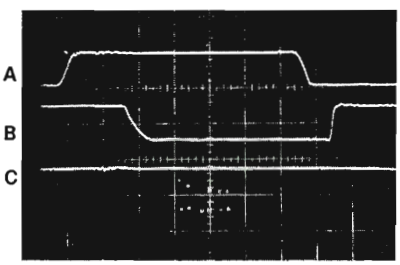
For more information on the SG3635, **Circle No 749.**

(c)



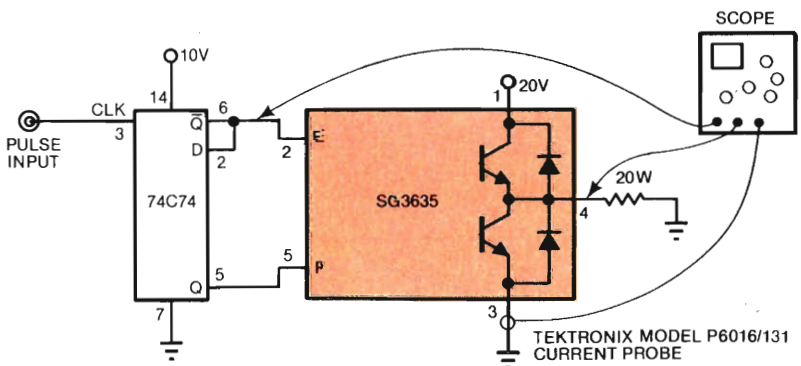
TRACE	VERTICAL	HORIZONTAL
A	20V/DIV	200 nSEC/DIV
B	500 mA/DIV	200 nSEC/DIV

(e)



TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	200 nSEC/DIV
B	20V/DIV	200 nSEC/DIV
C	100 mA/DIV	200 nSEC/DIV

(d)



NOTES:
RETURN SG3635 LOAD AND GROUND-PIN LEADS SEPARATELY TO SUPPLY

IC's high-current output yields fast motor reversal

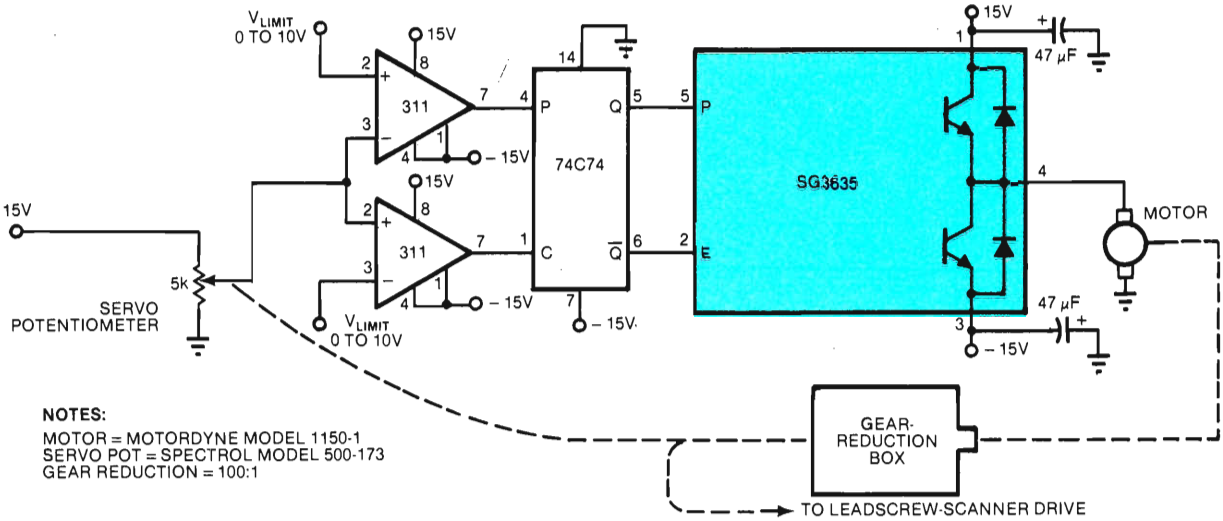


Fig 5—Control a shaft's angular position *with this servo-loop circuit. Select the position by applying limits to the comparator inputs. The circuit uses supplies shifted 15V negative to provide a ground-level bipolar output to the motor.*

a mechanical scanner in either direction between a set of programmed limits. The driver IC's ground pin is biased at −15V, allowing the device's output to swing symmetrically about 0V.

The 5-kΩ pickoff potentiometer detects the scanner's position, then trips a pair of limit comparators; these comparators in turn bias the RS flip flop that controls the SG3635. To provide logic-level compatibility with the driver, the flip flop uses 0 and −15 supplies instead of the usual +15 and 0V configuration. This circuit forces the scanner to run continuously between the limits defined by the V_{LIMIT} inputs. You could control speed by summing pulse-width-modulated signals at the comparator inputs or by gating the SG3635's inputs.

Tackle nonmotor drive problems, too

You can also use the driver IC in applications other than motor control. Consider, for example, the problem of driving long cables at high data rates—a difficult task because of the rapid buildup of parasitic capacitance

Continued on pg 204

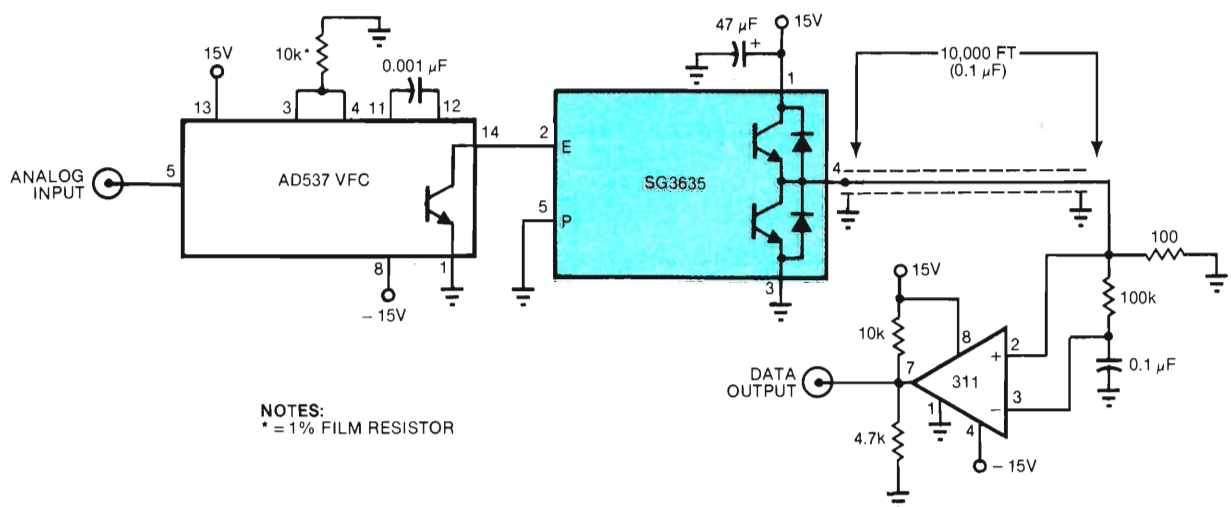


Fig 6—Driving a brutal capacitive load *presents little problem to the SG3635 driver. In this circuit, the IC drives a 10,000-ft data-communications cable having 0.1-µF capacitance. The driver transmits serial 100-kHz data to the receiving comparator.*

Drive long cables with total data recovery

with increasing cable length. In a remote data-monitoring application, for instance, a 10,000-ft cable displays 0.1-μF capacitance—a brutal load at high speed, making receiver-end data recovery difficult.

Fig 6's circuit provides the drive for this difficult load: The V/F converter presents a serial, 100-kHz square-wave data format to the SG3635. The driver's output (**Fig 7**, trace A)—somewhat distorted because of the load—drives the line. Trace B shows the IC's output current: The 5A peaks at the waveform's edges clearly reflect the heavy capacitance.

The square wave's distortion is relatively minor, allowing easy data recovery. The 311 comparator uses a simple RC network to set an adaptive amplitude threshold against which to compare the line output. Because the threshold is derived from the signal, power-supply shifts produce no undesirable effects.

In another nonmotor-related application, you can use the SG3635 in conjunction with a pH probe as a 3-mode controller (**Fig 8**). The FET op amp unloads the probe and routes the signal—via an RC filter—to the two comparators. The comparators, configured as a double-ended limit detector, bias the SG3635; the IC then drives valves that feed either acidic or basic solutions to the chemical vessel.

If pH is correct, both comparator's outputs remain HIGH and neither valve energizes: The appropriate LOW-switching comparator redresses eventual pH imbalance by turning the necessary valve on.

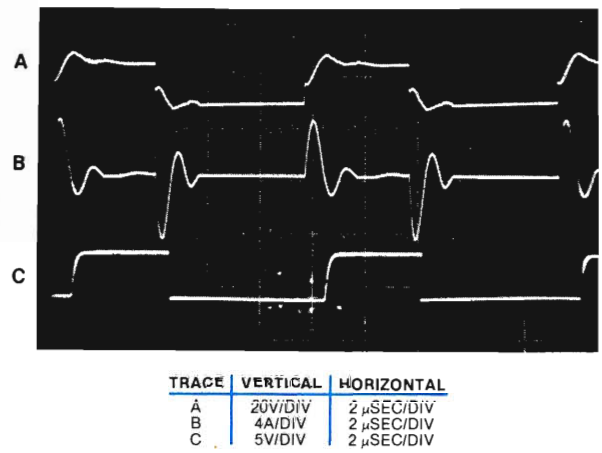


Fig 7—The effects of Fig 6's gluttonous capacitive load *are evident in traces A and B. The 10,000-ft line absorbs 5A current peaks during the IC's switching transitions. The receiving-end comparator uses an adaptive amplitude threshold to produce a clean output.*

In a final example of the driver IC's versatility, consider its use as a power-transistor driver. Driving these devices at high speed requires active turn-off techniques to sweep charges from the base-emitter junction. Moreover, many high-voltage power transistors need negative base bias to guarantee breakdown ratings.

Assume, for example, the use of unipolar base drive

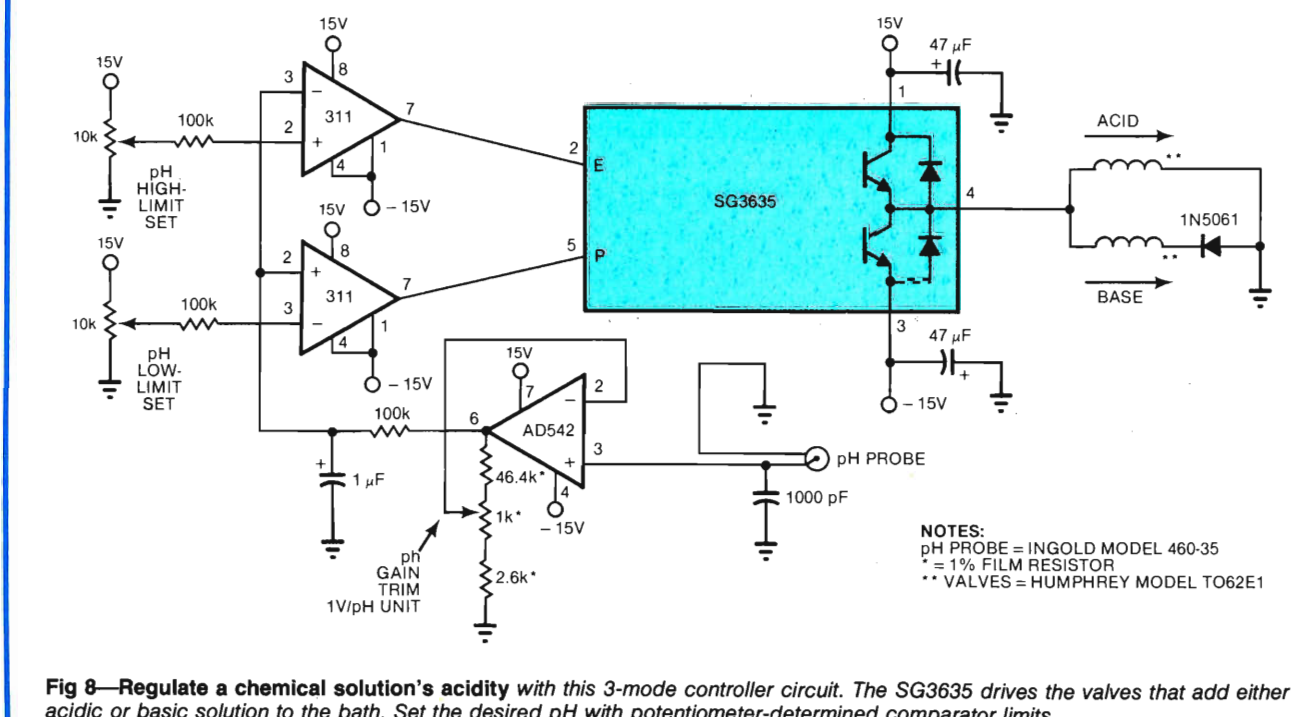


Fig 8—Regulate a chemical solution's acidity *with this 3-mode controller circuit. The SG3635 drives the valves that add either acidic or basic solution to the bath. Set the desired pH with potentiometer-determined comparator limits.*

Valve-control circuit maintains constant pH

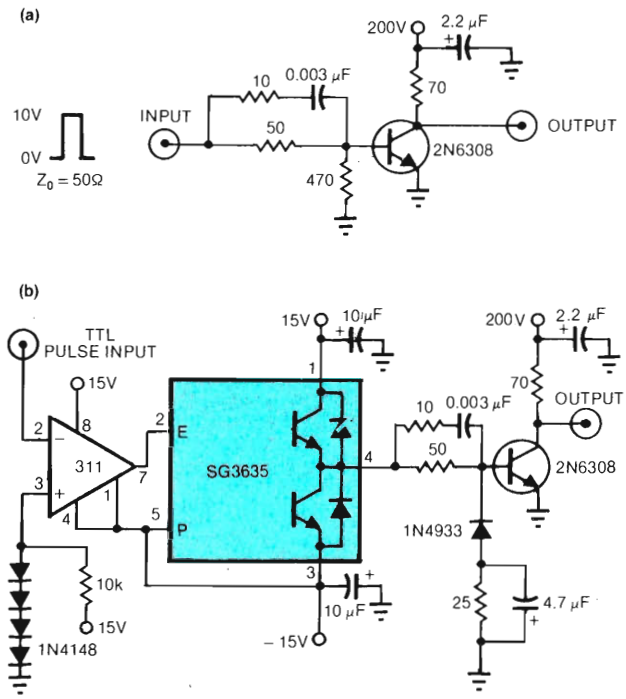
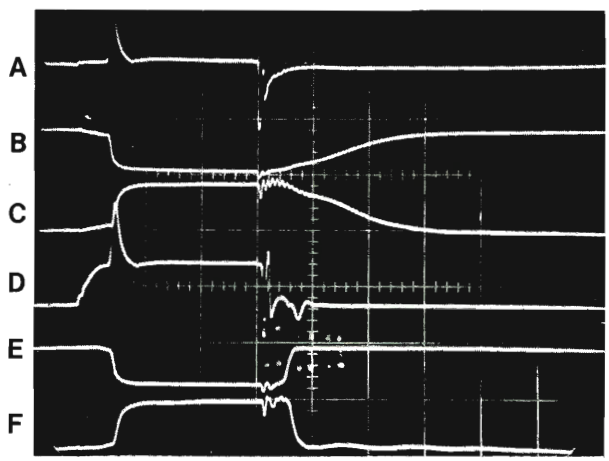


Fig 9—Using unipolar base drive (a) *for a high-power transistor can result in slow collector turn-off. A bipolar-drive circuit* ***(b)*** *shortens turn-off time considerably by sweeping out base-emitter charge. Moreover, the negative base bias improves the transistor's breakdown characteristics.*



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	500 nSEC/DIV
B	200V/DIV	500 nSEC/DIV
C	3A/DIV	500 nSEC/DIV
D	5V/DIV	500 nSEC/DIV
E	200V/DIV	500 nSEC/DIV
F	3A/DIV	500 nSEC/DIV

Fig 10—Dramatic turn-off-time differences *between unipolar- and bipolar-base-drive circuits* ***(Figs 9a*** *and* ***9b)*** *are evident in this photo. Long collector-voltage (trace B) and -current (trace C) ON-to-OFF transitions result from the unipolar drive (trace A); the bipolar drive (trace D) increases turn-off speed more than sevenfold.*

(**Fig 9a**) for a high-power 2N6308. **Fig 10,** trace A shows the transistor's base waveform; traces B and C display collector voltage and current, respectively. Because the base drive is unipolar, the collector turns off slowly: Voltage and current require about 1.5 μsec to settle. What's more, the transistor dissipates considerable power during turnoff, increasing its vulnerability to secondary breakdown. Inductive loads (eg, flyback transformers) can exacerbate the situation.

The solution? **Fig 9b**'s circuit uses an SG3635 to provide bipolar base drive, thereby shortening turn-off time. The 311 comparator shifts the TTL-command level to bias the driver's Enable input; shifting is necessary because the SG3635's ground pin is returned to −15V. The 25Ω resistor to ground limits the transistor's reverse bias. Traces D, E and F show the 2N6308's base voltage and collector voltage and current, respectively—you can see that collector turn-off time decreases to 200 nsec, greatly reducing the likelihood of secondary breakdown. **EDN**

Authors' biographies

Jim Williams, now an applications manager specializing in analog-circuit and instrumentation development at Linear Technology Corp (Milpitas, CA), was a consultant when this article was written. Before joining the firm, he served in a similar capacity at National Semiconductor Corp, worked as a consultant at Arthur D Little Inc and directed the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art and collecting antique scientific instruments in his spare time.

Stan Dendinger is manager for advanced product development at Silicon General Inc (Garden Grove, CA). There, he is responsible for the development and improvement of several of the firm's regulating pulse-width-modulator ICs. Stan holds a BSEE degree from the University of California at Berkeley. He is also a professional choral singer and enjoys modifying sports cars as a hobby.

Article Interest Quotient (Circle One)
High **488** ***Medium*** **489** ***Low*** **490**

Simplify feedback controllers with a 2-quadrant PWM IC

A 2-quadrant pulse-width-modulator IC eliminates many of the problems arising with unipolar devices in feedback-control applications.

Jim Williams, Consultant,
and **Stan Dendinger,** Silicon General Corp

The SG1731 pulse-width-modulator (PWM) IC brings to motor controllers and similar applications the efficiency previously limited to switching-power-supply circuitry. As a result, you can use it to design motor-controller circuits having parts counts smaller than previously achievable.

Switching-power-supply PWM controllers are designed to be 1-quadrant power conditioners, furnishing a dc output voltage with fixed polarity and amplitude proportional to a unipolar reference voltage. Motor controllers, on the other hand, require an integrated pulse train with a dc component proportional to the magnitude of an applied reference voltage and polarity determined by the reference's sign. Otherwise, they can't produce bidirectional rotation.

In addition, the architecture of power-supply PWM ICs often proves inappropriate for motor-control tasks, requiring so many auxiliary circuits that totally discrete designs often prove more economical. PWM

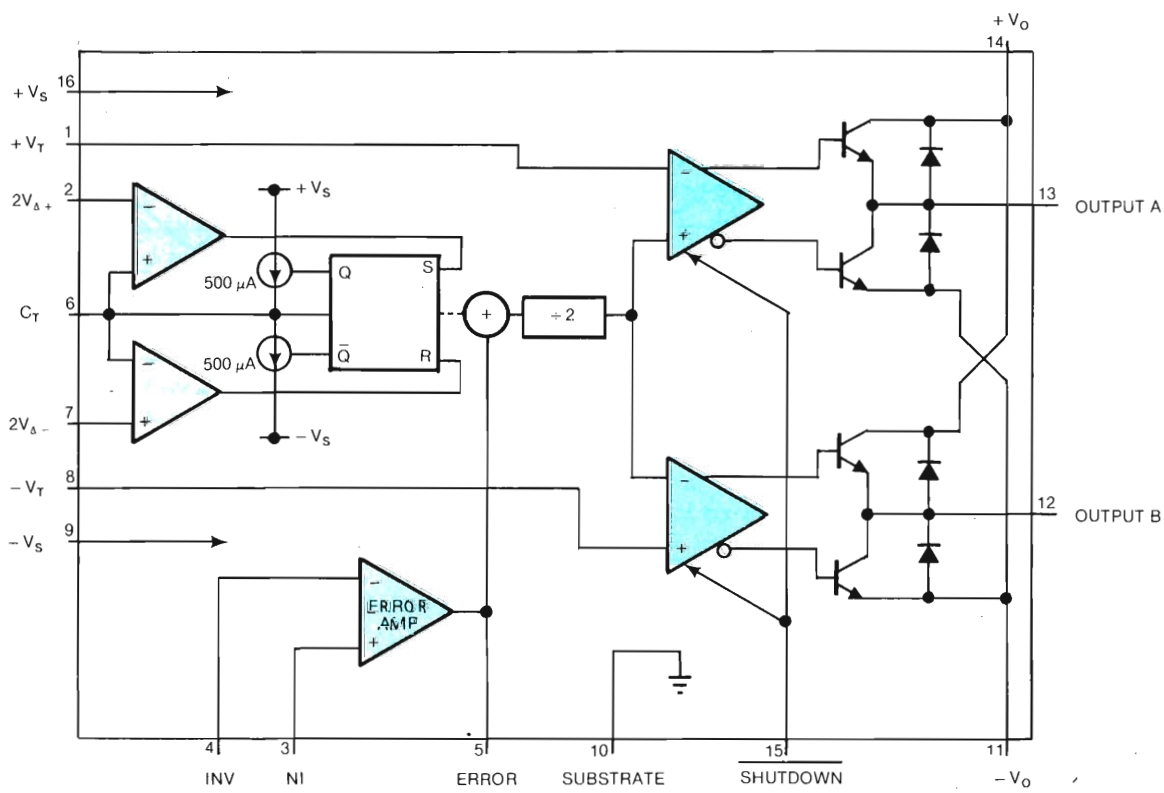


Fig 1—A dc-motor pulse-width-modulator IC, *the SG1731 features 50-Hz to 350-kHz oscillator range, adjustable deadband operation, a high-slew-rate error amplifier, a Shutdown input providing floating outputs, and dual 100-mA source/sink output drivers capable of operating from supplies to ±32V.*

Error voltage controls pulse-width modulation

power-supply controllers attempt to produce a variable-energy-content ac waveform, because power must be transferred via a high-frequency transformer. Unlike those from a PWM motor-control IC, the PWM pulses produced by these devices must alternate and are therefore produced by a dual-driver architecture.

Fig 1 shows the SG1731's structure. The device contains a triangle-waveform oscillator whose frequency is determined by an external capacitance at pin 6 and whose amplitude can be set through resistor or voltage programming at pins 2 and 7. The IC also contains a wide-band op amp for error-voltage generation, a summing/scaling network for level-shifting the oscillator waveform, externally programmable PWM comparators and dual ±100-mA continuous (±200-mA pk), ±32V totem-pole drivers with commutation diodes for full-bridge output drive. Typical supply voltages are ±15V, although the device can function at values as low as ±3.5V. You can use dual- or single-polarity supply voltages. Pin 15, the $\overline{\text{Shutdown}}$ terminal, forces the output drivers into high-impedance states when LOW.

Pulse-width modulation occurs when an error voltage gets added to the triangle waveform, attenuating the resulting signal by a factor of two and comparing it with threshold voltages $+V_T$ and $-V_T$ (pins 1 and 8). **Fig 2** illustrates the case for $V_\Delta < V_T$. When the error is 0V, no threshold crossings occur, and the output drivers remain at $-V_0$ **(Fig 2a).** As the error voltage goes positive, the upper threshold gets periodically crossed by the shifted waveform, and output driver A switches to $+V_0$ **(Fig 2b).** As the error voltage becomes larger, the duty cycle of driver A increases linearly toward 100%. The same action occurs at output B **(Fig 2c)** for negative error voltages.

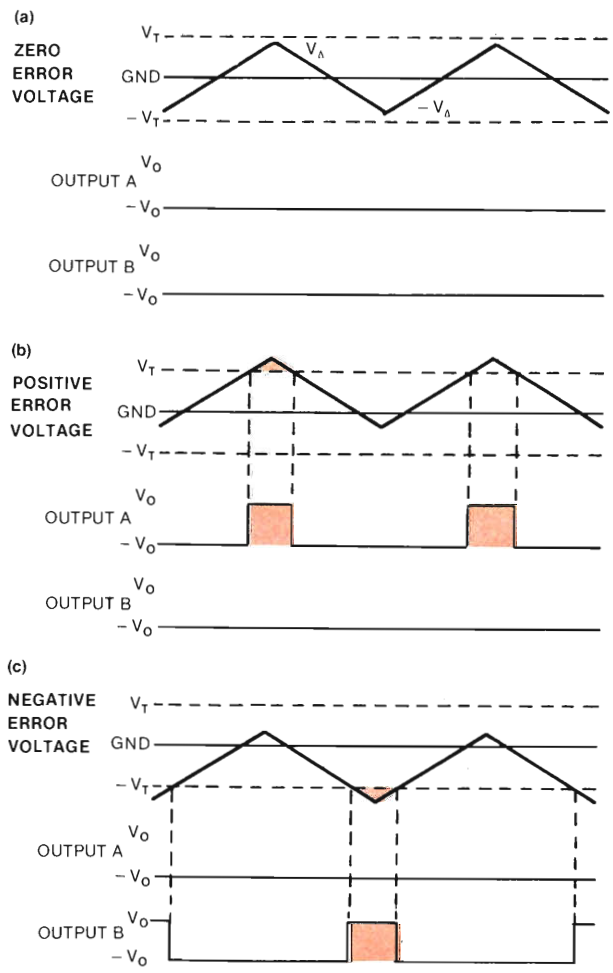


Fig 2—With oscillator voltage less than threshold voltage, *the SG1731's outputs switch LOW to HIGH when the error voltage shifts oscillator output outside the threshold.*

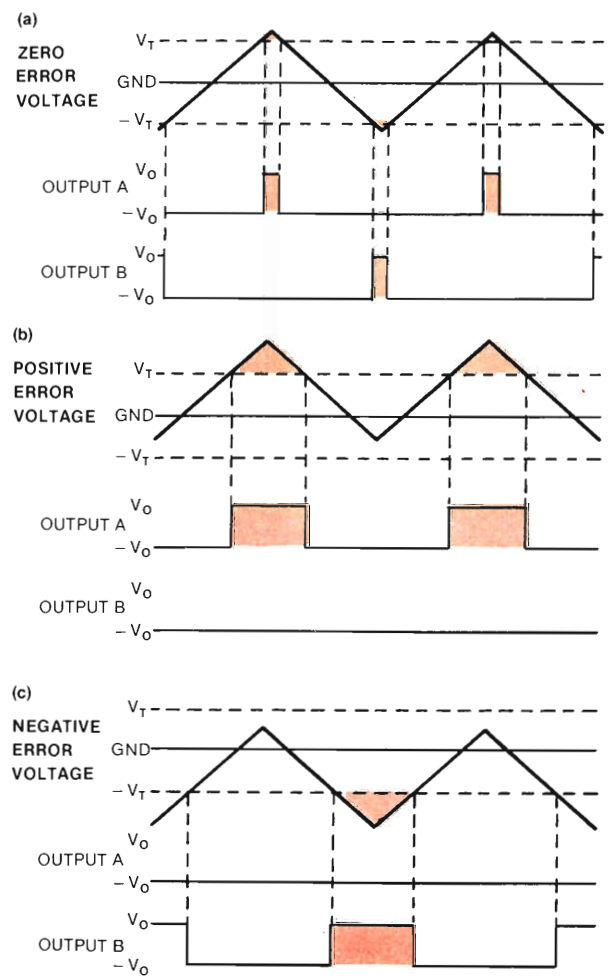


Fig 3—With oscillator voltage greater than threshold voltage *in the 1731, lack of a deadband provides resistance to motor movement caused by external forces.*

Class D amplifiers for audio applications

Almost all amplifiers use some form of output pass element to deliver power to a load. Because the amplifier controls this pass element, and because the amount of power delivered to the load varies, dissipation is inevitable. And at high power, substantial dissipation losses place limits on packaging, power consumption and efficiency.

One form of amplifier, the Class D stage, largely circumvents these problems by using a switched-mode output stage to deliver power to the load. Because the amplifier's output is either ON or OFF, efficiency is higher than that of a linear stage, and heat dissipation is low. In **Fig A,** the output of such a stage is represented by a series of width-modulated pulses whose power-time spectrum is related to the input signal.

In theory, this type of stage can serve in an efficient audio amplifier. And recently, designers have expressed a great deal of interest in developing such an amplifier. However, practical problems have made a workable switching design for audio difficult to achieve.

Historically, switched-mode-amplifier designs called for complex circuitry and expensive output devices. Producing a pulse-width modulator that provides 2-quadrant response with high linearity and wide bandwidth was difficult. In addition, even if available, low-loss output switches that operated at high carrier frequencies were expensive, and the drive circuitry quite complex.

The introduction of power-FET devices has reduced design-cost and complexity problems in the output stage. But although such components make the job easier, designers still must deal with several issues to achieve optimum performance.

One unpleasant surprise is the combination of the high-frequency

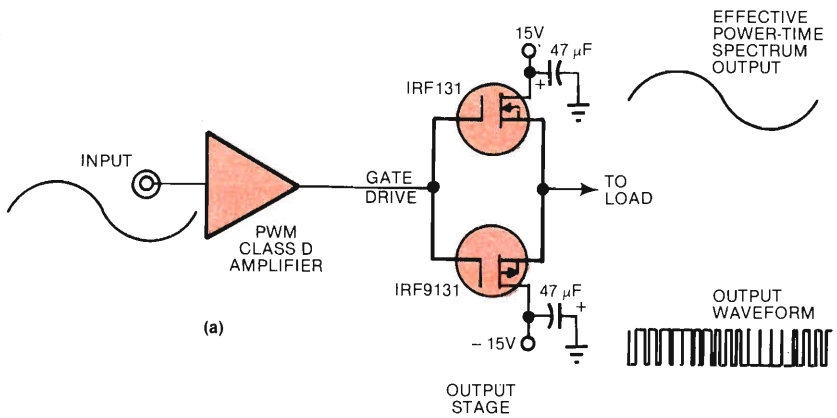
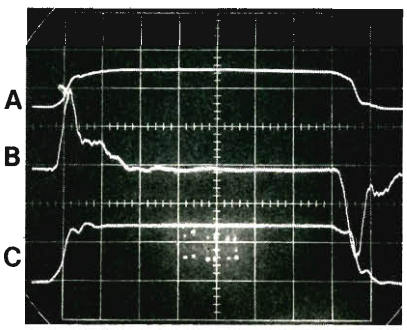


Fig A—A switched-mode PWM Class D amplifier *coupled to an FET output stage provides efficient operation.*

carrier and the FETs' input capacitance. The FET gate drive (**Fig B,** trace A) causes the current drawn through the input capacitances (trace B) to peak at 400 mA on both edges as the FETs switch. Although the FETs have a high impedance at dc, the high carrier frequency required for audio calls for substantial average gate current. This requirement in turn calls for some form of preceding driver.

A more serious problem centers on filtering the carrier at the load (a speaker in audio applications). Filter design is complicated by the uncertain characteristics of the lead wire and speaker that connect to the amplifier. Even if these parameters are fixed by specification, the speaker's reactive nature complicates the design.

Even assuming the filter can be built, the waveform across the speaker is well out of the phase with the input because of carrier-induced phase shift as well as filter phase shift. As a result, closing a feedback loop from the load proves difficult. It might be possible to use a complementary phase-shift network to correct for this shortcoming, but the design of this type of an audio-grade compensation scheme is difficult. Without feedback, the problem goes away, but nonlinearities in



TRACE	VERTICAL	HORIZONTAL
A	50V/DIV	200 nSEC/DIV
B	200 mA/DIV	200 nSEC/DIV
C	20V/DIV	200 nSEC/DIV

Fig B—Fig A's FET output stage *draws 400-mA pk gate current when the FETs switch (trace B). Trace A is the gate drive signal; trace C, the FETs' source lines.*

the pulse-width modulator then contribute to output distortion.

Finally, the high-frequency harmonics in the switching stage pose a difficult RFI-suppression problem. The same fast switching that yields efficiency and wide-range audio bandwidth also qualifies as a potential broadband radio transmitter and must be suppressed. This need mandates careful layout, expensive and complex packaging and RFI suppression on both power and speaker connections.

No motor power required with deadband operation

A motor connected across the full bridge formed by drivers A and B receives a high-frequency pulse train. When integrated by the armature's L/R time constant, this pulse train results in a voltage drive proportional to the error signal's magnitude. Drive-signal and error-voltage polarities are identical.

With this deadband operation, no motor power gets applied in a small region around the servo loop's null point. Although this action conserves power (desirable in some applications), it results in a loss of both positioning accuracy and mechanical stiffness. Deadband operation is also not desirable in switching (Class D) audio amplifiers. There, crossover distortion is unacceptable, and poor speaker damping results (see **box,** "Class D amplifiers for audio applications").

The other SG1731 mode of operation is shown in **Fig 3,** where $V_\Delta > V_T$. At the loop null point, the motor receives drive pulses that resist externally produced armature movement. The integrated drive voltage is 0V with no error voltage (**Fig 3a**) because the drive pulses alternate in polarity and have identical widths at the null point. **Figs 3b** and **3c** show the effects of error voltages on the oscillator signal.

This is the preferred control mode in a missile-fin-actuator system, for example, where aerodynamic forces on the airfoil attempt to move the motor armature away from the null position.

You can configure the SG1731 as a bidirectional motor-speed controller as shown in **Fig 4.** The motor specified runs directly from the device's outputs, and the tachometer produces an output directly proportional to the motor's speed and direction. This high-level signal gets divided down and filtered by the discrete components associated with the tachometer, then applied to the 1731's error-amplifier input. The 1731 internally compares this signal with the speed-control input's value and provides output drive of the appropriate phase and magnitude, completing a speed-control loop. Set the comparator voltages for nondeadband operation. The lowest rotation speed depends on the motor's friction characteristics.

Instantaneous-direction-reversing applications might require an optional current-limiting circuit rather than ±15V applied directly to pins 11 and 14. At the time of direction reversing, the motor draws peak currents that could damage the 1731's output drivers. Q_1's ability

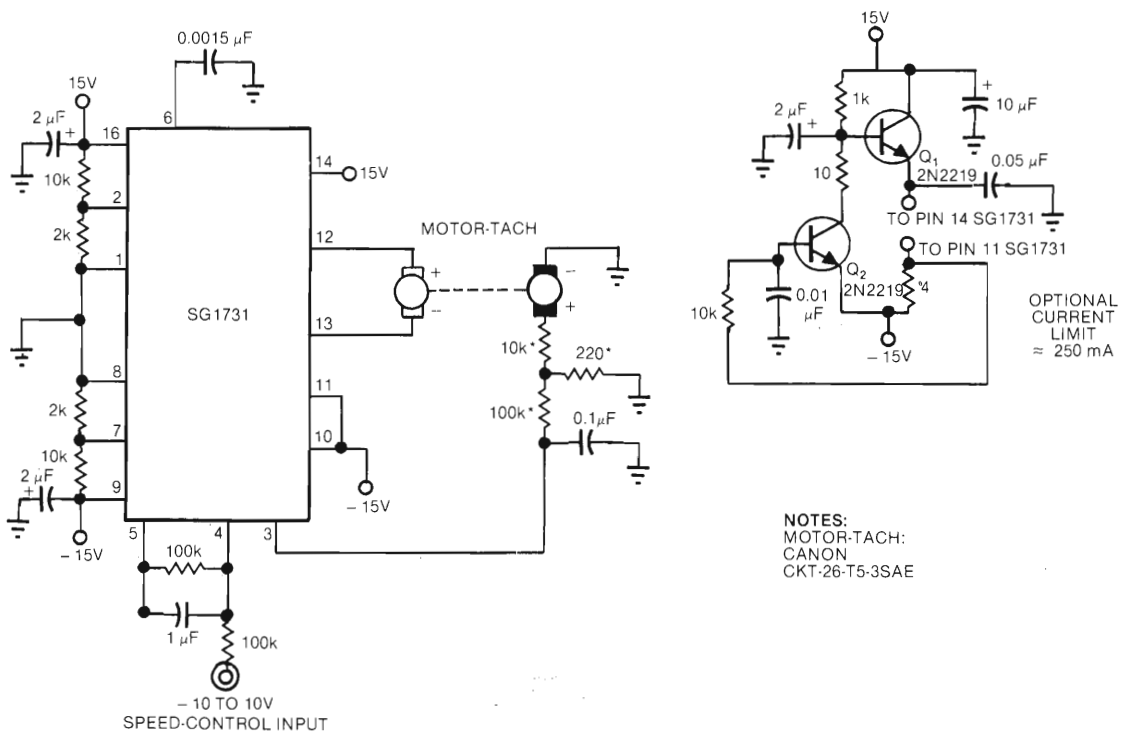


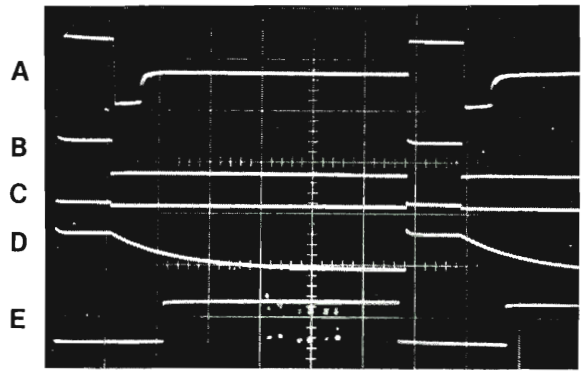
Fig 4—In this bidirectional motor-speed controller, *the tachometer provides feedback while the current-limiting circuit protects the outputs from surge currents.*

to supply current is controlled by Q_2's state, which in turn depends on the voltage across the 4Ω current-sensing resistor. If the motor current exceeds 200 to 250 mA, Q_2 turns on and Q_1 shuts off.

Another bidirectional speed-control loop appears in **Fig 5.** Here, SG1635 drivers control higher motor power and eliminate the need for a speed-monitoring tachometer; instead, back EMF produced by the motor serves as a feedback signal. This arrangement entails some increase in circuit complexity but eliminates the tachometer's cost.

The circuit's basic servo mode is similar to that of **Fig 4.** The 311 comparator (IC_1) senses the polarity of the input command signal. Its output goes to the 1635s via a diode and inverter, allowing both 1635s to be OFF, neither sinking nor sourcing current, when the 1731 is not producing output pulses. **Fig 6** shows the circuit waveforms. When either 1731 output is HIGH, the other output is LOW, and the motor is driven. When both outputs are LOW, the 1635s are OFF and the motor is electrically floating.

The motor's inductive turn-off spike gets damped by the 1635s' internal diodes. After turn-off, the waveform



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	200 μSEC/DIV
B	20V/DIV	200 μSEC/DIV
C	10V/DIV	200 μSEC/DIV
D	20V/DIV	200 μSEC/DIV
E	20V/DIV	200 μSEC/DIV

Fig 6—Waveforms for Fig 5's tachless controller *include the controller's outputs (traces B and C) and the voltage across the motor (trace A). The 10-kΩ/0.02-μF network's decay time (trace D) ensures that the FET drive (trace E) remains off until after the inductive spike has settled out.*

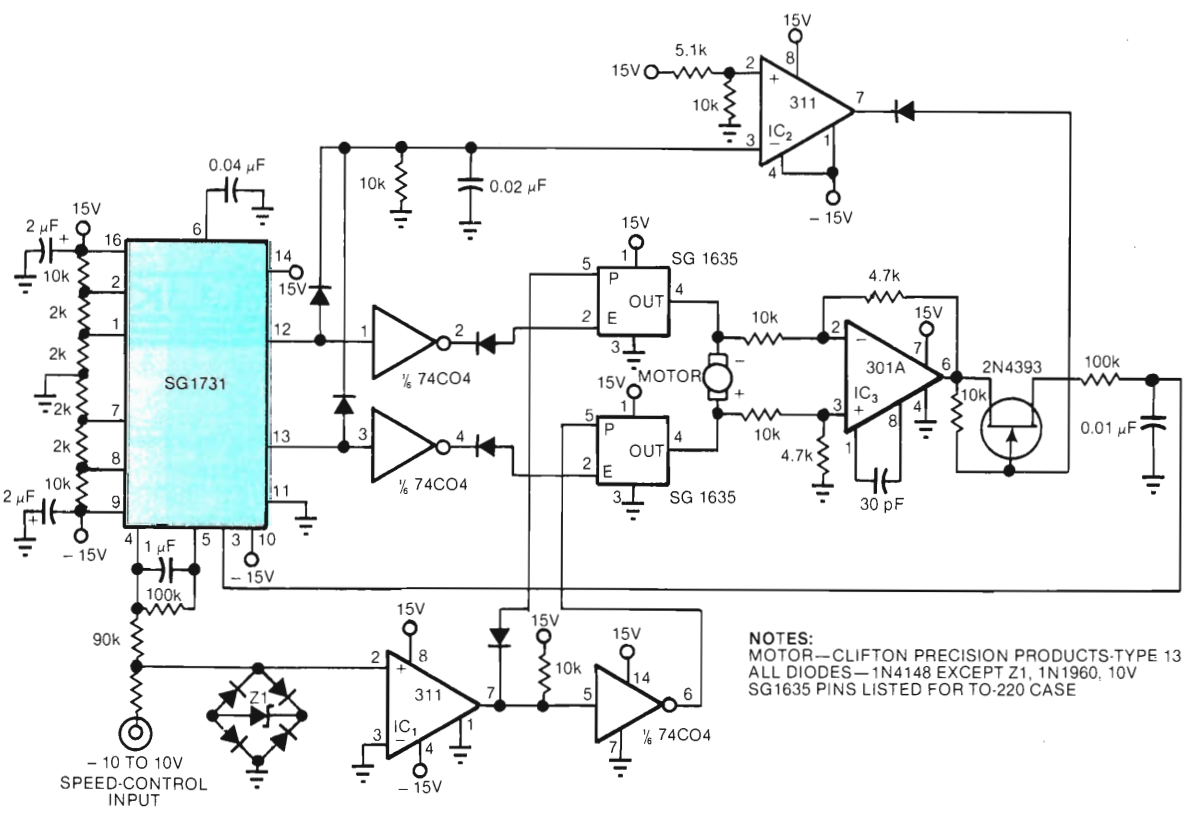


Fig 5—A tachless controller *based on the 1731 uses motor back EMF and some additional parts to reduce overall cost.*

Eliminate servo hunting with long time constants

returns to a dc level determined by the back EMF of the undriven motor, now functioning as a tachometer. This level gets differentially picked off by the 301A op amp (IC_3), whose output feeds a switched synchronous filter. This filter, composed of the FET and the 100-kΩ/0.01-μF combination, samples the back-EMF value during the motor's powered interval.

A 311 (IC_2) gates the FET switch synchronously with the 1731's output. The diode-RC network feeding IC_2 allows either output to actuate the filter. The 10-kΩ/0.02-μF network's decay time length (**Fig 6,** trace D) ensures that the FET drive (trace E) remains OFF until well after the inductive spike has settled out.

The pure dc filter output feeds back to the 1731's error amplifier to complete the speed-control loop. The zener-diode bridge clamps all inputs above approximately ±10V; otherwise the 1731's outputs would saturate at dc and the switched feedback loop would never operate.

Another SG1731 application appears in **Fig 7.** Here, two 1731s bidirectionally control the speed and shaft position of a printed-circuit-type motor.

The shaft position gets sensed at the output of a geardown transmission. Slave the 1731s together to avoid producing frequency beating from separate oscillators; take the triangle waveform of $SG1731_A$ through a 301A follower and use the output to drive the capacitor pin of $SG1731_B$. This is an effective way to slave 1731s together because the follower's low-impedance output overrides whatever state the unbiased internal oscillator of $SG1731_B$ might take. Control the shaft position by sensing it with a potentiometer that feeds a signal back to $SG1731_A$. This signal then gets compared with the Position input, and the outputs of $SG1731_A$ drive the shaft to the position required to balance the error amplifier's inputs.

$SG1731_B$ functions in a speed-control loop similar to that described in **Fig 4.** It controls speed by using its output pins, via a diode OR gate, to pulse-width-modulate $SG1731_A$'s $\overline{\text{Shutdown}}$ pin. The 311 comparator prevents either $SG1731_B$ output from going LOW on a dc basis by synchronously gating signals into the device's output comparators, forcing the appropriate output HIGH.

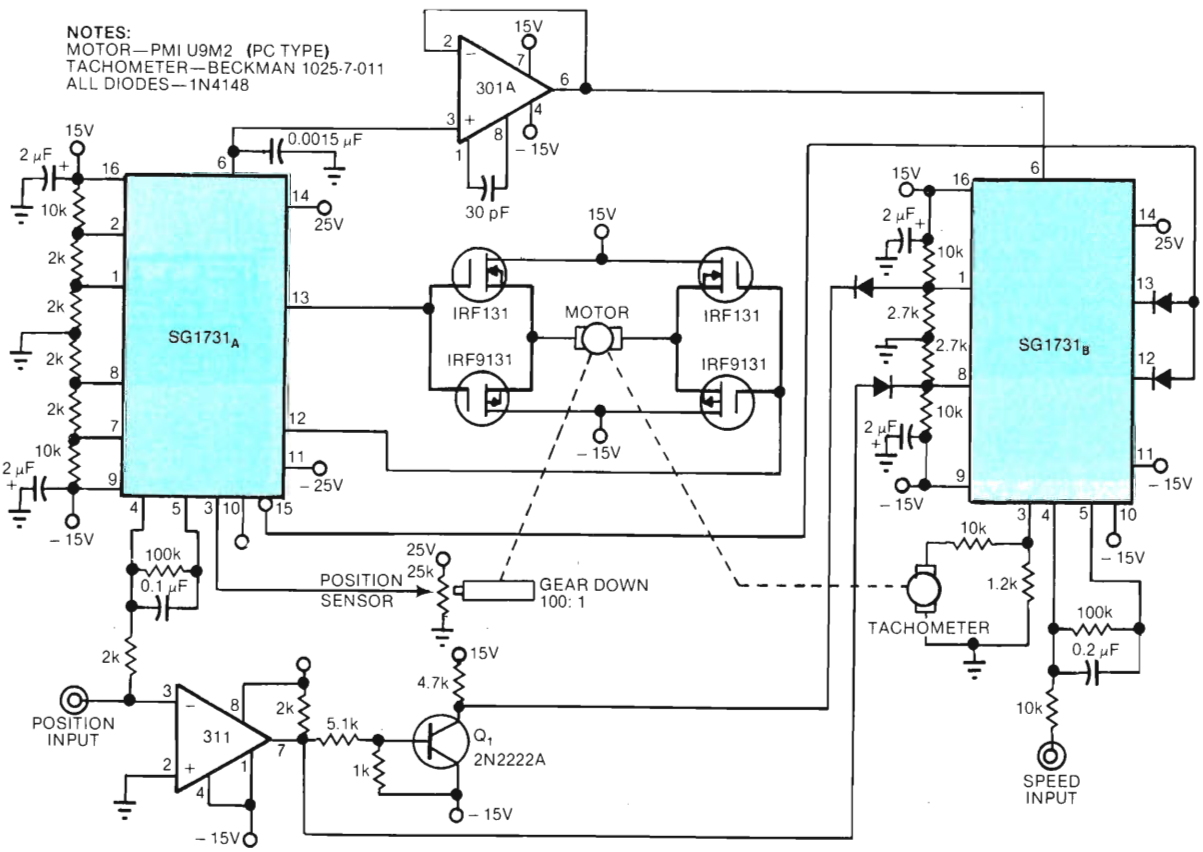


Fig 7—In this bidirectional motor-speed-controller/positioner application, *$SG1731_A$ acts as a position servo, while $SG1731_B$ controls speed.*

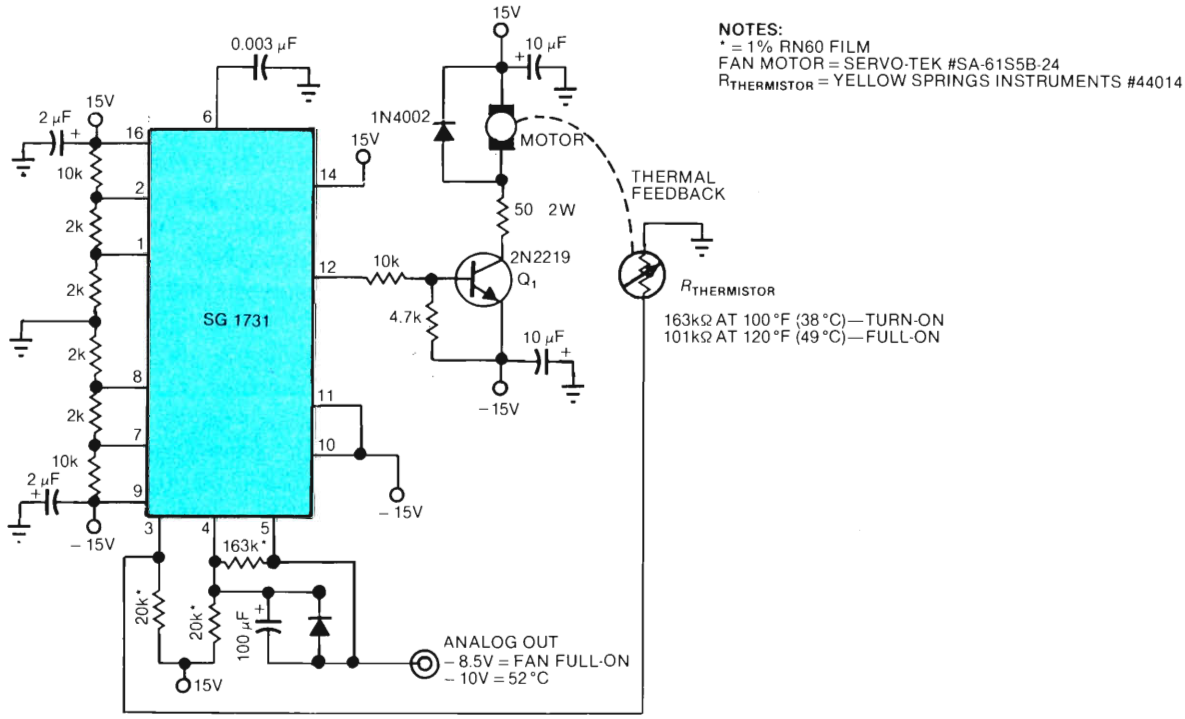


Fig 8—A fan-temperature controller's error-amplifier output *(pin 5) warns of an overtemperature condition.*

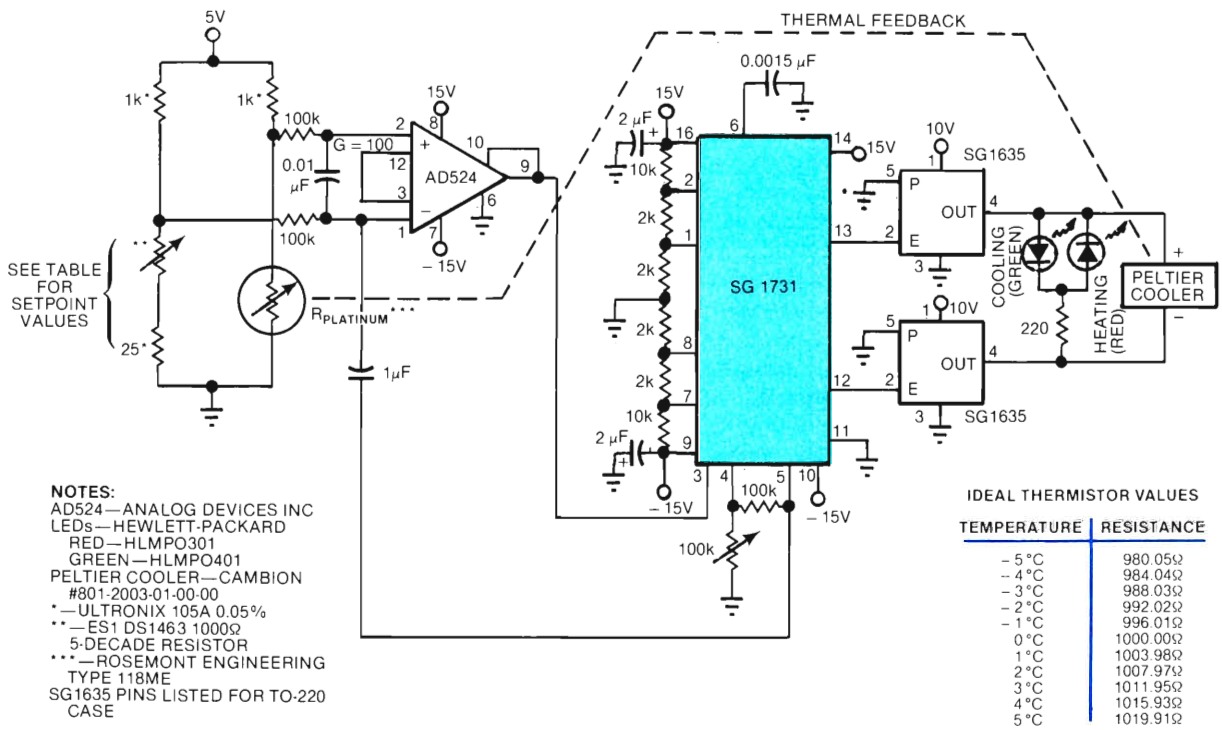


Fig 9—A well-insulated Peltier cooler *with good heat removal on its normally hot side specs stability better than 0.02°C typ.*

Motors adapt easily to Class D operation, speakers don't

Consider $SG1731_A$ to be a position servo; $SG1731_B$ controls how quickly the position is acquired. Dead-zone control results from voltage-modulating $SG1731_B$'s comparator thresholds.

Fan-temperature control safeguards instruments

You can also use a 1731 to control a fan motor's speed, regulating instrument temperature and extending fan life (**Fig 8**). At least one oscilloscope manufacturer uses this approach, and it has also found use in several military applications.

When power is applied, the thermistor, located near the fan, has a high resistive value. This condition unbalances the amplifier-driven bridge, sending pin 12 LOW. Q_1 and the fan motor are off. But as the instrument warms, thermistor resistance decreases, producing PWM signals at pin 12 and turning Q_1 and the fan motor on.

The 100-μF capacitor determines the time constant across the error amplifier; a short time constant produces audibly annoying hunting in the servo. The 50Ω resistor limits motor current, and the 1N4002 diode dampens motor spikes.

The SG1731 can function in nonmotor applications, too. The freezing point of water serves as a reference point for the calibration of various types of temperature sensors, such as platinum RTDs and thermocouples. In such applications, an ice slurry in a Styrofoam container or a Dewar bottle is usually used to achieve the 0°C condition. Although inexpensive, this approach requires constant ice replenishment and water removal and tends to be messy. As an alternative, you can use the SG1731 to provide 2-quadrant control for a Peltier-junction-type thermoelectric cooler.

Current flow in a Peltier device cools one side of the junction and heats the other; reversing the applied current causes the cold side of the junction to heat and the hot side to cool. Commercial devices use a large number of junctions to achieve high thermal capacity and are about the size of a postage stamp. They are optimized for one direction of current flow but can work both ways.

Fig 9's circuit capitalizes on this characteristic to achieve a very precise temperature reference that cools to 0°C and then settles out very quickly. Most thermal control loops settle slowly because energy can only be

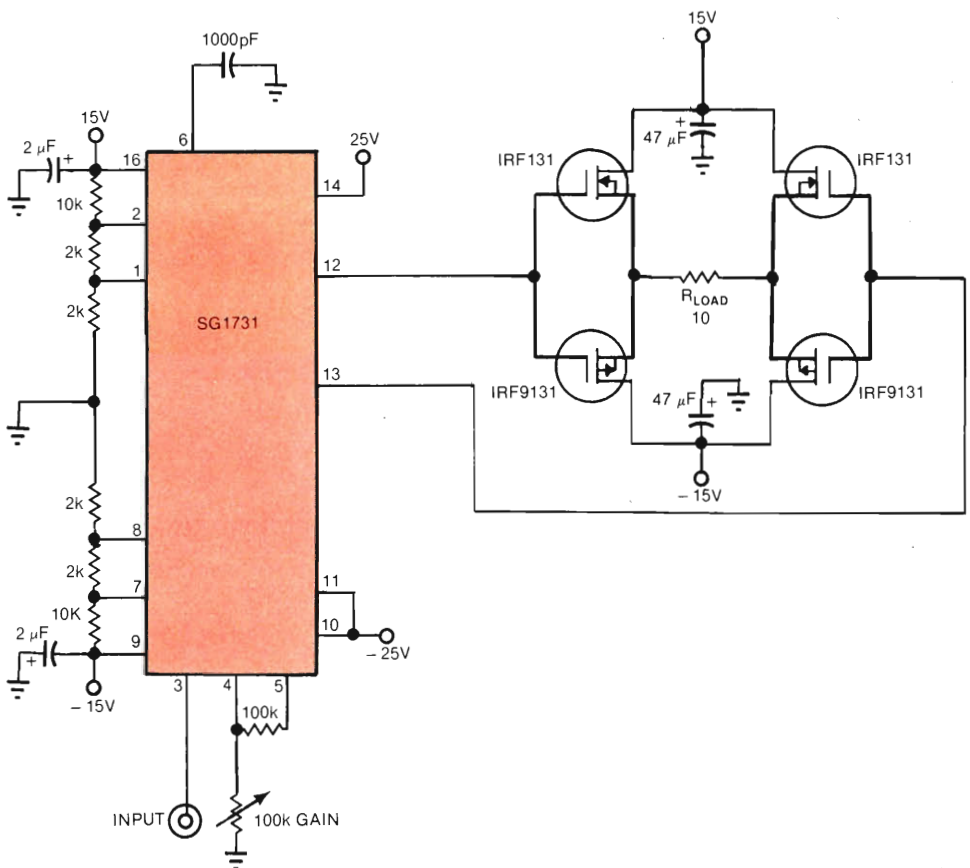
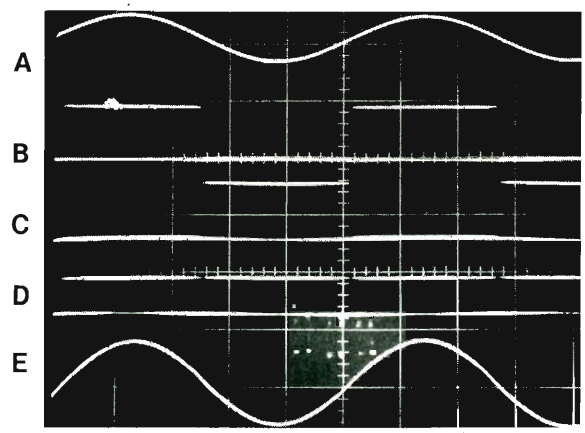


Fig 10—A switched-mode power amplifier *using a 25-kHz carrier transmits a 400-Hz waveform to a load.*

Temperature reference is bidirectional



TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	500 μSEC/DIV
B	50V/DIV	500 μSEC/DIV
C	50V/DIV	500 μSEC/DIV
D	50V/DIV	500 μSEC/DIV
E	20V/DIV	500 μSEC/DIV

Fig 11—In these waveforms for Fig 10's amplifier, *trace A is the amplifier's input, traces B and C the 1731's outputs and trace D the waveform across the load. Trace E, a 3-kHz filtered version of trace D, shows that power density approximates input signal.*

removed (as in a refrigerator) or added (as in a crystal oven). But because the Peltier device is thermodynamically bidirectional, it's an ideal choice for use in a low-temperature servo.

When power is applied, the platinum sensor (at a high resistive value) unbalances the bridge and causes the AD524 instrumentation amplifier to saturate negatively. This action turns the 1731 and its 1635 drivers on, resulting in current flow through the Peltier device in the cooling direction. When the temperature reaches 0°C, the 1731 tends to cut off, causing loop overshoot. However, the heat-pump reversal in the Peltier device forces short thermal settling times.

The 100-kΩ potentiometer adjusts loop gain; the 1-μF capacitor sets bandwidth. The 100-kΩ resistors and the 0.01-μF capacitor across the instrumentation amplifier filter out the fast chopping noise the platinum sensor, a wirewound device, picks up.

If you use the resistance decade shown, you can control the junction at any desired temperature around 0°C. For an ideal 1000Ω sensor at 0°C, the **table** values shown in **Fig 9** apply. You can substitute the actual 0°C value for the platinum sensor used, biasing all values by the difference between the sensor resistance at 0°C and 1000Ω. The bidirectional thermal control and high loop gain produce very rapid response to any shift in temperature setpoint, plus high stability.

Finally, the SG1731's 2-quadrant capability allows its use as a switched-mode (Class D) power amplifier. Motors and other devices that can integrate the time-power spectrum of a Class D amplifier output are obvious loads. The design can also serve audio applications but requires careful attention to output filtering to achieve acceptable distortion levels.

Fig 10 shows the 1731 set up to deliver high power to a 10Ω load via complementary power FETs. The device's output stage swings ±25V, providing a 10V enhancement for turning on the FETs. The active 1731 outputs are ideal for driving power FETs because they can both source and sink the relatively high gate currents caused by the FETs' input capacitances. **Fig 11** shows the waveforms associated with this circuit. **EDN**

The big picture

The applications described in this article only scratch the surface of the SG1731's capabilities. For more information and a data sheet, **Circle No 684.**

Authors' biographies

Jim Williams, now an applications manager specializing in analog-circuit and instrumentation development at Linear Technology Corp (Milpitas, CA), was a consultant when this article was written. Before joining the firm, he served in a similar capacity at National Semiconductor Corp, was a consultant at Arthur D Little Inc and directed the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art and collecting antique scientific instruments in his spare time.

Stan Dendinger is manager for advanced product development at Silicon General Inc (Garden Grove, CA). There, he is responsible for the development and improvement of several of the firm's regulating pulse-width-modulator ICs. Stan holds a BSEE degree from the University of California at Berkeley. He is also a professional choral singer and enjoys modifying sports cars as a hobby.

Article Interest Quotient (Circle One)
High **485** ***Medium*** **486** ***Low*** **487**

ANALOG DESIGN

Bipolar IC op amps enhance circuit precision

If traditional bipolar op amps don't meet your circuits' stringent performance needs, consider two new ICs that provide increased accuracy and suit varied uses.

Jim Williams, Linear Technology Corp

You can take advantage of two new bipolar IC op amps to improve measurement- and control-circuit precision. These devices, the LT1001 and LT1002, provide better bias, offset and common-mode parameters than do their predecessors (see **box**, "Latest op amps offer performance improvements"). Thus, they suit use in in a variety of critical applications—such as signal conditioners, battery chargers, motor positioners and voltage references.

Consider, for example, **Fig 1a**'s strain-gauge conditioner. In addition to exploiting the LT1002's low offset and drift, this differential-input circuit employs a novel switched-capacitor front-end stage that achieves performance not available from typical instrumentation amplifiers. For instance, the front end provides a dc common-mode rejection ratio (CMRR) that exceeds 160 dB, furnishes a ±300V common-mode range and provides gain accuracy and stability limited only by external resistors. As a result, the circuit withstands the severe transient and fault conditions often encountered in industrial environments.

Two series-connected pairs of LED-driven, optically coupled MOSFET switches (S_1 through S_4) form the heart of the switched-capacitor front end. During data-acquisition cycles, S_1 and S_2 close, allowing a 1-μF polypropylene capacitor (C_1) to charge to the bridge's differential level.

During data-read cycles, S_3 and S_4 close, and C_1 charges a 0.2-μF capacitor (C_2) that connects to op amp A_1's noninverting input. A 10-kΩ resistor (R_1) reduces data-read errors by requiring several clock cycles for C_2 to charge to C_1's constantly refreshed bridge-output level. A_1's feedback resistors scale C_2's voltage to provide 0 to 10V outputs for 0 to 30-mV differential bridge voltages. A 0.1-μF feedback capacitor sets the circuit for 5-Hz low-pass response.

Because only the bridge's differential voltage appears at A_1's inputs, the circuit's common-mode range depends only on the switches' maximum-voltage rating. Note, however, that at high voltages, the switches' 3-μA max leakage current might introduce output errors.

To ensure that data-acquisition and -read switches never close simultaneously, amplifier A_2 and its associated CMOS logic components generate precise, nonoverlapping 93-Hz clocks. **Fig 1b**'s trace A shows the circuit's data-acquisition pulse; trace B illustrates the data-read pulse. When the data-acquisition pulse goes LOW, S_1 and S_2 turn on and S_3 and S_4 turn off. The delay between data-acquisition falling edges and data-read

rising transitions ensures that S_1 and S_2 turn off fully before S_3 and S_4 begin to conduct. Trace C shows the voltage across the data-acquisition switches' drive LEDs.

A_3 and Q_2 provide the bridge's 10V excitation level by amplifying an LM329's 6.9V reference output. During data-acquisition cycles, Q_1 conducts, passing the excitation voltage to the bridge. When data-read cycles begin, Q_2 grounds Q_1's base, thereby turning the excitation voltage off to reduce leakage through S_1 and S_2. While Q_2 clamps Q_1's base, an input diode drives A_3's inverting input HIGH; at the start of acquisition cycles, the diode unclamps A_2 and the op amp quickly drives Q_1's emitter to 10V. Switched and dc reference outputs support ratiometric connections to monitoring ADCs.

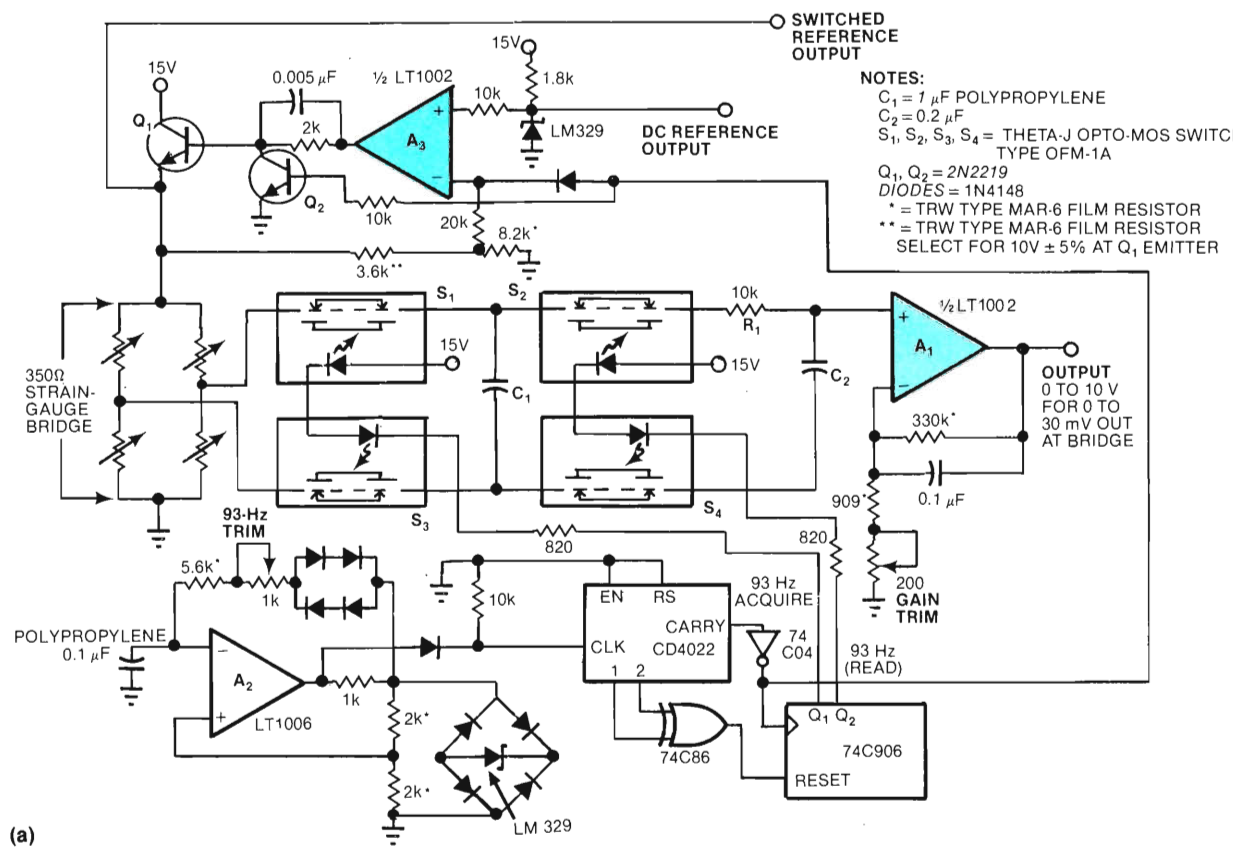
Note that because the trimmable 93-Hz switching frequency isn't harmonically related to the 60-Hz power lines, the circuit is insensitive to power-line-generated noise. In addition, the MOSFET switches' optical drive eliminates the charge-injection problems common to FET-drive switched-capacitor networks and therefore increases circuit precision. Unfortunately, though, the optical switches' 750-μsec state-change time limits the network's carrier to relatively low frequencies. But because strain-gauge bridge circuits don't condition rapidly changing signals, this problem remains minor.

Overcome thermal nonlinearity

Now suppose you want to make high-accuracy temperature measurements. Platinum resistance temperature detectors (RTDs) prove most stable in such applications, but their nonlinear temperature-vs-resistance characteristics complicate signal conditioning. Over a 0 to 100°C range, for example, the detectors' nonlinearity results in errors as great as 0.4°C. By using **Fig 2**'s circuit, though, you can compensate for such nonlinearity and thus achieve ±0.025°C absolute accuracy over a 0 to 100°C range.

In this circuit, A_1 functions as a fractional-gain inverter that forces a constant current through the 1-kΩ (at 0°C) platinum RTD. An LM329 and its associated 10-kΩ resistor provide the current reference. Because A_1 operates with a gain of less than unity, only a low voltage appears across the RTD, and self-heating-induced errors remain small.

A_1's output, which varies with the RTD's tempera-

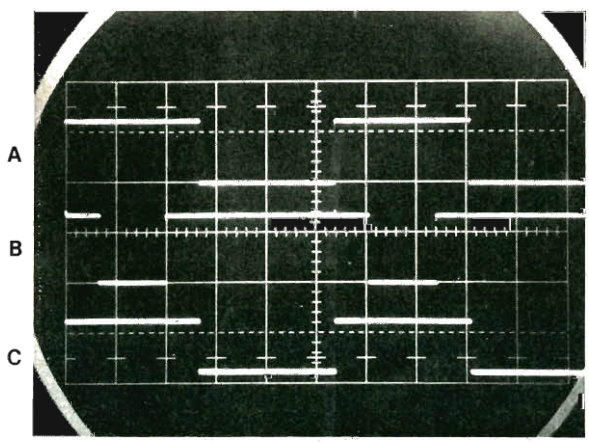


ture, feeds output amplifier A_2. This op amp furnishes scaled gain and offsets; its output swings over precisely 0.000 to 10.000V for 0.00 to 100.00°C RTD changes. A_2's 1-μF feedback capacitor limits noise pickup.

Normally, RTD-based thermometers exhibit 0.4°C nonlinearity errors because of imperfect sensor response. In this circuit, however, a small portion of A_2's output gets returned to A_1's inverting input. This feedback corrects nonlinearity errors by dynamically changing the circuit's reference current, thus introducing compensatory variations in the thermometer's gain slope.

To calibrate the thermometer circuit, substitute a precision decade-resistance box (such as a GenRad Model 1432-K) for the RTD. Then set the box to 1000.0Ω—a resistance that corresponds to the RTD's 0°C value—and adjust the 20-kΩ offset trimmer for 0.000V at the circuit's output terminal.

Next, set the decade box to 1138.7Ω (the RTD's 35°C resistance) and adjust the 20-kΩ gain trimmer for a 3.500V circuit output. Finally, set the box to 1392.6Ω (the RTD's 100.00°C value) and adjust the 200Ω linearity trimmer for a 10.000V output. After performing each calibration step once, repeat the procedure until all three outputs are stable and the error over the entire temperature range remains less than ±0.025°C.



(b)

TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	2 mSEC/DIV
B	10V/DIV	2 mSEC/DIV
C	10V/DIV	2 mSEC/DIV

Fig 1—A precision op amp *combines with four LED-driven optically coupled MOSFET switches to form a strain-gauge-bridge conditioner with a dc common-mode rejection ratio that exceeds 160 dB* ***(a).*** *The scope photo* ***(b)*** *illustrates the circuit's performance: Data-acquire and -read pulses (traces A and B) control the differential-to-single-ended signal transition performed by the MOSFET switches and their associated capacitors. The LEDs' optical drive (trace C) eliminates the charge-injection problems common to FET-based switched-capacitor networks.*

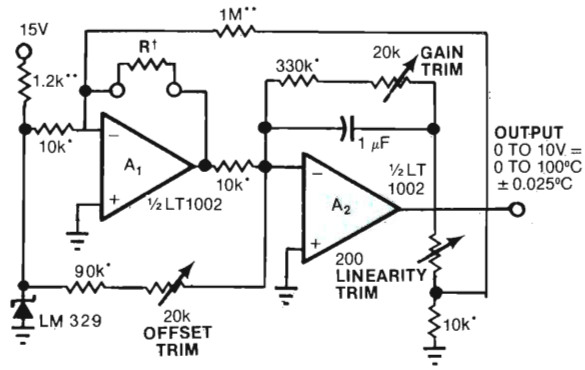


Fig 2—An op-amp-based thermometer *corrects for a platinum resistance temperature detector's (RTD's) nonlinear response. This circuit provides ±0.025°C absolute accuracy over a 0 to 100°C measurement range.*

Note that the decade-resistance-box values are equivalent to a nominal 1000.0Ω at 0°C RTD sensor levels. You can accommodate sensors that deviate from these nominal values by factoring in the deviation from 1000.0Ω. RTD manufacturers typically supply deviation data in a form that expresses the offsets resulting from fabrication tolerances. Other errors—such as deviations arising from material impurities—remain negligible.

Control battery charger thermally

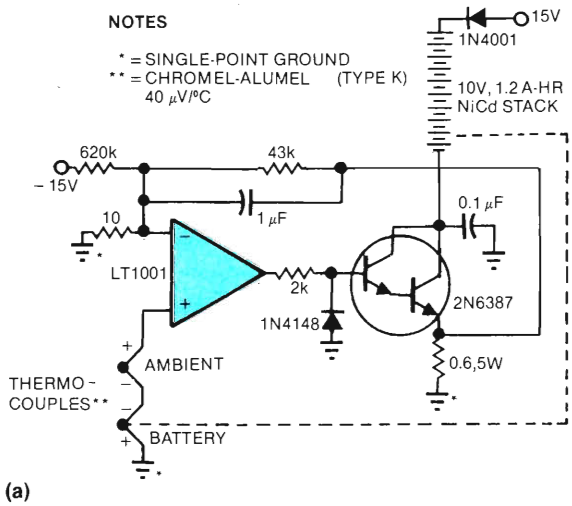
Another heat-measuring application involves the use of thermocouples to determine battery-cell temperatures. Charging NiCd batteries, for example, calls for high currents and short cycle times. Unfortunately, these requirements usually result in excessive internal heating that degrades battery performance and causes gas to escape into the atmosphere. Traditional charging schemes that involve monitoring cell voltages for fixed, high-charge-rate intervals alleviate some problems. But because cell voltages don't necessarily indicate battery charge states, open-loop schemes don't account for battery-characteristic shifts arising from aging and ambient-temperature effects.

Fig 3a's thermocouple-based circuit overcomes these limitations by monitoring battery-cell temperatures and tapering charge rates accordingly. As a result, it rapidly charges NiCd batteries without accelerating their aging. In addition, a second thermocouple nulls

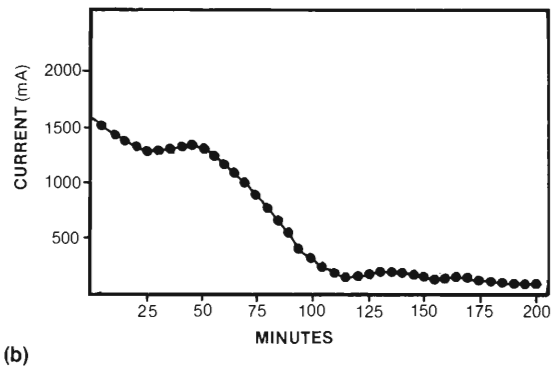
Signal-conditioning amplifier minimizes nonlinearity

the effects of ambient-temperature variations.

To understand the circuit's operation, assume that a discharged 10V NiCd battery pack is connected to the charger's 2N6387 Darlington-transistor pair. The battery thermocouple mounts directly to a battery cell, and the ambient thermocouple attaches to an object having a thermal mass approximating that of the battery pack. Under these conditions, both thermocou-

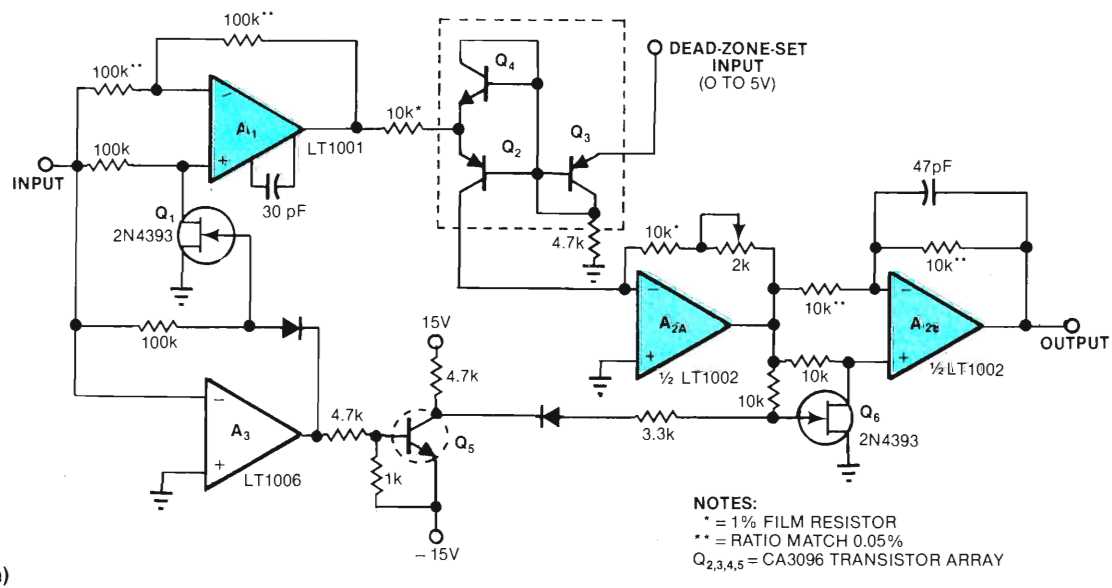


(a)



(b)

Fig 3—A thermally controlled NiCd-battery charger (a) *monitors cell-to-ambient temperature differences and adjusts charging currents accordingly. A current-vs-time plot* ***(b)*** *shows that a 10V, 1.2-Ahr battery draws a high charging current until internal heating occurs. Then the closed-loop control stage tapers the charging-current flow.*



(a)

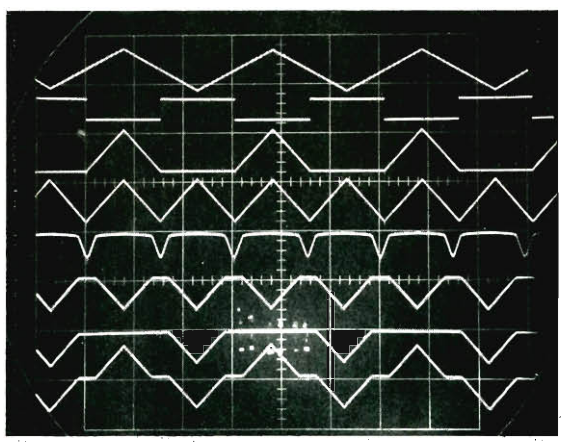
Fig 4—Suiting use in motor-driven servo positioners, *this op-amp circuit* ***(a)*** *generates an adjustable, symmetrical dead band. Thus, it allows accurate control of servo-motor stiffness and hunting characteristics around system null points. The scope photo* ***(b)*** *illustrates the operation of the circuit's precision rectifier (traces A, B, C and D), dead-band generator (traces E and F) and output demodulator (traces G and H).*

ples remain at the same temperature, and their output voltages cancel. Thus, the op amp's noninverting input remains at 0V.

At a charge cycle's beginning, a 620-kΩ resistor connected from V− to A_1's summing junction causes the op amp's output to swing positive. The Darlington pair then turns on, and current flows from the 15V supply through the battery pack and then to ground via the 0.6Ω shunt resistor. Consequently, the shunt's voltage rises, and the op amp causes approximately 1.6A to flow through the battery pack.

As the battery charges, it generates heat. The battery-mounted thermocouple detects the resulting temperature rise, and the potential difference between the two thermocouples establishes a small negative voltage at the op amp's noninverting input. For example, a 1°C difference between the two thermocouples generates a 40-μV noninverting-input level.

As the thermocouple voltage rises, the op amp balances its inputs by gradually reducing the current that flows through the battery (**Fig 3b**). Note that the battery charges at a high rate until heating occurs; then, circuit feedback tapers the charge rate, limiting the battery's surface-temperature rise to approximately 5°C above ambient level. The LT1001's low offset and drift ensure that the small thermocouple voltages resulting from such minimal temperature elevations accurately determine charge rates.



TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	500 μSEC/DIV
B	50V/DIV	500 μSEC/DIV
C	5V/DIV	500 μSEC/DIV
D	5V/DIV	500 μSEC/DIV
E	2V/DIV	500 μSEC/DIV
F	5V/DIV	500 μSEC/DIV
G	5V/DIV	500 μSEC/DIV
H	5V/DIV	500 μSEC/DIV

(b)

Dead-band circuit drives servo motor

Temperature monitors aren't the only circuits that benefit from the LT1001 and LT1002's precision; other applications for the op amps include servo-motor positioners. These circuits require the generation of precision, adjustable, symmetrical dead bands that control a servo motor's null-point response. Because dead-band stages often precede high-gain servo amplifiers, though, they must exhibit only small dead-band offsets.

Fig 4a details a precise, adjustable dead-zone circuit that includes a synchronous rectifier (A_1 and A_3); a variable unipolar dead-zone cell (A_{2A}, Q_2 and Q_4); and a demodulator (A_{2B}). To understand the circuit's operation, consider that a triangle wave (**Fig 4b**, trace A) drives the input. Comparator A_3 senses the waveform's polarity (trace B) and causes Q_1 to alter A_1's operating mode. When the input signal swings to negative levels, A_3's output goes HIGH, Q_1 conducts, and A_1 becomes a unity-gain inverter. Positive-going inputs drive A_3's output LOW, thus cutting off Q_1 and causing A_1 to function as a noninverting buffer (trace C). As a result, this synchronous-rectification stage presents the dead-zone cell with a unipolar input signal (trace D).

A_1's output feeds a voltage-adjustable current source (Q_2) that drives current-to-voltage converter A_2's summing node. Q_4 protects Q_2's base-emitter junction against reverse bias, and Q_3 provides the current-source network with V_{BE} temperature compensation.

When the dead-zone-set input at Q_3's emitter reaches a level greater than A_1's output, Q_2 turns off (trace E) and A_{2A}'s output goes to zero. Conversely, when A_1's output exceeds the dead-zone-set input, Q_2 conducts and A_{2A} operates as a current-to-voltage converter. A_1's inverted output thus appears at A_{2A}'s output, except with the region within the deadband removed (trace F).

To recover the bipolar input signal, a synchronous demodulator formed by A_{2B} and Q_6 alters the polarity of A_{2A}'s output signal in the same way that A_1 and Q_1 change input-signal polarities. Transistor Q_5 inverts A_3's output, causing Q_6 to turn on and off as Q_1 switches off and on. In this manner, A_{2B} inverts A_{2A}'s signal when the input swings positive; it operates in a noninverting mode (trace G) for negative-going inputs. Thus, the circuit generates a replica of the original input waveform but inserts a user-definable dead band (trace H).

Because one transistor (Q_2) processes both positive and negative signals, **Fig 4a**'s circuit produces nearly ideal dead-zone symmetry. And because Q_2's V_{BE} drop limits the minimum dead-band amplitude to 600 mV,

Control battery charging with a thermocouple-based amp

A_1's offsets don't propagate to the circuit's outputs, and A_3's delay and offset effects cause no errors. Therefore, only A_{2A} and A_{2B} must possess low offset voltages.

The LT1002 also excels when combined with a MOSFET-switched toroidal transformer in a precision variable voltage reference. This circuit (**Fig 5a**) provides simultaneous high- and low-voltage outputs with wide dynamic ranges and 10-ppm FS resolution. The circuit's low-voltage output spans 0 to 10V in 100-μV increments; the high-voltage range covers 0 to 100V in 1-mV steps.

The reference's low-voltage range derives from a noninverting gain stage (A_1) driven by an LM199 6.9V reference. A panel-mounted Kelvin-Varley-divider (KVD) circuit sets the range's output level, and a 2N2219 output transistor (Q_1) boosts the circuit's output capability. A_1's noninverting operation ensures that the KVD drives a high-impedance load; the op amp's low-bias current and high CMRR allow error-free KVD buffering. Q_1's 100Ω collector resistor limits short-circuit output current.

To generate the circuit's high-voltage output, a multivibrator formed by comparator A_3 and its associated components produces a 40-kHz chopping clock. This signal gets divided by a 74C74 flip flop, and the resulting complementary 20-kHz square waves bias two VN46 VMOS FETs. The FET switches contribute to the reference's wide dynamic range because their low

Latest op amps offer performance improvements

Careful product design, fabrication and testing allow the LT1001C (single) and LT1002C (dual) bipolar op amps to offer performance previously unavailable from moderate-cost precision ICs. Compared with existing industry-standard amplifiers (such as the OP-07 and OP-207), the two recently introduced devices furnish upgraded gain and accuracy specifications **(table)**.

Most significant among the op amps' enhanced specs are common-mode rejection rato (CMRR), power-supply rejection ratio (PSRR), signal gain (A_{VOL}) and power dissipation (P_D). For example, the $2.60 (100) LT1001C's 110-dB CMRR represents a threefold improvement compared with the OP-07's performance. And the LT1001/1002's 106-dB PSRR betters the OP-07's characteristics by a factor of six. Moreover, the LT1001C doubles the OP-07E's open-loop dc gain and exhibits no gain glitch, even when sinking 6- to 8-mA load currents.

Power-dissipation comparisons also favor the LT1001C by at least 33%. Moreover, the op amp's reduced dissipation entails no slew-rate or gain-bandwidth-product losses. Similarly, the $5 (100) LT1002C's key specs equal or exceed OP-207's published specifications.

For more information on these two op amps, **Circle No 727.**

OP-AMP SPECIFICATION COMPARISONS

PARAMETER	LT1001C	OP-07E	OP-07C	UNIT
V_{OS}	60(15*)	75	150	μV
$\Delta V_{OS}/\Delta T$	1.0	1.3	1.8	μV/°C
I_B	4	4	7	nA
I_{OS}	3.8	3.8	6	nA
CMRR	110	106	100	dB
PSRR	106	94	90	dB
GAIN(R_L = 2k)	400	200	120	V/mV
GAIN(R_L = 1k)	250	N/A	N/A	V/mV
P_D	80	120	150	mW

PARAMETER	LT1002C	OP-207E	OP-207F	UNIT
V_{OS}	100	100	200	μV
$\Delta V_{OS}/\Delta T$	1.3	1.3	1.8	μV/°C
CMRR	110	106	100	dB
PSRR	106	94	90	dB
A_{VOL}	350	200	150	V/mV
GBW	0.5	0.6(TYP)	0.6(TYP)	MHz
SR	0.15	0.2(TYP)	0.2(TYP)	V/μSEC
P_D	85	120	150	mW

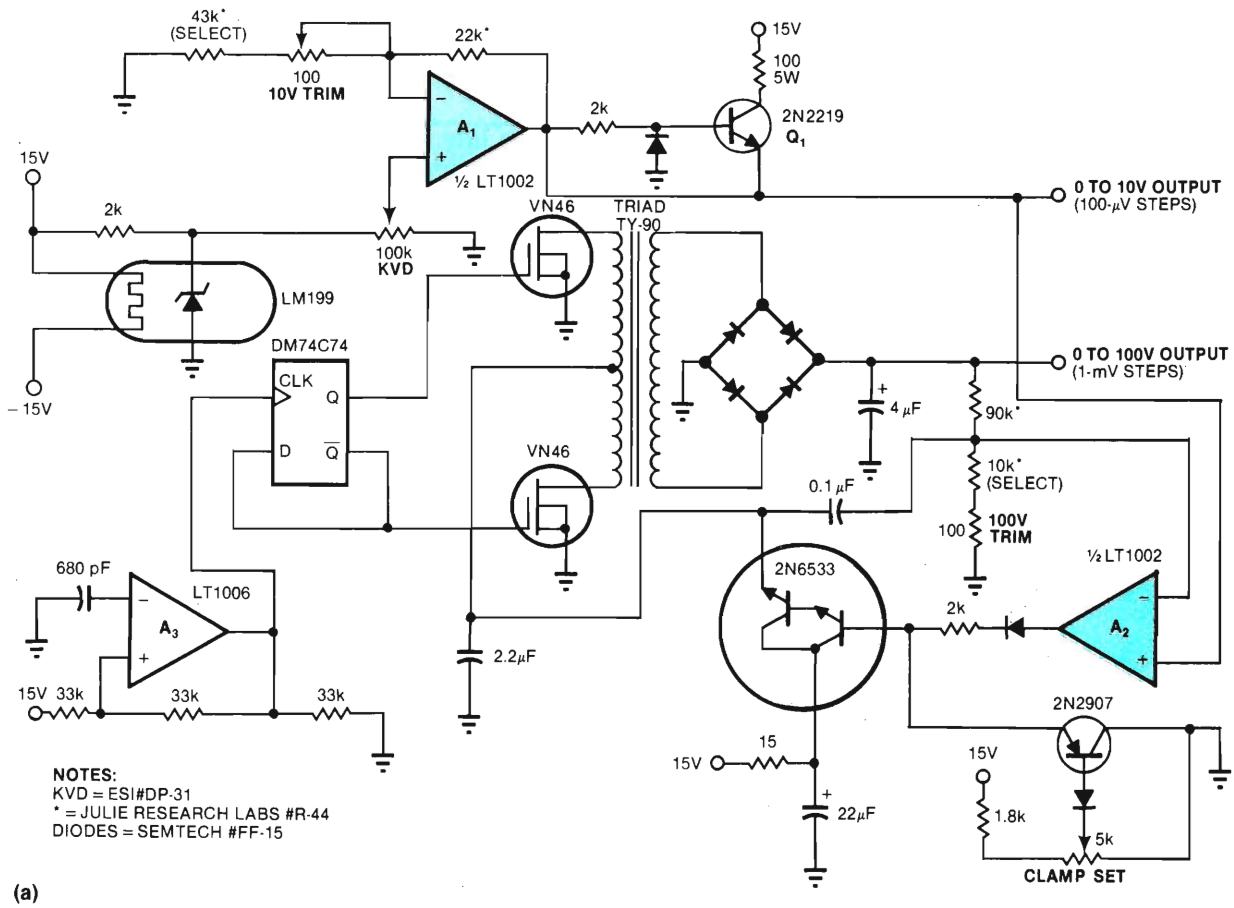
NOTES:
*MILITARY GRADE WITH 883B PROCESSING (LT 1001AM/883).
ALL SPECIFICATIONS ARE MAX AND MIN UNLESS OTHERWISE NOTED FOR V_{CC} = ± 15V.

Servo-controlled circuit furnishes dual references

saturation resistance results in controlled output resolution for levels as low as 1 mV.

Op amp A_2 compares the transformer/rectifier/filter combination's divided output with the low-voltage output. The amplified difference voltage biases a 2N6533 power Darlington that closes a feedback loop around the transformer by driving the toroid's primary center tap. By selecting the high-voltage divider's resistors, you can calibrate the loop for precise 0 to 100.00V outputs that correspond to KVD dial settings. A 1-μF capacitor around A_2 and the power Darlington stabilizes the feedback loop, and a 2N2907 transistor serves as a coarse voltage clamp for the high-voltage output. The clamp allows you to establish a maximum output voltage level.

To calibrate the voltage-reference circuit, you must



(a)

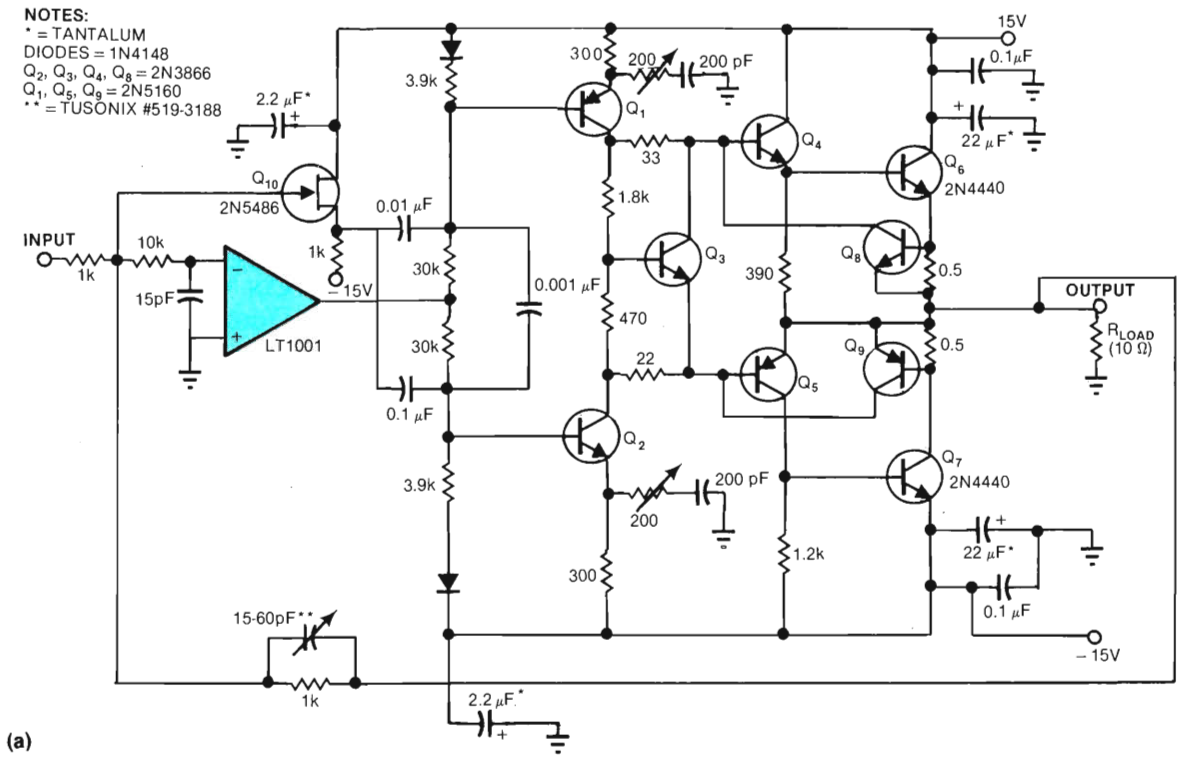
LOW AND HIGH VOLTAGE RANGE ERRORS

10V RANGE		100 V RANGE	
ZENER TEMPERATURE DRIFT: 5°C × 0.2 PPM/°C	= 1 PPM	10V RANGE ERRORS	= 36 PPM
ZENER TIME DRIFT/YEAR	= 25 PPM	A_2 TIME AND TEMPERATURE ERRORS	= 0 PPM
A_1 OP AMP E_{os} DRIFT: 0.5 μV/°C × 5°C × 1.4 = 3.5 μV	= 0 PPM	TOTAL ERROR (FULL SCALE)	= 36 PPM
A_1 OP AMP E_{os} TIME DRIFT: 1 YR = 10 μV/YR	= 0 PPM		
KVD: 2-PPM/°C RATIO SHIFT × 5°C	= 10 PPM		
TOTAL ERROR: OVER ± 5°C AND 1YR (FULL SCALE)	= 36 PPM		

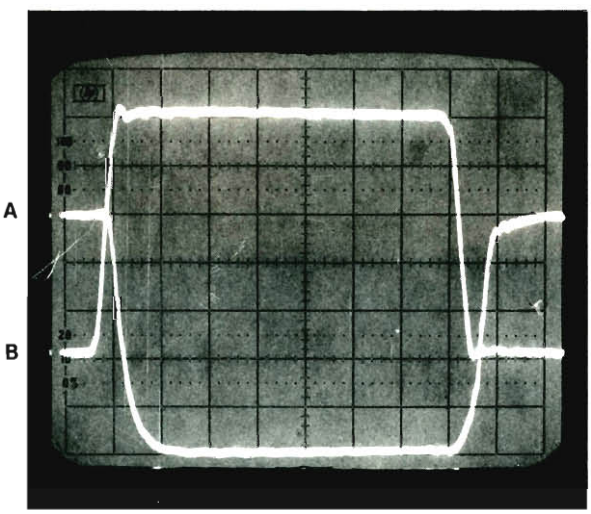
(b)

Fig 5—An ultraprecise variable voltage reference (a) *provides dual ranges: A 0 to 10V low-voltage span features 100-μV resolution, and a 0 to 100V high-voltage range furnishes 1-mV steps. The table* ***(b)*** *summarizes the circuit's post-calibration errors.*

Achieve dc accuracy and speed with a combination circuit



(a)



TRACE	VERTICAL	HORIZONTAL
A	2V/DIV	10 μSEC/DIV
B	2V/DIV	10 μSEC/DIV

(b)

Fig 6—Both high speed and dc accuracy result *when a precision op amp stabilizes a high-frequency broadband amplifier. This circuit* ***(a)*** *features ±1A drive capability, 8-MHz power bandwidth and 350-nsec settling to 0.1%. The scope trace* ***(b)*** *illustrates the amplifier's 1000V/μsec compensated slewing.*

first select A_1's input resistor. (For 0 to 10V low-voltage outputs, a 43-kΩ resistor proves best.) Then adjust the 100Ω trim resistor for a 10.0000V low-voltage output with the KVD dials set to full scale. A_1's low offset voltage eliminates the need for an offset trim.

Next, set the high-voltage output range by choosing A_2's input resistor; for 0 to 100V high-voltage outputs, use a 10-kΩ unit. Now adjust the 100Ω high-voltage-trim resistor for a 100.00V output with the KVD set for full scale. **Fig 5b** summarizes the voltage reference's post-calibration errors.

Low-drift bipolar op amps such as the LT1001 and LT1002 can also improve the precision of high-speed, high-current circuits. Traditionally, precision circuits have sacrificed speed and output-drive capability in favor of dc accuracy. Most dc-stable circuits operate only at relatively low frequencies, and self-heating problems have limited precision-circuit output-current capabilities. Now, however, you can satisfy seemingly conflicting performance requirements with a precision high-speed op amp that provides 1A output-drive capability, 350-nsec settling to 0.1% and 850-nsec settling to 0.01%.

In this circuit (**Fig 6a**), an LT1001 stabilizes a broadband stage; the composite amplifier exhibits the

Decoupling capacitors complete the design

op amp's high accuracy and functions with the broadband circuit's speed. The amplifier features a 1500V/μsec max slew rate, full-power output to 8 MHz and ±10V drive into 10Ω loads. Moreover, it offers ±1A short-circuit protection.

To combine precision and high speed, the composite amplifier includes a feedforward path that routes high-frequency signals around the relatively slow LT1001. Low-frequency signals pass through the input op amp, though, so the overall circuit's dc characteristics depend only on the LT1001's performance.

The discrete high-speed stage employs signal transistors with operating frequencies approaching 1 GHz; its output buffer comprises two npn RF power transistors arranged in a quasicomplementary output configuration. (High-speed pnp power transistors aren't currently available.) Transistors Q_8 and Q_9 limit short-circuit current by sensing voltage drops that develop across 0.5Ω-resistor shunts. When they're turned on, the limiting transistors furnish degenerative feedback around the output stage, restricting output-current flow.

To trim **Fig 6a**'s circuit, adjust the 200Ω compensation trimmers and the 15- to 60-μF variable feedback capacitor for a tradeoff between slew rate and output settling. **Fig 6b** illustrates the amplifier's optimum response (trace B) to a fast input pulse (trace A). When properly trimmed, the circuit slews at 1000V/μsec, and its output appears clean to within the resolution of a 275-MHz monitoring oscilloscope. For best results, construct this circuit using proven RF-layout techniques, and furnish ground planes and heat sinks for the 2N4440 transistors. **EDN**

Author's biography

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in related capacities at National Semiconductor Corp, Arthur D Little Inc and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art and collecting antique scientific instruments in his spare time.

Article Interest Quotient (Circle One)
High **476** ***Medium*** **477** ***Low*** **478**

Basic circuit-design techniques yield stable clock oscillators

Almost all digital or communication systems require some form of clock source, and while generating accurate and stable clock signals is often a difficult design problem, it's not impossible.

Jim Williams, Linear Technology Corp

All too often, designers consider clock-oscillator design to be some sort of black art—especially when it comes to crystal-based circuitry. This article proves that such designs are not necessarily so mysterious. By using good basic design techniques, you can readily generate clock sources for a variety of applications. Because quartz crystals are the basic building blocks for most clock sources, the discussion will start by highlighting several designs.

There's no black magic involved

High-performance crystal-oscillator circuit design demands a variety of complex considerations and subtle implementation techniques. Nevertheless, most applications don't require this level of attention and are relatively easy to serve. In fact, crystal-based clock-circuit designs can be quite simple (**Fig 1**).

The first four circuits ((**a**) through (**d**)) are commonly called gate oscillators. In (**a**), the 2-MΩ resistor biases the CMOS Schmitt trigger into its linear operating region. The capacitor adds phase shift and the circuit oscillates at the crystal's resonant frequency—100 kHz. **Fig 1b** shows a similar design that oscillates at 1 MHz. The CMOS gate provides inverting gain with the capacitors supplying the additional phase shift to produce oscillation. Higher frequency operation requires a TTL gate for the gain element (**Fig 1c**). Note that because TTL elements have low input impedance, it's no longer possible to use a single-resistor biasing scheme. In this case, the RC T-network establishes the gate's bias point. In the oscillator circuit (**Fig 1d**), the two linearly biased gates provide a 360° phase shift with the crystal providing the feedback path. The capacitor simply blocks dc in the gain path.

Gate oscillators not perfect

While gate oscillators are quite popular, they can cause problems ranging from temperamental operation to lack of oscillation. The gain elements are the primary problem source—it's not possible to reliably identify the analog characteristics of digital gates. For example, there's no guarantee that gates from various manufacturers will produce the same results when plugged into the oscillator circuit. In other cases, the circuit will work but the status of other gates within the package will affect its performance. Finally, some circuits seem to favor certain gate locations within the IC package.

Given these difficulties, gate oscillators are not the best possible choice in a production design. They deserve mention, however, because they do feature low component count and they can satisfy noncritical applications.

Other routes to low parts count

Not all single-stage oscillator circuits suffer such problems, however. **Fig 1e** illustrates a circuit design

Despite low parts count, gate oscillators are temperamental

using discrete components. Contrasted against the IC-based oscillators, it provides a good example of the design flexibility and certainty available with components specified in the linear domain.

This circuit will oscillate over a wide range of crystal frequencies—typically 2 to 20 MHz. The 2.2k and 33k resistors combine with the diodes to develop a pseudo current source that supplies base current. At 25°C, base current equals

$$(1.2V-V_{BE})/33k=18\ \mu A.$$

When the transistor saturates ($V_{CE}\approx 0$), oscillations will cease. Neglecting V_{CE} SAT, saturation will occur when

$$I_C\ SAT=5V/1k=5\ mA.$$

To develop this collector current with 18 μA of base drive, transistor dc beta must equal

$$5\ mA/18\ \mu A=278.$$

At 1 mA, beta spread for the 2N3904 specs at 70 to 210, so there's no problem with saturation—even at supply voltages below 3V.

In a similar fashion, you can calculate temperature effects. Over 25 to 70°C, V_{BE} will vary

$$-2.2\ mV/°C\times 45°=-99\ mV.$$

The compliance voltage of the current source will shift

$$2\times -2.2\ mV/°C\times 45°C=-198\ mV.$$

Hence a first-order compensation occurs and total V_{BE} shift equals

$$-198\ mV-99\ mV=-99\ mV.$$

This V_{BE} drift causes a shift in base current. At 25°C,

$$I_B=0.6V/33k=18\ \mu A.$$

At 70°C,

$$I_B=0.5V/33k=15\ \mu A.$$

This 3-μA drift (about 16%) compensates for the transistor's h_{FE} shift (about 20% from 25 to 70°C) with temperature. Thus, the circuit's behavior over temperature is quite predictable. Nevertheless, because of resistor, diode and V_{BE} tolerances, only first-order temperature compensations for h_{FE} and V_{BE} are appropriate.

Fig 2a shows another design approach. Here, the crystal is connected directly across the timing capacitor of a standard RC-comparator multivibrator circuit. Because the circuit's free-running frequency is close to the crystal's resonant frequency, the crystal steals

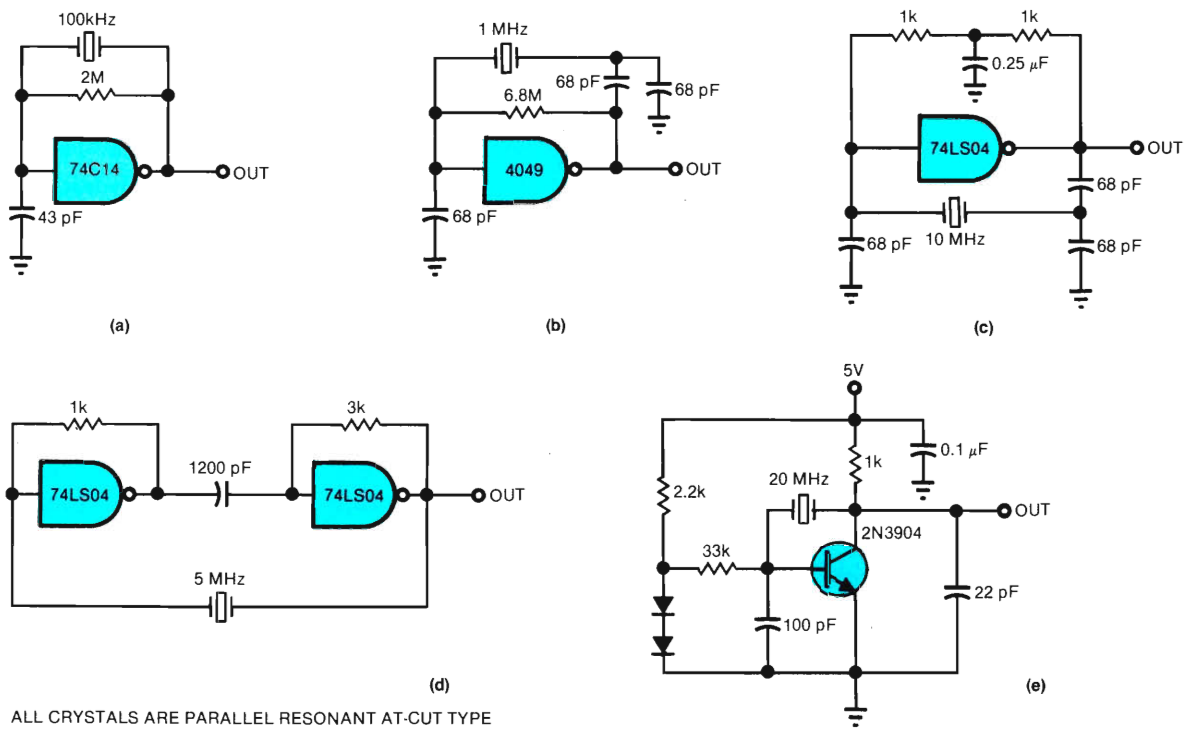


Fig 1—While they feature design simplicity, *the temperamental operation inherent in gate oscillators* ***((a)*** *through* ***(d))*** *makes them a poor choice for production designs. On the other hand, circuits based on discrete components* ***(e)*** *provide reliable operation from a small number of components.*

energy from the RC, forcing it to run at the crystal's frequency. Crystal activity at the LM311's input is readily apparent in trace A of **Fig 2b.**

In circuits of this type, it's important to ensure that enough current is available to start the crystal resonating quickly while still maintaining an appropriate RC time constant. *(Ed Note: The start-up resistance of crystals varies widely among manufacturers. Start-up resistance is normally higher than the crystal's series resistance and is usually not spec'd. Consult your crystal supplier about a low start-up-resistance crystal if your clock starts oscillating slowly or not at all.)* Typically, you should set the free-running frequency 5 to 10% above crystal resonance and set the feedback resistor to allow about 100 μA of current flow in the capacitor-crystal network. Comparator delays restrict this circuit's useful operating range to a few hundred kHz.

The circuits discussed to this point will typically feature temperature coefficients of 1 ppm/°C and 5- to 10-ppm long-term (1 yr) stability. Higher stability is achievable with more attention to circuit design.

Controlling temperature effects

Fig 3 shows a Pierce-type oscillator circuit with the paralleled fixed and variable capacitors allowing fine frequency trimming. The 2N3904 provides 180° of phase shift, and the loop components provide the additional 180° necessary for oscillation. The LT1005 voltage regulator and the LT1001 op amp combine for precise servo control of the crystal's temperature.

The LT1001 extracts the differential bridge signal and drives the Darlington stage to power the heater, which is monitored by the thermistor, Rt. In practice, you should tightly couple the sensor and the heater. You should also select RC feedback-network values to optimize the thermal characteristics of the oven. In this case, oven construction employs a 3.0×1.0×0.125-in. piece of aluminum tube stock. The heater windings are distributed around the cylinders and the assembly sits in a small insulating Dewar flask. This allows 75°C-setpoint (the zero TC or turnover temperature of the specified crystal) control of 0.05° over 0 to 70°C.

The LT1005 regulator provides the source for the bridge from its auxiliary output and also disables system power until the crystal's temperature (and hence its frequency) stabilizes. When the power is first applied, the thermistor has high resistance and causes the LT1001 to saturate positively. This turns on Q_2 (which is configured to act like a zener diode) and that, in turn, biases Q_3 ON. Q_3's collector current pulls the regulator's control pin low, disabling its output. When the oven arrives at its control point, the LT1001's output comes out of saturation and servo-controls the oven at a point well below Q_2's zener value. This turns off Q_3, enabling the regulator to supply power to the rest of the system.

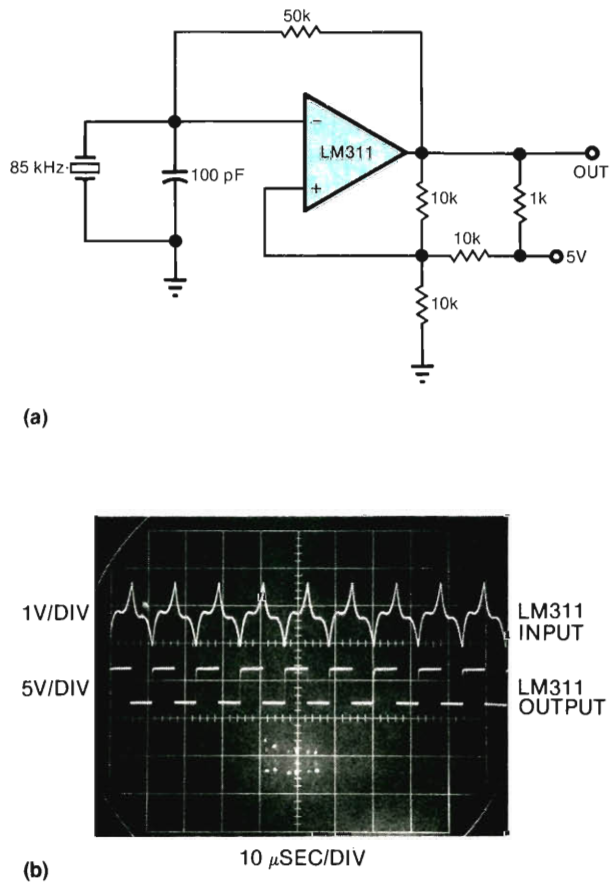


Fig 2—For low-frequency applications, *you can use a standard RC comparator/multivibrator circuit* ***(a)*** *to develop a clean clock signal* ***(b)****. Nevertheless, because of comparator delays, this type of circuit is not recommended for operation above a few hundred kHz.*

The oven approach is the most effective way of controlling temperature effects. For the crystal and circuit values shown, this clock will drift less than 5×10^{-9} over 0 to 70°C, with a time drift of 1 part in 10^{-9} per week. Ovens do require substantial power and warm-up time, however, and this is unacceptable in some cases.

Compensate for the problems

You can also offset temperature effects by measuring the ambient temperature and inserting a scaled compensation factor into the crystal clock's frequency-trimming network. To take advantage of this open-loop

Mechanical and electrical factors affect resonator performance

R¹—YSI ÷ 44014 (35.39k at 75 °C

*—TRW MAR-6

CRYSTAL—BLILEY #BG61AH-5S; 5 MHz, 75 °C TURNING POINT

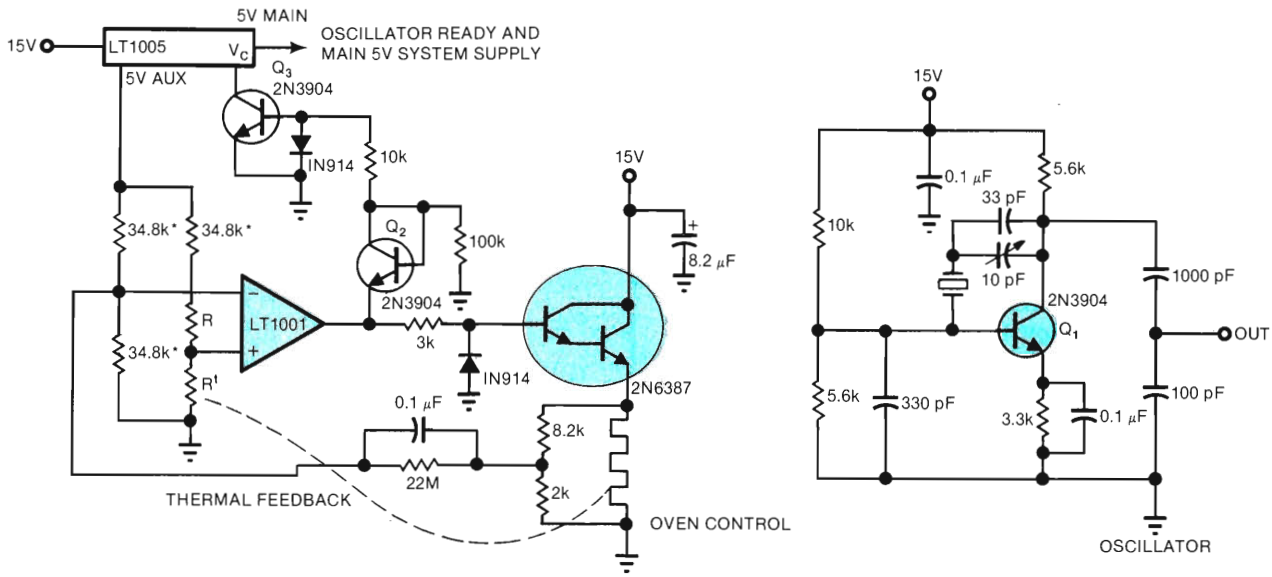


Fig 3—The oven approach is the most effective way *to minimize temperature-related clock-frequency drifts. This clock will drift less than* 5×10^{-9} *over 0 to 70°C.*

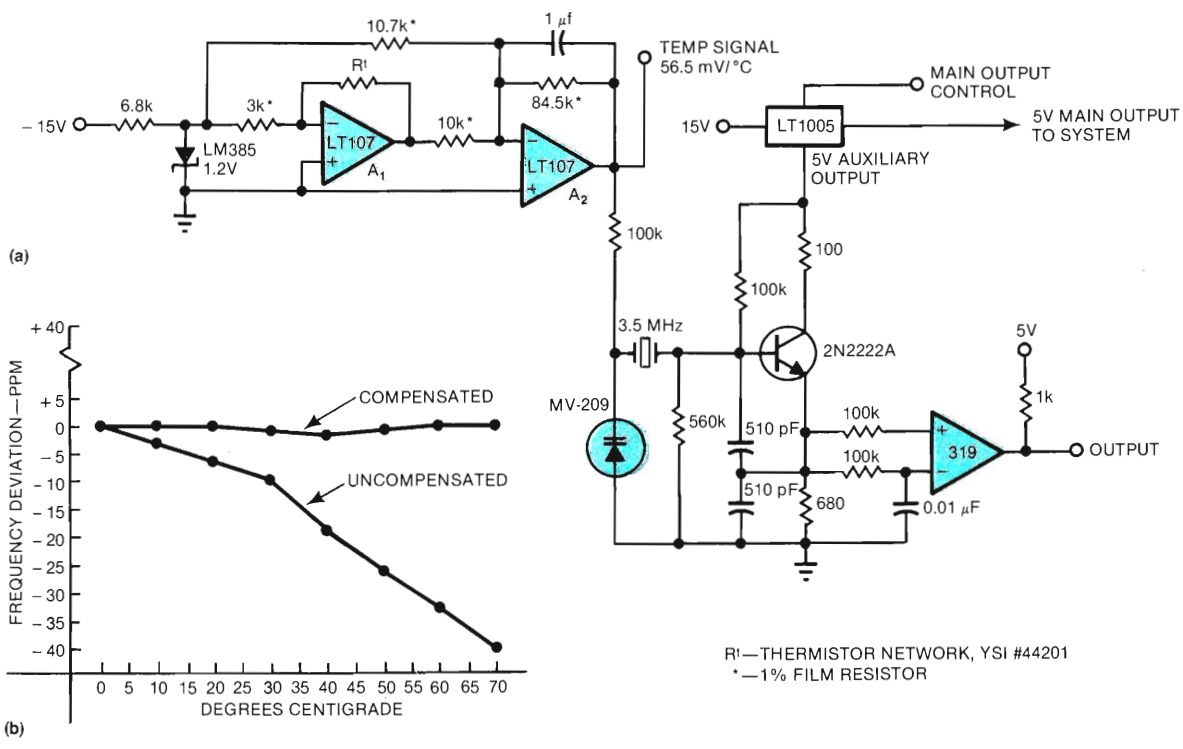


Fig 4—As an alternative to oven control, *this Colpitts-type crystal oscillator* ***(a)*** *uses a varactor diode to implement open-loop temperature compensation. As the results show* ***(b)****, the technique works quite well.*

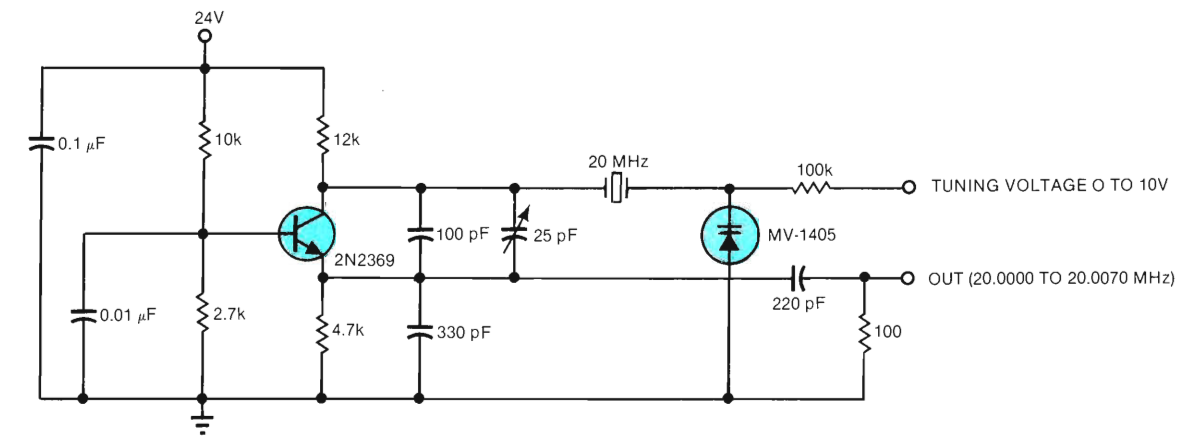
correction technique, you must be able to match the clock frequency versus temperature characteristic—a parameter that is quite repeatable.

Fig 4 shows a temperature-compensated crystal oscillator (TXCO), which uses a first-order linear fit for temperature compensation. The oscillator is a Colpitts type that approximates an emitter follower with a capacitively tapped tank network. The LM319 picks off the oscillator's output; the RC network at its inverting input provides a signal-adaptive trip threshold.

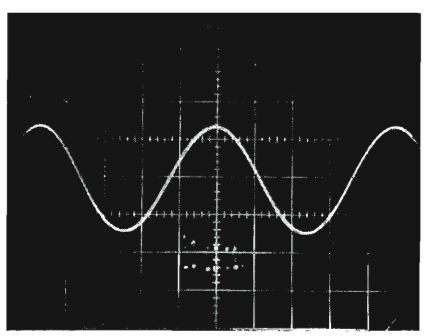
The LT1005 regulator's auxiliary output buffers supply variations and the main-regulator output-control pin lets you shut down the system without removing power from the oscillator—a feature that improves overall circuit stability. The linear thermistor network in A_1's feedback loop senses the ambient temperature while A_2 handles scaling and offset functions. A_2's voltage output also contains the ambient-temperature information required for clock compensation.

Correction is implemented by varying the bias of the varactor diode in series with the crystal, using the varactor's shift in capacitance to pull the crystal's frequency such that it cancels temperature-induced errors. If you keep the thermistor and the circuit at the same temperature, compensation is very effective (**Fig 4b**). The uncompensated −40-ppm frequency shift is corrected to within 2 ppm. You can achieve better compensation by including second- and third-order terms in the temperature-to-voltage conversion to more accurately mirror the nonlinear frequency-drift characteristic.

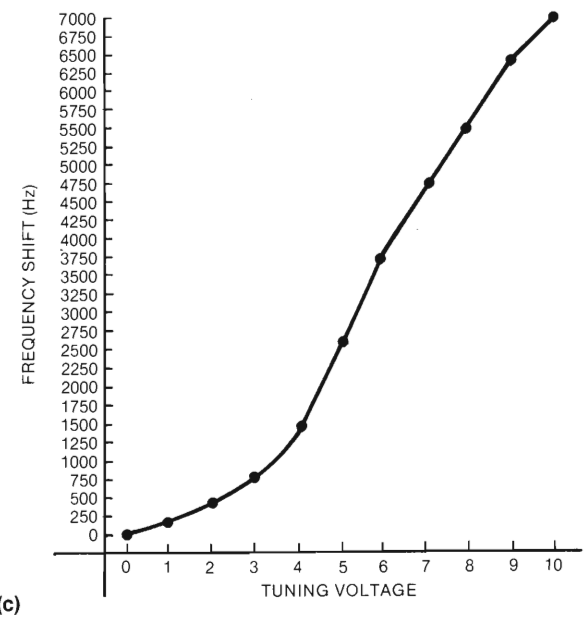
In a second varactor-based compensation scheme (**Fig 5a**), the circuit is configured to enable rather than



(a)



(b)



(c)

Fig 5—Configured to allow rather than oppose frequency shift, *this voltage-controlled crystal oscillator* ***(a)*** *has a clean 20-MHz sine-wave output* ***(b)****. While the output does show a 7-kHz drift over the 10V tuning range* ***(c)****, you can improve linearity by conditioning the varactor network's response.*

Crystal-based multivibrator clocks satisfy low-frequency needs

oppose frequency shift. This voltage-controlled crystal oscillator (VXCO) has a clean 20-MHz sine-wave output (**Fig 5b**) suitable for communications applications. Over its 10V tuning range, the oscillator shows a 7-kHz shift from center frequency (**Fig 5c**). The nonlinear response is irrelevant in many applications (phase-locking or narrow-bandwidth-FM secure communications, for example), but you can achieve better linearity by conditioning the tuning voltage or the varactor network's response.

In circuits of this type, it's important to remember that the crystal's Q limits the frequency pulling range. It is difficult to achieve a wide dynamic pull range without stopping the oscillator or forcing it into abnormal modes. Typical circuits like the one in **Fig 5a** offer pull ranges of several hundred ppm. You can

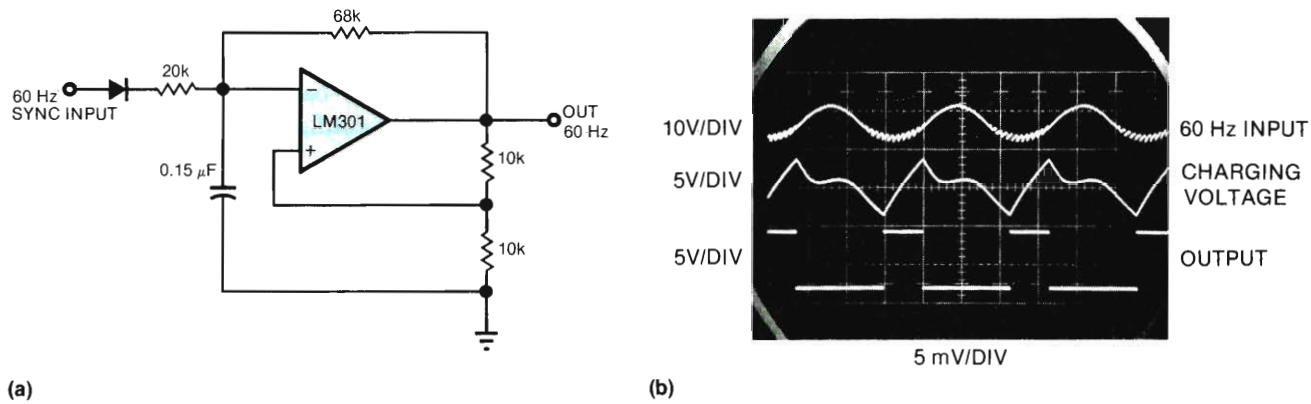


Fig 6—Tuned to free run near 60 Hz, *this synchronous clock* ***(a)*** *derives its noise-rejection capabilities from the RC network's integrator characteristics. Noise and fast spiking on the 60-Hz input* ***(b)*** *have little effect on the capacitor's charging characteristics or the circuit's output.*

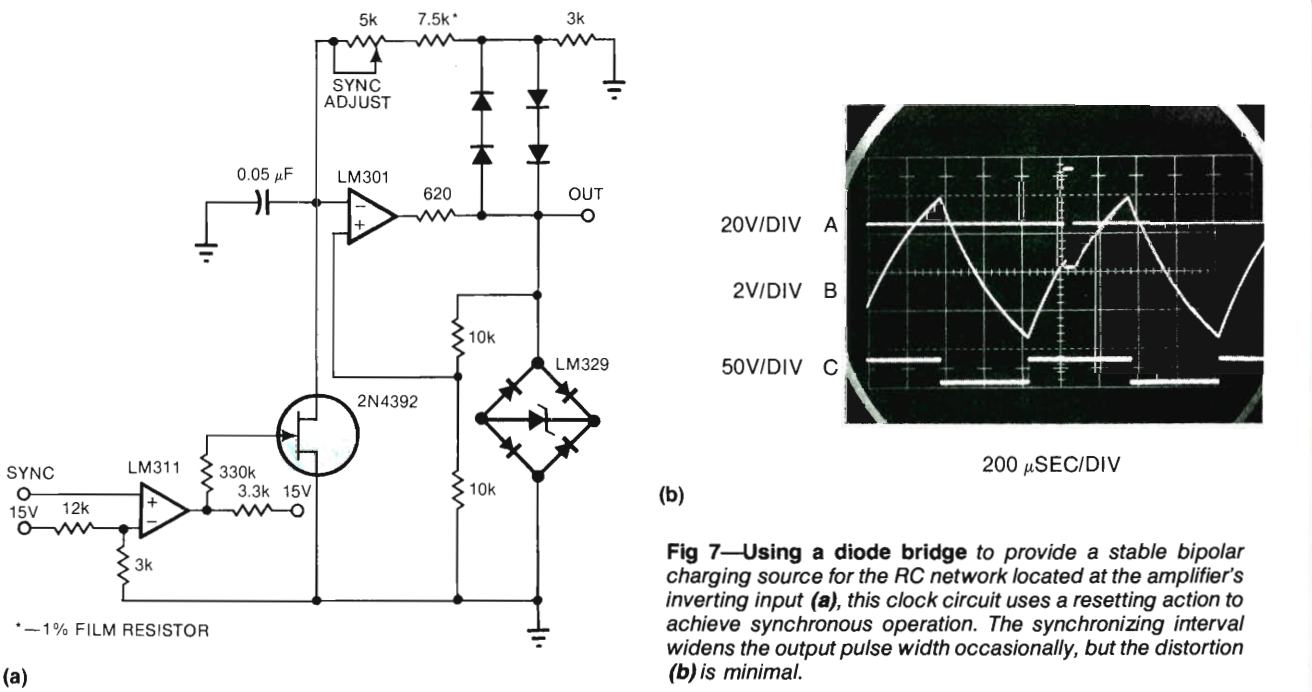


Fig 7—Using a diode bridge *to provide a stable bipolar charging source for the RC network located at the amplifier's inverting input* ***(a)****, this clock circuit uses a resetting action to achieve synchronous operation. The synchronizing interval widens the output pulse width occasionally, but the distortion* ***(b)*** *is minimal.*

Temperature-related output shifts are minimal with oven control

realize larger pull ranges (2000 to 3000 ppm) without losing crystal lock, but the clock's output-frequency stability suffers somewhat.

Although crystal-based circuits are universally applied, they cannot satisfy all clock requirements. As an example, many systems require a reliable 60-Hz synchronous clock. Some circuit solutions employ zero-crossing detectors or simple voltage-level detectors, but they have poor noise-rejection characteristics. There are better solutions.

Handling adverse environments

To develop a line-driven clock oscillator that accommodates adverse conditions, the circuit design should take advantage of the narrow bandwidth of the 60-Hz fundamental. Even if hysteresis is applied, design approaches using wide gain bandwidth invite noise-related problems. **Fig 6a** shows a synchronous clock that will not lose lock under noisy line conditions.

The basic RC multivibrator is tuned to free run near 60 Hz, but the synchronizing input locks the oscillator to the line frequency. The RC network's integrator characteristics provide the circuit's noise-rejection performance (**Fig 6b**). Noise and fast spiking on the 60-Hz input have little effect on the capacitor's charging characteristics, and the circuit's output is stable.

In a second synchronous-clock circuit (**Fig 7a**), operation is the equivalent of a reset-stabilized dc amplifier. In this instance, the circuit free runs at a frequency that's higher than the synchronizing input.

The LM301 and its associated components form a stable oscillator. The LM329 bridge combines with the compensating diodes to provide a stable bipolar charging source for the RC network at the 301's inverting input. The LM311 comparator level-shifts the synchronizing pulse (trace A, **Fig 7b**) to drive the 2N4392 FET. When the sync pulse increases, it turns on the 2N4392, which grounds the capacitor (trace B, **Fig 7b**) and interrupts normal oscillator action for a small fraction of a cycle. When the sync pulse falls, the capacitor's charge cycle (which has been reset to zero) starts again.

This resetting action synchronizes the RC charging frequency. Occasionally, the synchronizing interval in this operation will slightly enlarge the output pulse

About quartz crystals

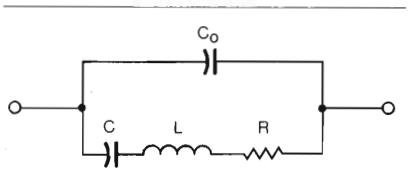
A quartz crystal's equivalent circuit **(figure)** is a series-parallel combination of elements. C_O defines the static capacitance produced by the contact wires, the crystal electrodes and the crystal holder. In the motional arm (the RLC term), C equals the mechanical mass, R includes all electrical losses in the crystal and L represents the reactive aspect of the quartz.

The electrical characteristics of individual crystals will vary as a function of the angle of cut from the mother crystal. These cuts are chosen to optimize temperature coefficient, frequency range and other parameters. The basic AT cut, used in most crystals in the 1- to 150-MHz range, provides a good compromise between optimum temperature coefficient and frequency range.

Mechanical and electrical factors combine to affect resonator performance. Mechanical factors include the method of lead attachment, package-sealing method and internal environment (eg, vacuum, partial pressure, etc). Electrical (circuit) considerations include load capacitance, crystal resistance, drive level, temperature coefficient/turning point and frequency tolerance.

Load capacitance defines the reactance the crystal must present to the circuit. In some circuits, the crystal operates in the parallel-resonant mode where it looks inductive. In other cases, the circuit operates at series resonance and the crystal appears resistive. In this mode, you must specify the circuit's load capacitance (including all parasitics). Typical values for load capacitance are around 30 pF.

Drive level is critical since the crystal can dissipate only limited power (10 mW typ) and still maintain all specifications. Excessive drive levels can fracture the crystal.



The crystal's temperature coefficient (TC) is usually specified near the turning point—the temperature at which the crystal TC equals zero. Typically, the turning point is around 75°C and TC will be less than 1 ppm/°C over the operating range. Different cuts, however, can alter these numbers considerably.

Frequency tolerance defines the deviation from ideal frequency, when the crystal operates under specified circuit conditions at a defined temperature. Tolerances range from 50 ppm to less than 1 ppm.

Crystal clocks are popular, but can't serve all applications

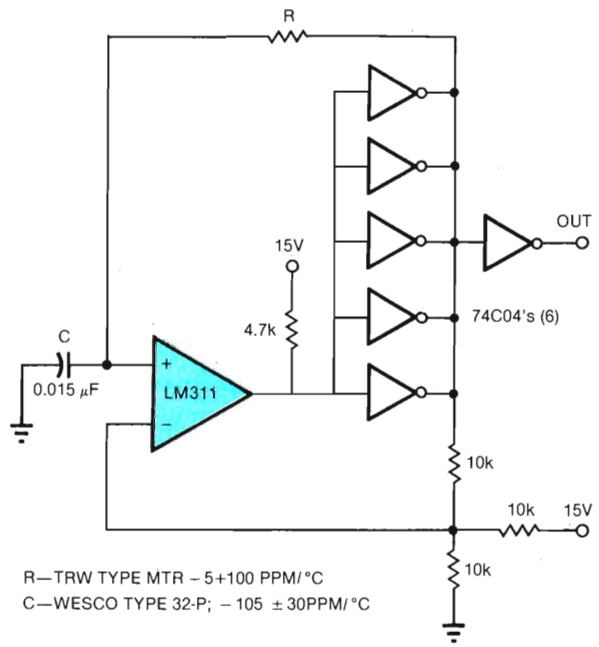


Fig 8—To make the capacitor's charge/discharge time constant *almost totally immune from supply and temperature shifts, this RC oscillator circuit employs paralleled CMOS inverters between the LM311 output and the feedback resistors.*

width (trace C, **Fig 7b**). Setting the potentiometer so that the sync pulse occurs when capacitor voltage is near zero will minimize output pulse-width deviation, and also provide maximum protection against lock loss due to RC drift over time and temperature. The maximum practical output-to-sync frequency ratio for this circuit is about 50.

Pure RC oscillators represent a final class of clock circuits. While they lack the stable performance achievable with synchronized or crystal-based designs, these economical oscillators feature circuit simplicity and are used extensively in baud-rate generators.

For maximum stability, an RC oscillator's output frequency must be insensitive to drift in as many circuit elements as possible. The clock circuit of **Fig 8** depends on the RC elements themselves for circuit stability. All other components contribute very low-order error terms—even for substantial shifts.

The circuit is a standard comparator-multivibrator with paralleled CMOS inverters interposed between the LM311 comparator output and the feedback resistors. This scheme replaces the relatively large and unstable bipolar V_{CE} saturation losses of the 311's output with the superior ON characteristics of MOS. In addition to being low and resistive, the MOS switching losses tend to cancel. Paralleling the inverters also reduces errors to insignificant levels.

With this arrangement, the capacitor's charge and discharge time constant is almost totally immune to temperature and supply-voltage shifts. The 10k resistors don't have to be precision types because their shifts will cancel. In addition, the symmetrical nature of the oscillator negates the effects of the comparator's dc input errors. The RC network is the only significant error source left.

The polystyrene capacitor's nominal −120 ppm/°C temperature coefficient (TC) is partially offset by the specified resistor's opposing positive TC. In practice you can only achieve a first-order compensation because no exact TC is available for the capacitor.

Over 0 to 70°C, this circuit shows a 15 ppm/°C TC and a power-supply rejection factor of less than 20 ppm/V. In contrast, a 555-based clock using the same compensating RC network shows 95 ppm/°C and 1050 ppm/V, respectively. At operating frequencies above 5 to 10 kHz, circuit stability degrades because of comparator propagation delays. **EDN**

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2. Burgoon, J R, and Wilson, R L, "SC-Cut Quartz Oscillator Offers Improved Performance," Hewlett-Packard Journal, March 1981.

Author's biography

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in related capacities at National Semiconductor Corp, Arthur D Little Inc and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art and collecting antique scientific instruments in his spare time.

Article Interest Quotient (Circle One)
***High* 476 *Medium* 477 *Low* 478**

Special circuit-design techniques enhance regulator performance

Because of their simplicity and ease of application, 3-terminal regulators are very popular. Nevertheless, some applications require special circuit-design techniques to enhance device performance.

Jim Williams, Linear Technology Corp

Three-terminal regulators provide an effective way of accommodating voltage control requirements. In most applications involving moderate output voltages and currents (5 to 50V at up to 5A), you can use them with no special design considerations. Nevertheless, what do you do if you need to control currents in the 8 to 12A range? What about regulating 100V outputs? This article will provide the answers to these questions. The discussion will highlight some circuit-design techniques that enhance the performance of off-the-shelf regulators without degrading their parameters or increasing operational stresses.

The circuit designs covered let you increase the current, voltage and power-output capabilities of 3-terminal regulators, allowing you to solve unique system design problems. A technique for improving a regulator's stability rounds out the discussion. Let's start by featuring some designs that let you reliably increase a regulator's output current.

Tolerances complicate matters

Extended output current probably ranks as the most common regulator modification. Conceptually, the simplest way to increase output current is to parallel two devices. In practice, though, regulator output-voltage tolerances can cause problems. There are ways to avoid these problems, however, and still get regulator output currents to add (**Fig 1**).

This circuit capitalizes on the 1% output tolerance of the specified regulators (LM-type devices, with a 4% tolerance, will not work in this circuit). A single resistive divider provides the sense voltage for both regulators, and the low-valued resistors provide ballast to account for the small difference in regulator output

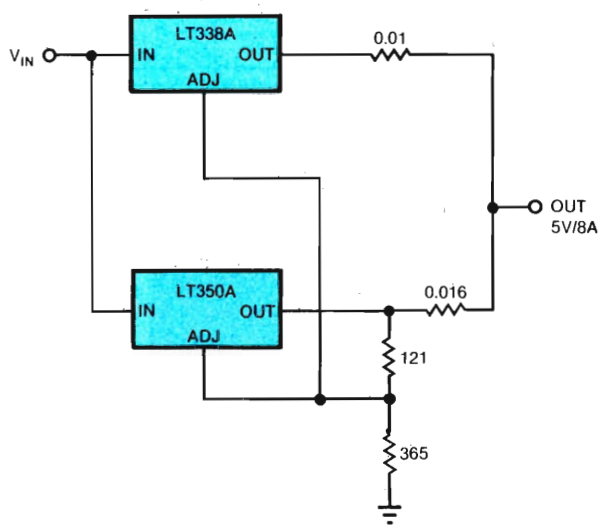


Fig 1—To realize trouble-free current summation, *this network uses a single sense-voltage source for both regulators and ballast resistors to offset the slight difference in regulator output voltages.*

voltages. Unfortunately, this added impedance degrades overall circuit load regulation by a factor of ten (to about 1%).

There are ways to extend output-current capability without degrading load regulation (**Fig 2a**). Although somewhat complex, this circuit avoids the ballast-resistor problems and features a fast-acting logic-controlled shutdown function as well as adjustable current limiting.

This network scheme extends the current capability of the LT1005 multifunction regulator by a factor of 12, while retaining its enable feature and auxiliary 5V output. The LT1005 servo controls booster transistor Q_1; Q_2 senses the voltage across the 0.05Ω current-limit resistor. When the shunt voltage is high enough, it turns on Q_2, which in turn biases Q_3 ON and shuts down the regulator by grounding its enable pin. The thermoswitch (mounted on Q_1's heat sink for optimum performance) disables the LT1005 to limit dissipation in Q_1 during prolonged short-circuit conditions.

Quite often, boosted regulators of this type have insufficient dynamic damping. This improper loop compensation leads to large output transients as the load shifts. This is particularly true when the load drops out—because of Q_1's voltage gain, output transients can approach the level of V_{IN}.

In **Fig 2a**, the 100-μF capacitor damps Q_1's overshoot tendency. The 250-μF capacitor maintains Q_1's emitter at dc, while the 20Ω resistor provides turn-off bias. Although this is obviously a brute-force technique, the compensation works well (**Fig 2b**).

Normally, the regulator sees no load. A high level on

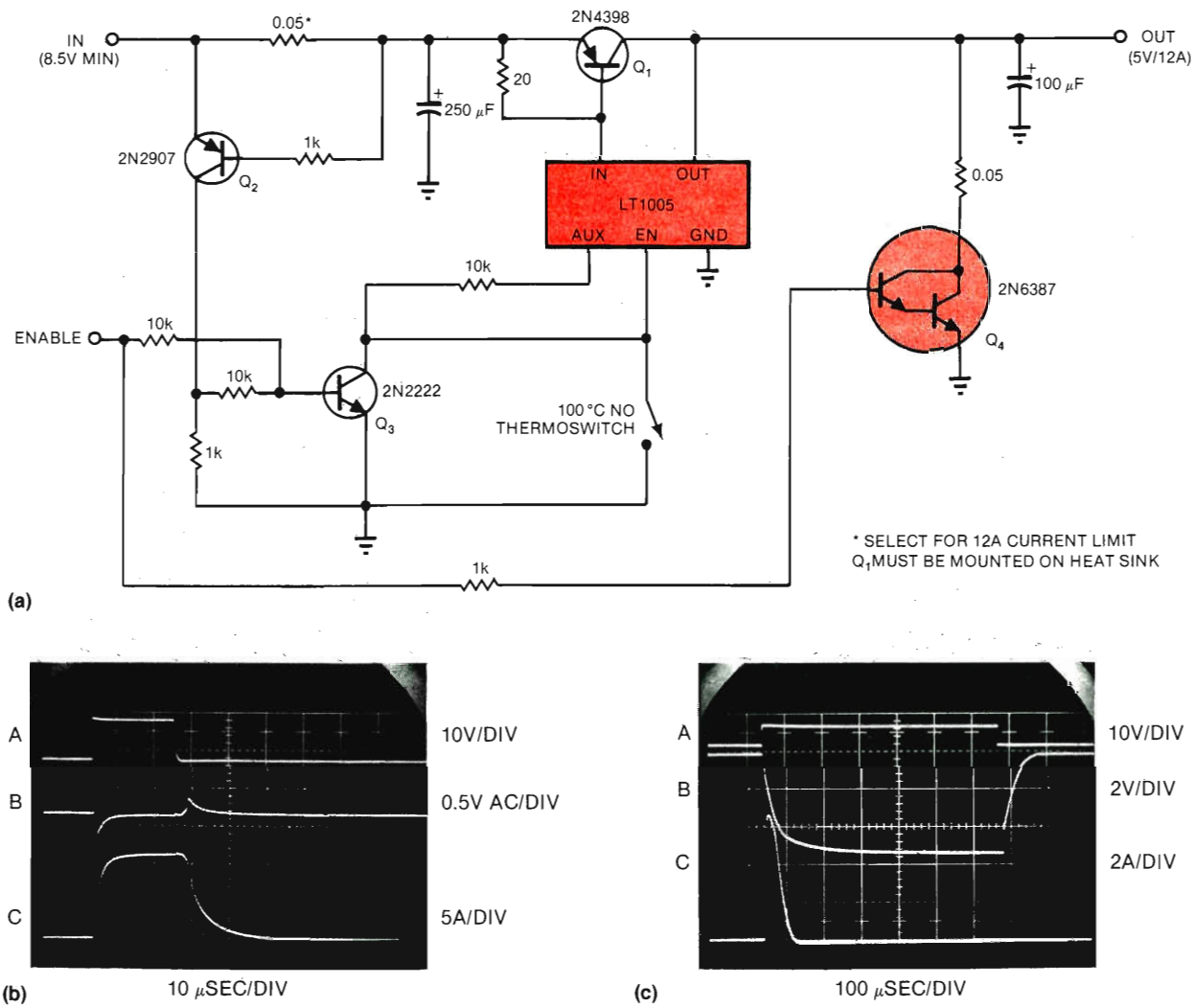


Fig 2—Offering a factor-of-12 improvement in output-current capability, *this network features adjustable current limiting* ***(a)****. While the compensation technique uses brute force, it works quite well* ***(b)****. Q_4 speeds up regulator response to an enable command as can be seen in* ***(c)****.*

trace A, however, indicates that a 12A load is suddenly present across the output terminals (trace C). The regulator output voltage (trace B) recovers quickly with minor aberration. While the output capacitor helps stabilize the network, it prevents the regulator's output from falling quickly when the enable command is activated. Since Q_1 cannot sink current, the capacitor's discharge time is load limited.

Q_4 corrects this problem even when there's no load. When the enable line goes high (**Fig 2c**, trace A), Q_3 comes on, cutting off the 1005 and forcing Q_1 off. Simultaneously, Q_4 comes on to rapidly pull down the regulator output (trace B) and sink the capacitor's discharge current (trace C). If fast turn-off is unnecessary, you can omit Q_4.

Modifying the output voltage

Another area for regulator-performance enhancement involves the control of high output voltages. Theoretically, high voltages present no problems for the regulator because it has no ground pin. Normally, the regulator floats at the supply's upper level—as long as you don't exceed the maximum V_{IN}-V_{OUT} differential, there are no problems. A short at the output, however, develops voltage levels that exceed this differential limit, thereby destroying the regulator.

Fig 3 illustrates a complete high-voltage regulator circuit that accommodates 100V at 100 mA and withstands shorts to ground. Even at 100V output levels, the LT317AT functions in its normal mode, maintaining 1.2V between the output and adjustment pins. Under these conditions, the 30V zener is off and Q_1 conducts. Should a short occur at the output, the zener conducts, forcing Q_1's base to 30V and clamping its emitter at V_Z-2V_{BE} to maintain the regulator well within its V_{IN}-V_{OUT} rating.

Since Q_1 is a high-power device (12W rating), it will sustain a 90V V_{CE} at whatever current the transformer and regulator will supply. The transformer saturates at 130 mA so Q_1 stays within its safe operating area. With Q_1 and the LT317AT thermally coupled, the regulator soon goes into thermal shutdown and oscillations commence.

This action continues as long as the output remains shorted, protecting the regulator and the load. The 500-pF capacitor combines with the 10Ω/0.02-μF damper network to augment transient response, while the diodes provide safe discharge paths for the capacitors.

Handling high power outputs

Power-dissipation control is another area where added circuitry can augment regulator performance. You can, of course, simply increase the size of the heat sink to offset dissipation problems, but this is an inefficient approach. A better solution involves placing the regulator within a switched-mode loop that servo controls the voltage across the regulator. This allows the regulator to function normally, while the switched-

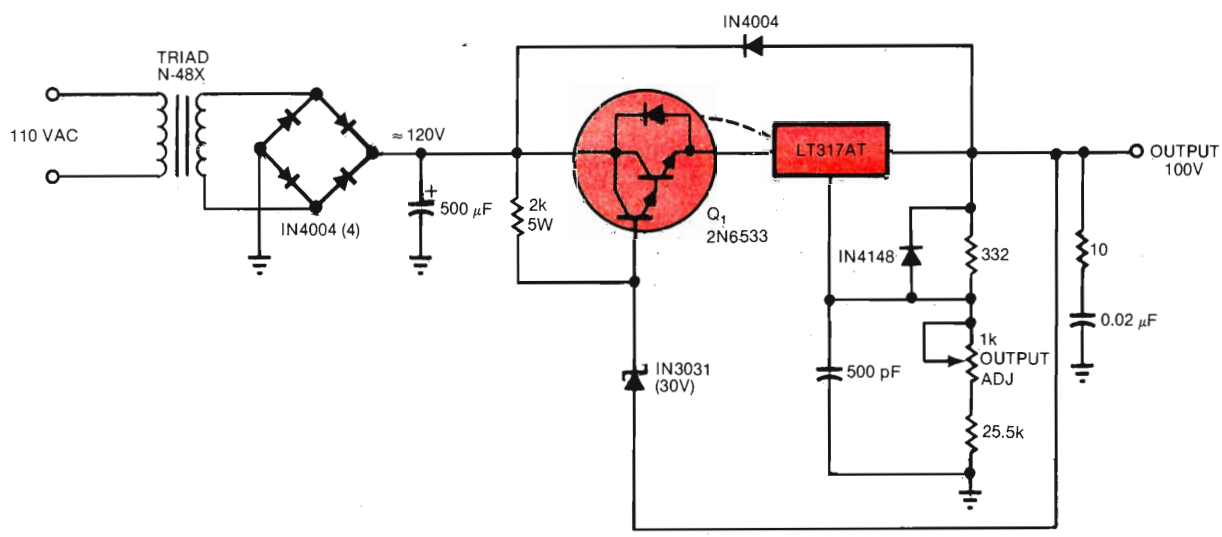


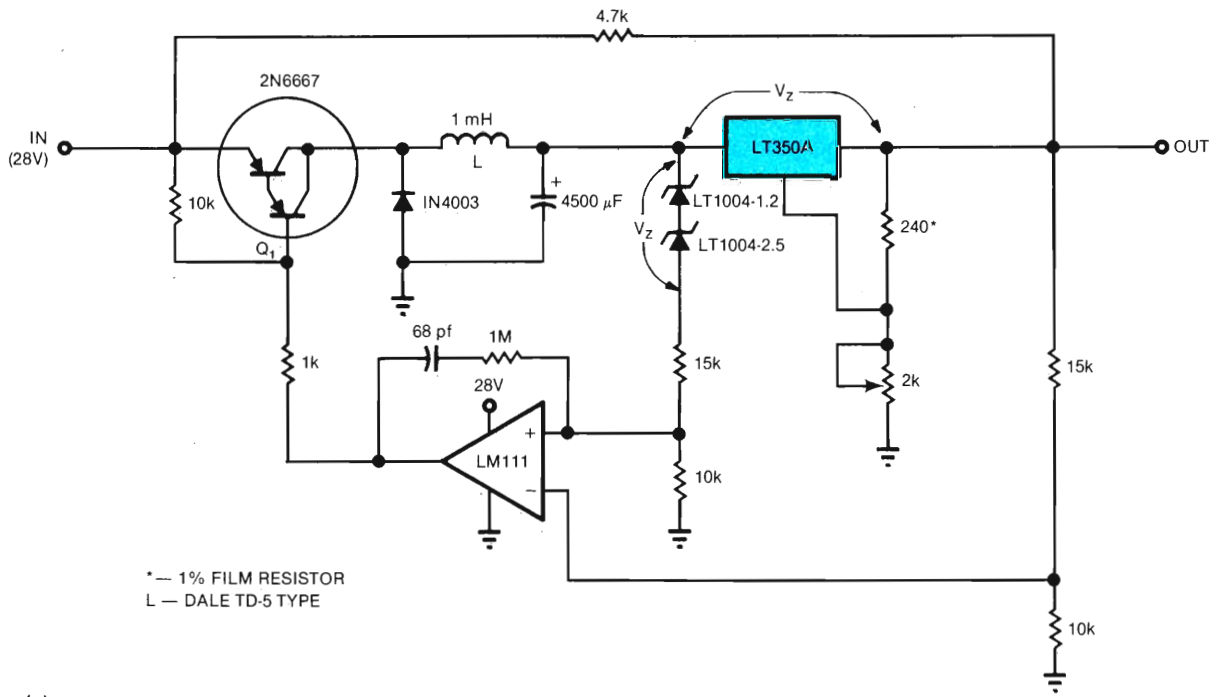
Fig 3—Featuring immunity to output short circuits, *this regulator circuit accommodates 100V at 100 mA. Even at 100V output levels, the LT317AT functions in its normal mode, maintaining 1.2V between the output and adjustment pins.*

Improper loop compensation creates large output transients

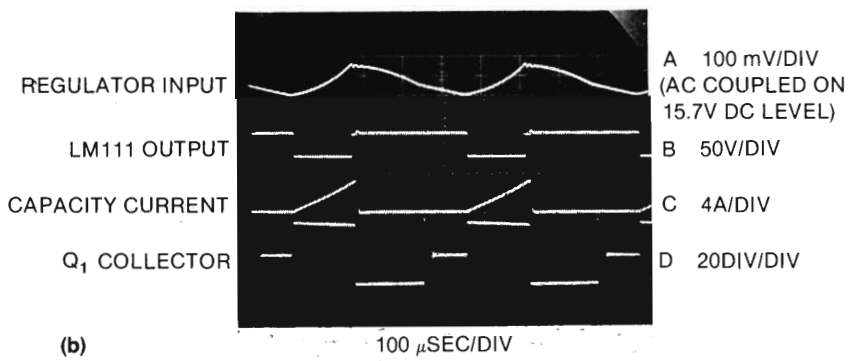
mode control minimizes its input/output voltage differential—regardless of line or load changes. Although it is not quite as efficient as the classical switching regulator, this approach offers lower noise performance and the fast transient response available with linear regulators.

Fig 4a details a dc-driven version of the scheme. The LT350A functions in a conventional manner, supplying its rated 3A regulated output. The remaining components form the switched-mode dissipation limit control. This control loop forces the potential across the LT350A to equal V_Z. When the regulator input **(Fig 4b)** decays far enough, the LM111 output goes low and turns on Q_1, allowing input-current flow to charge the 4500-μF capacitor and raise the regulator's input voltage. When the regulator input rises high enough, the comparator output goes high, cutting off Q_1 and stopping the capacitor's charge cycle.

The 1N4003 damps the current-limiting inductor's flyback spike. The LM111's feedback network sets loop hysteresis at about 80 mV p-p; the 4.7k resistor ensures circuit startup. This free-running oscillation-control scheme substantially reduces regulator dissipation without degrading its performance. Even with load



(a)



(b)

Fig 4—To offset dissipation problems, *you can place the regulator within the switched-mode loop* ***(a)*** *that servo controls the voltage across the regulator. When the regulator input decays far enough* ***(b)****, the 4500-μF capacitor charges to raise the regulator's input voltage.*

shifts or changes in input or output conditions, the loop always minimizes regulator dissipation.

This dissipation-limiting technique will also accommodate more sophisticated circuits (**Fig 5a**). This ac-powered network provides a 0 to 35V, at 3A, regulated output under high-line/low-line conditions. Two SCRs

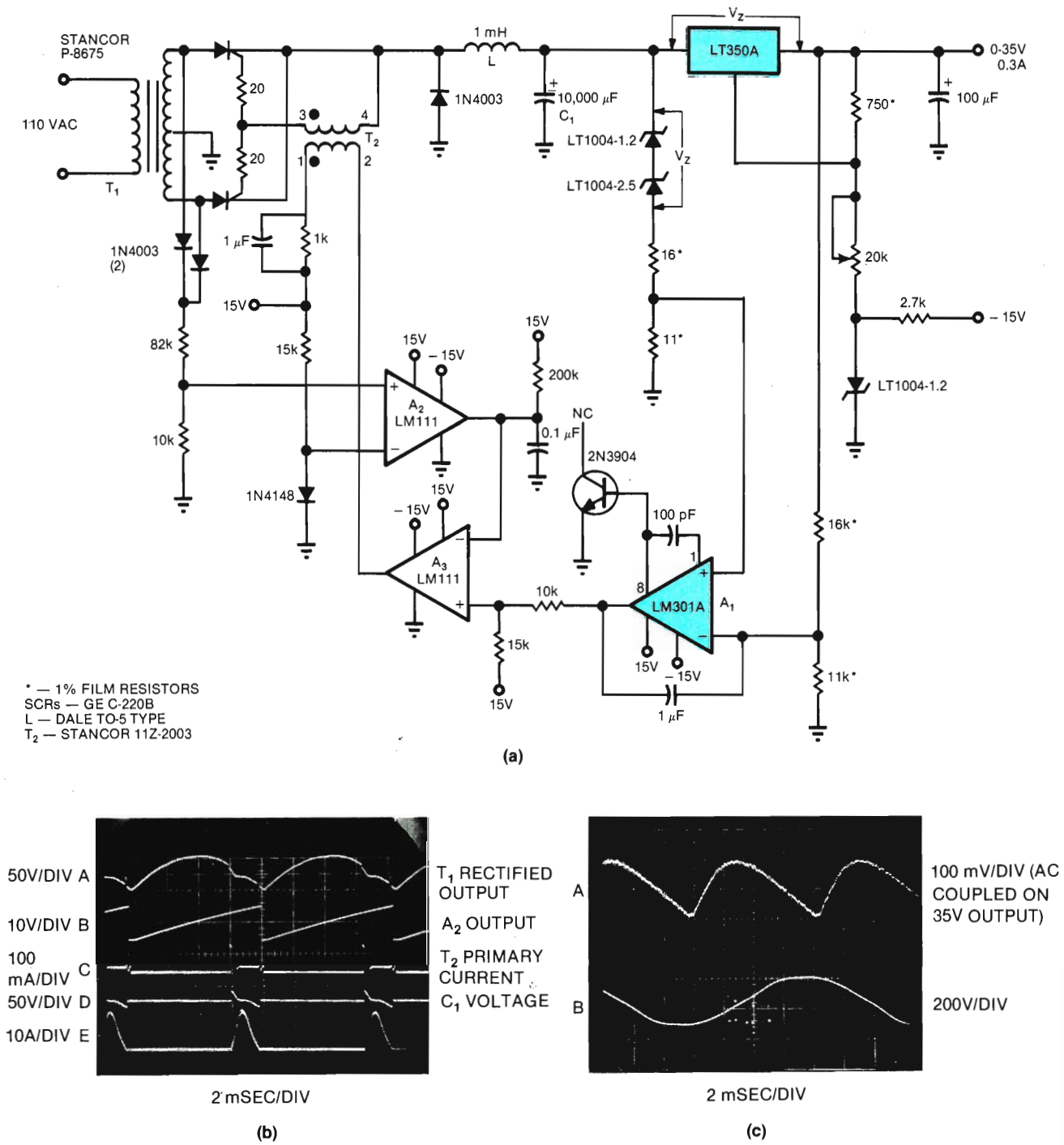


Fig 5—You can also use dissipation-limiting techniques *to develop a circuit that provides a 35V/3A regulated output under high-/low-line conditions* ***(a)****. The capacitive feedback around* A_1 *stabilizes the circuit without compromising the 350A's transient response* ***(c)****.*

Switched-mode control scheme minimizes voltage differentials

and a center-tapped transformer provide power to the LC network. T_1's output is also diode rectified (**Fig 5b**), divided and used to reset the 0.1-μF capacitor at comparator A_2's output.

A_3 compares the line-synchronous ramp at A_2's output to the LM301A's offset to develop an output at A_1; this represents the deviation from the zener-voltage level that the loop is trying to establish across the LT350A. When the ramp output exceeds the voltage level at A_3's noninverting input, the comparator output goes low, dumping current through T_2's primary. This fires the appropriate SCR and establishes a path for current to charge the 10,000-μF capacitor. When the ac line drops low enough, the SCR commutates and charging ceases.

On the following half cycle, the alternate SCR fires to repeat the process. In this fashion, the loop controls the SCR's firing phase angle to maintain the voltage across the LT350A at 3.7V (V_Z). The 1.2V LT1004 at the 350A output permits you to set circuit output voltage down to zero; the 2N3904 clamp at A_1 prevents loop hangup.

Although A_1 supplies an analog voltage, the ac-driven nature of the circuit forces it to approximate a smoothed, sampled-loop response. Conversely, the regulator constitutes a true linear system. Because these two feedback systems are interdependent, compensation can be difficult. The capacitive feedback around A_1 keeps the loop gain's frequency cutoff low enough to stabilize the circuit without compromising the 350A's transient-response characteristic (**Fig 5c**).

Trace A shows the output noise—made up of residual 120-Hz ripple plus regulator noise—with the circuit

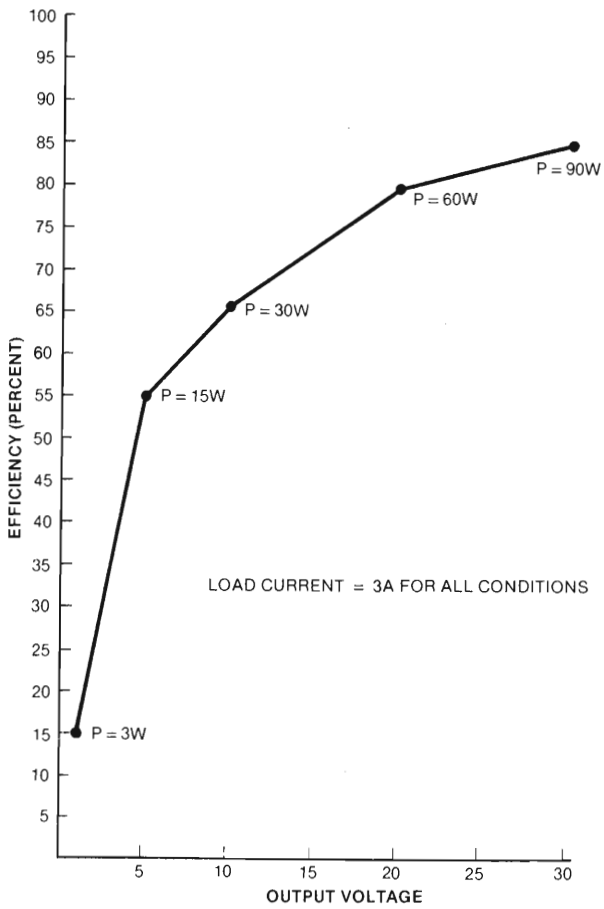


Fig 6—Good efficiency is a key feature *of the compensation scheme employed in* ***Fig 5****. Static losses across the regulator and SCRs combine to reduce efficiency at low output voltages, but efficiency improves at higher outputs.*

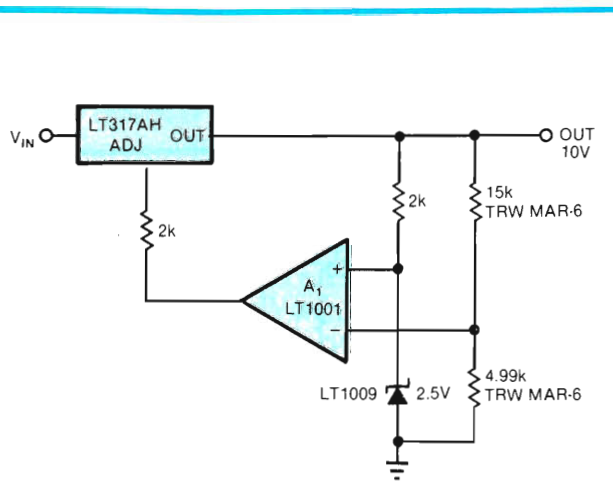


Fig 7—To improve regulator stability over time and temperature, *A_1 forces the adjustment pin to maintain the regulator output at 10V.*

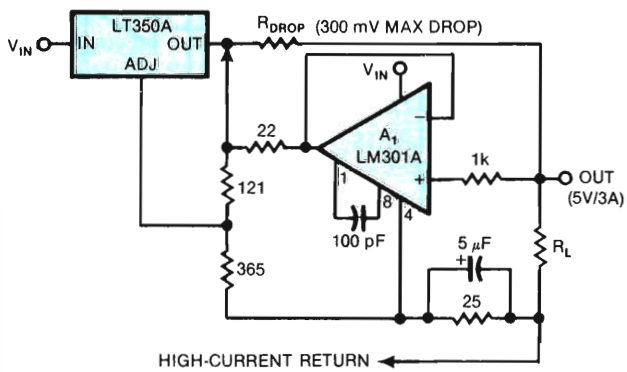


Fig 8—To eliminate troublesome voltage drops *in supply lines, this regulator network remotely senses the feedback voltage right at the load.*

Trace A shows the output noise—made up of residual 120-Hz ripple plus regulator noise—with the circuit

handling a 105W load (35V/3A). Note the absence of fast-switching transients and harmonics. Noise reflected into the ac power line (trace B) is also negligible because the inductor limits current rise time to about 1 msec—much slower than normal switching supplies.

This circuit will function over all line, load and output-voltage conditions with good efficiency (**Fig 6**). Efficiency suffers at low output voltages—where the static losses across the regulator and SCRs are significant—but the method attains 85% efficiency at the higher output levels.

Output stability can also be improved

Power is not the only area where you can augment regulator performance. **Fig 7** illustrates a method of improving a regulator's output stability over time and temperature—a capability that's most useful when you're powering a transducer-based strain gauge. As shown, precision amplifier A_1 compares a portion of the regulator's output voltage to the 2.5V reference. A_1's output forces the LT317A's adjustment-pin voltage to whatever level is necessary to maintain the output at 10V.

A_1 contributes negligible error. The specified resistors track within 5 ppm/°C, and the reference contributes about 20 ppm/°C. This scheme in no way compromises the regulator's short-circuit or thermal-overload-protection specifications.

The circuitry in **Fig 8** allows a regulator to remotely sense the feedback voltage, thereby eliminating voltage-drop effects in the supply lines. Such drops are of major concern in applications involving the transmission of high currents over relatively long supply rails or pc-board traces.

Functionally, the circuit uses A_1 to sense the voltage directly at the load. The output of A_1 and the regulator's output add together—this sum in turn modifies the adjustment-pin voltage to compensate for the voltage lost across R_{DROP}. The feedback divider returns from the load through a separate lead to complete the

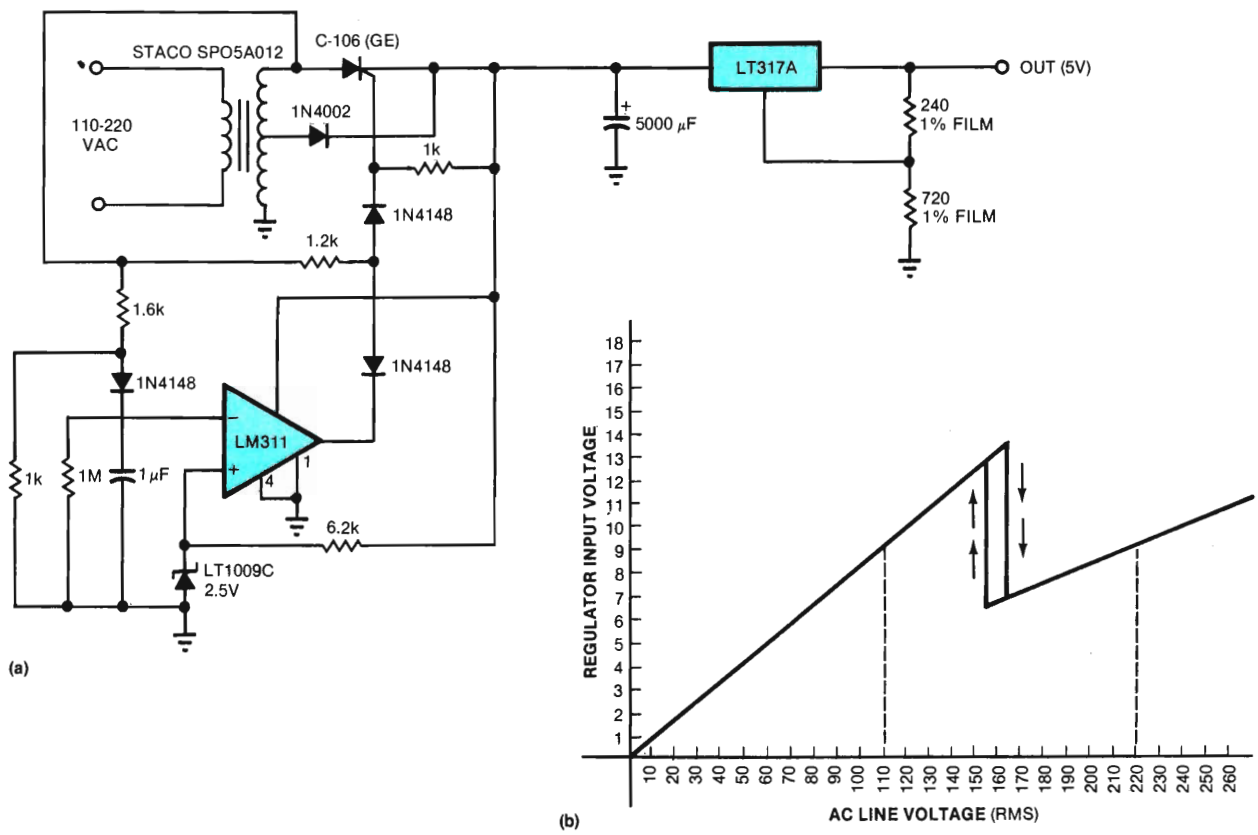


Fig 9—To accommodate multiple inputs, *this network* ***(a)*** *automatically cuts regulator drive in half for 220V inputs to maintain a safe dissipation level. The switch to center-tapped drive occurs midway between 110 and 220V* ***(b).***

Center-tap drive network handles multiple input signals

remote-sensing scheme. The 5-μF capacitor serves as a noise filter; the 1-kΩ resistor limits bypass-capacitor discharge when you turn off the power.

A final circuit (**Fig 9a**) lets you run regulator-powered circuitry from 110 or 220V ac without having to switch transformer windings. Best of all, regulator dissipation does not increase operating from 220V ac.

When the transformer is driven from 110V ac, the LM311 output goes high, allowing the 1.2-kΩ resistor to supply gate bias for the SCR (the 1N4002 is off). The SCR rectifies the transformer output and the regulator sees about 8.5V at its input. A 220V ac source at the transformer input drives the LM311's inverting input beyond 2.5V and clamps its output low. This steers the SCR's gate bias to ground through the 311's output transistor (the 1N4148 diodes in the LM311's output line prevent reverse voltages from reaching the SCR or the 311 output). With the SCR now off, the 1N4002 delivers current to the regulator from the transformer's center tap.

Although the transformer input voltage has doubled, output potential is halved and the regulator's power dissipation stays the same. The line-input versus regulator-input voltage transfer function (**Fig 9b**) illustrates circuit performance. The switch to center-tap drive occurs midway between 110 and 220V ac. The desirable hysteresis is a function of the transformer's output-voltage shifts caused by the step change in loading. **EDN**

Author's biography

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in related capacities at National Semiconductor Corp, Arthur D Little Inc and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art and collecting antique scientific instruments in his spare time.

Article Interest Quotient (Circle One)
High **482** ***Medium*** **483** ***Low*** **484**

Take advantage of thermal effects to solve circuit-design problems

You probably consider thermal effects in circuits your enemy, but they can prove useful in many design situations.

Jim Williams, *Linear Technology Corp*

The direct relationship between temperature and electronic-device failure is the source of more design headaches than any other single consideration. But instead of trying to eliminate or compensate for thermal parasitics in circuits, you can use them to achieve novel solutions to measurement and control problems.

A look at a temperature-control loop illustrates the techniques involved, and familiarity with some of these techniques can help you apply them in less obvious but equally useful ways.

Fig 1 shows a precision temperature controller for a small components' oven. When power is applied to the circuit, the thermistor—a negative-temperature-coefficient device—exhibits a resistance that's high enough to saturate amplifier A_1's output positive. This forces the LT3525 switching regulator's output (pin 13)

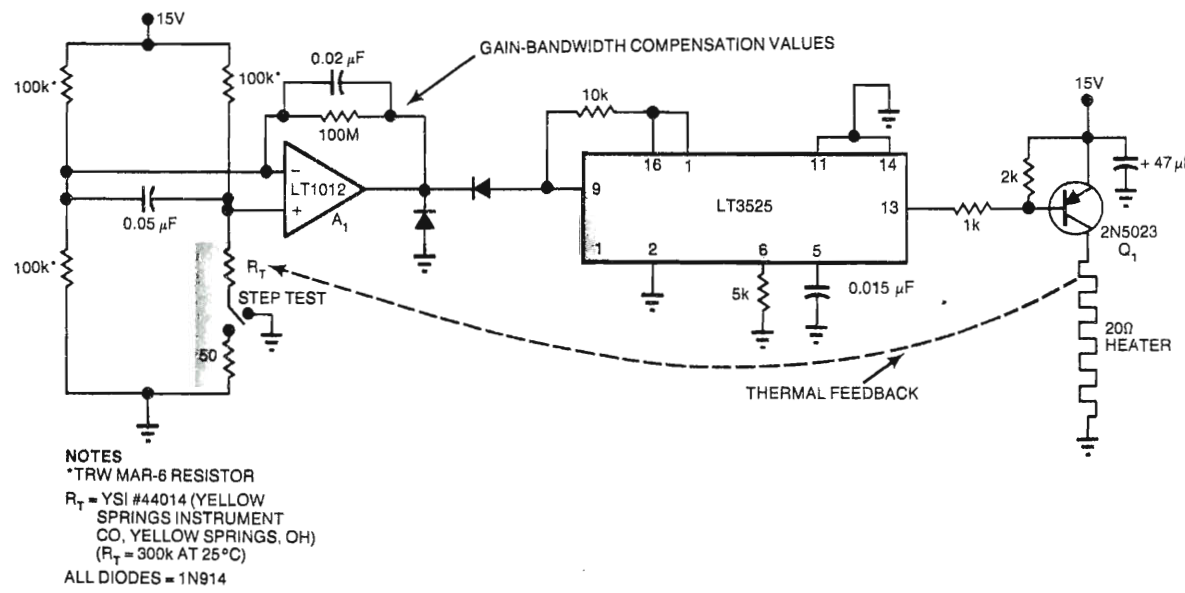


Fig 1—A precision temperature controller for a small oven *makes use of a thermistor's negative temperature coefficient. The 50Ω resistor and switch in series with the thermistor can generate a step input for testing the circuit's response.*

RC networks model a thermal control loop

Low, biasing Q_1 On. As the 20Ω heater warms, the thermistor's resistance decreases, reducing the voltage at A_1's positive input. When that voltage decreases to the inverting input's level, A_1 comes out of saturation, and the LT3525 pulse-width modulates the heater via Q_1, completing a feedback path. Because the heater voltage's modulation rate is much higher than the thermal loop's response, the oven maintains an even, continuous heat flow.

To achieve such high-performance control, you must match A_1's gain-bandwidth product (GBW) to the requirements of thermal-feedback path. Theoretically, achieving this match should be a simple matter using conventional servo-feedback techniques. But practically, the long time constants and thermal delays inherent in thermal systems present a challenge, and thermal-control systems often demonstrate the unfortunate relationship between servo systems and oscillators.

Modeling the thermal loop

A thermal-control loop can be simplistically modeled as a network of resistors representing thermal resistance and capacitors representing thermal capacitance. **Fig 2** models a heater, sensor and heater/sensor interface, each of which has an RC factor that contributes to the lumped delay in a thermal system's ability to respond. To prevent oscillation, A_1's GBW must be limited to account for this delay, although high control performance dictates that A_1's GBW be large. Thus, the delays must be minimized.

The delay associated with the heater itself depends to some extent on the size of the heater, and placing the

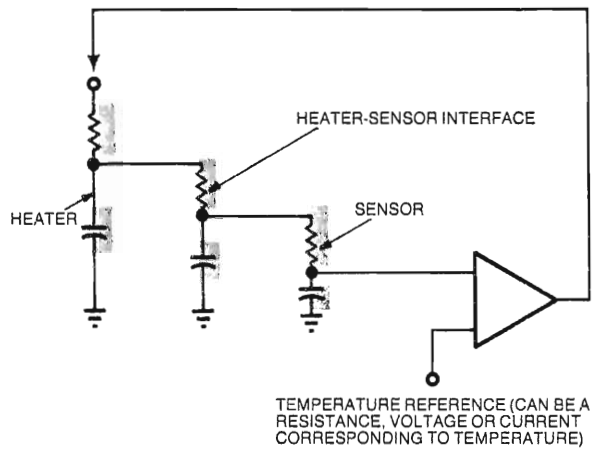


Fig 2—Resistor-capacitor networks can model a heater *and a sensor as well as the heater/sensor interface.*

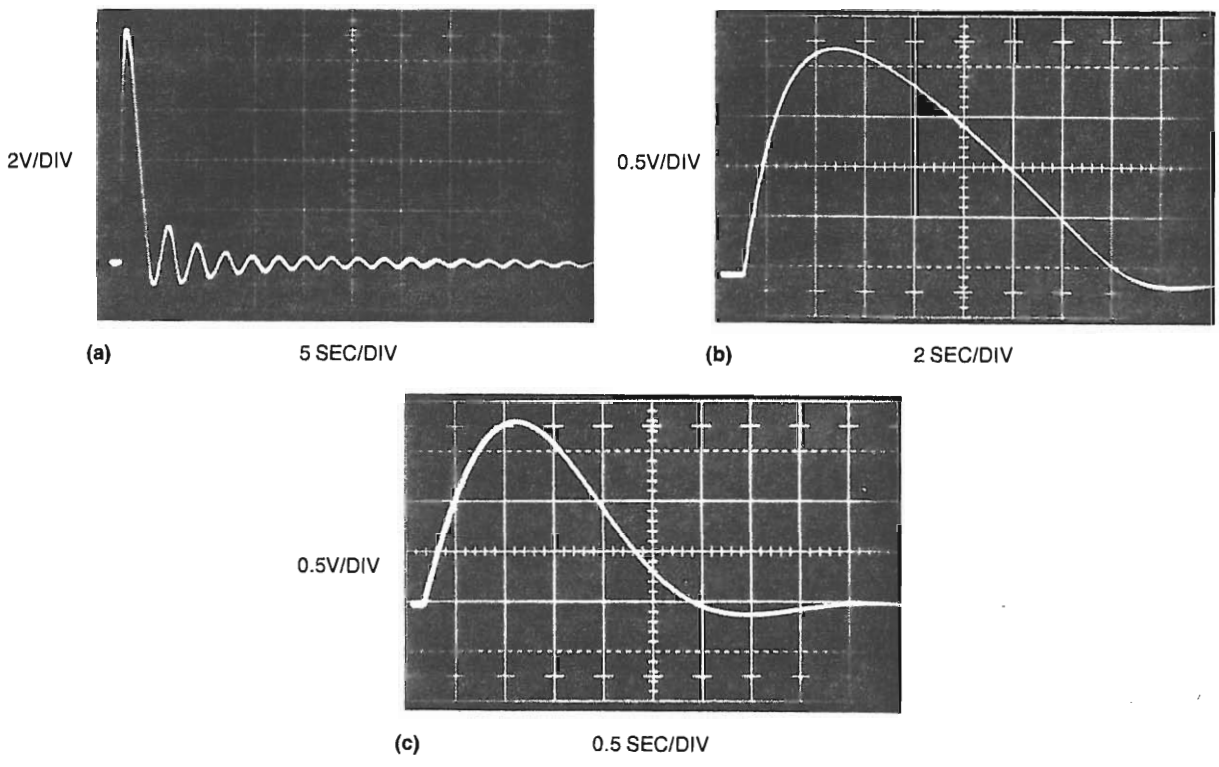


Fig 3—A step input to Fig 1's *circuit can result in underdamped* ***(a)****, overdamped* ***(b)*** *or critically damped* ***(c)*** *responses. The critically damped performance results from the component values shown in* ***Fig 1.***

sensor in intimate contact with the heater reduces the heater-sensor-interface time constant. To minimize the sensor's RC product, you should select a sensor whose size is relatively small compared to the capacity of its thermal environment. Clearly, for an oven with 6-in.-thick aluminum walls, you don't have to use the smallest sensor available. Conversely, for controlling the temperature of a 1/16-in.-thick glass microscope slide, a very small (ie, fast) sensor is in order.

After minimizing thermal time constants, your next step is to choose insulation, which keeps the heat-loss rate down so that the temperature-control system can keep up with the losses. For any given system, increasing the ratio between heater and sensor time constants and the insulation time constants betters performance.

Optimizing the loop

After attending to these thermal considerations, you can optimize the loop's GBW. **Fig 3** shows the effects of different compensation values at A_1. To fine tune the compensation, you can alter the temperature set-point in small steps and observe the loop response at A_1's output. In **Fig 1**, the 50Ω resistor and switch in the bridge's thermistor leg simulate a 0.01°C step.

Fig 3a shows the effects of too much gain bandwidth —the step input forces a damped ringing response that remains at a significant level for more than 50 sec. The ringing eventually dies out making the loop conditionally stable. A further increase in A_1's GBW would result in continuous oscillation. **Fig 3b** illustrates the effect of reducing GBW. Settling time is much faster and more controlled. The waveform is overdamped, indicating that a higher GBW can be achieved without compromising stability.

Fig 3c shows the response for the component values shown in **Fig 1**, and it illustrates a nearly ideal critically damped recovery. Settling occurs within 4 sec. An oven so optimized can easily attenuate external temperature

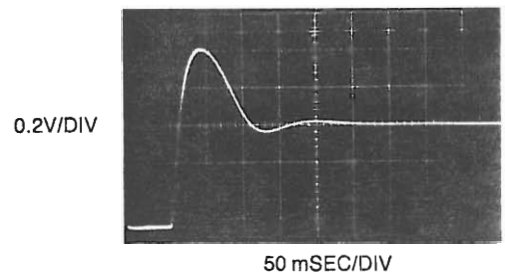


Fig 5—The small die size *of* ***Fig 4****'s transistor array allows a quick, clean response. Settling time in response to a full-scale step input is 250 msec.*

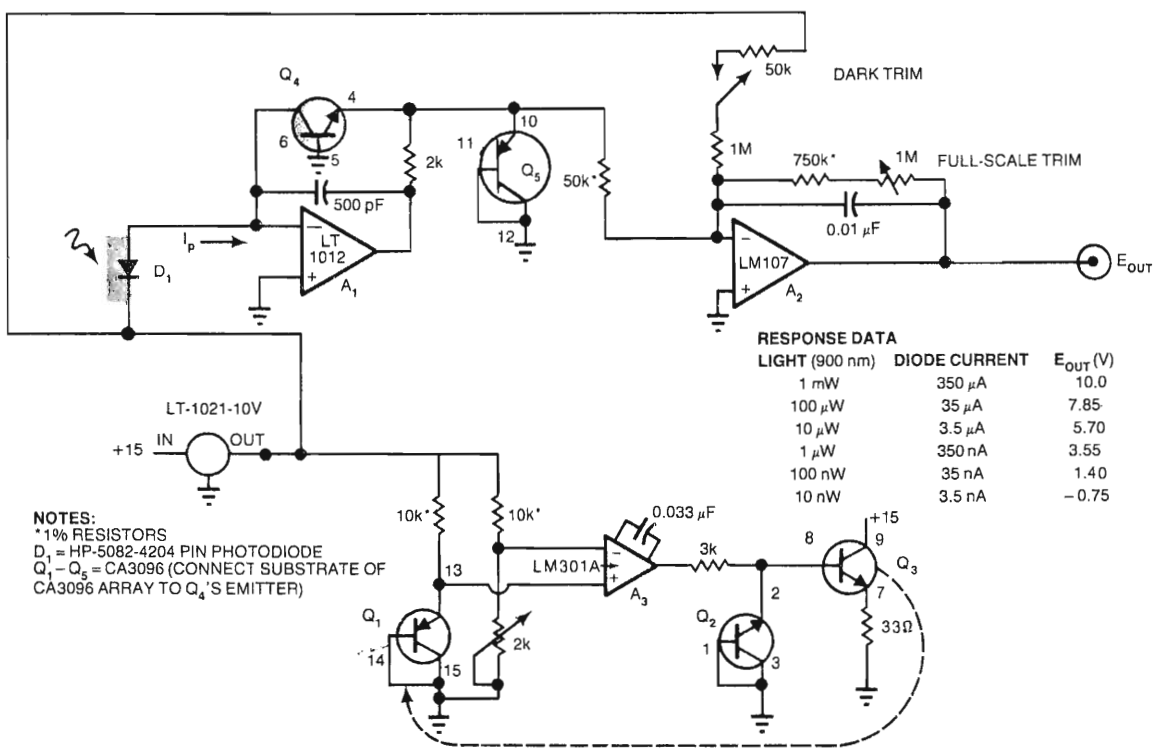


Fig 4—Logarithmic signal conditioning *allows this circuit based on a PIN photodiode to measure light levels over a 100-dB range. The circuit precisely controls the temperature of* Q_4*, the logging transistor.*

shifts by a factor of thousands without overshoots or excessive lag.

With this background in the basics of thermal-loop operation, consider some practical applications for temperature control. PIN photodiodes, for example, often serve in photometric circuits. The photodiode in **Fig 4**, for instance, responds linearly to light intensity over a 100-dB range, and digitizing this diode's linearly amplified output would require an A/D converter with 17-bit resolution. Using signal-conditioning circuitry to logarithmically compress the diode's output eliminates this resolution requirement, but it involves using logarithmic amplifiers, which depend on a transistor's V_{BE} vs collector-current relationship.

This characteristic is highly temperature sensitive and often requires special components and layout considerations to achieve good results. Using temperature-control techniques, however, **Fig 4**'s circuit logarithmically signal conditions the photodiode's output and requires no special components or layout.

In **Fig 4**, A_1 and Q_4 convert the diode's photocurrent to a voltage output with a logarithmic transfer function. A_2 provides offset and additional gain. A_3 and its associated components form a temperature-control loop that maintains Q_4 at a constant temperature. (All transistors in this circuit are part of a CA3096 monolithic array.) The 0.033-μF at A_3's compensation pins gives good loop damping if the circuit is built using the array transistors as shown—this configuration achieves optimal temperature control at Q_4, the logging transistor. Because of the array die's small size, response is quick

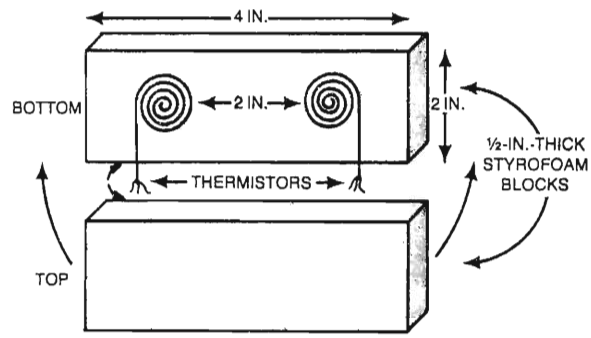
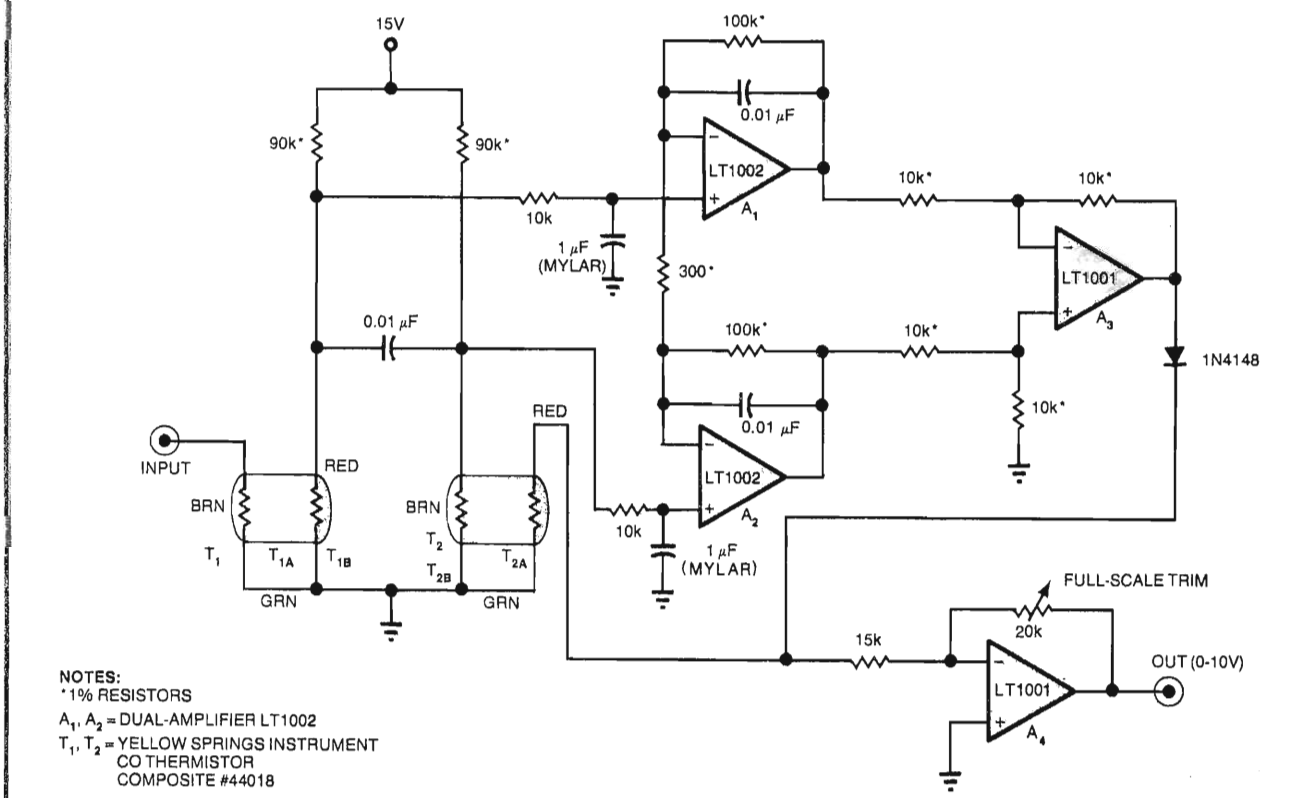


Fig 7—Sandwiching two thermistors *between Styrofoam blocks provides them with an isothermal environment. Coiling the thermistor leads attenuates heat-pipe effects to the outside ambient temperature.*



NOTES:
*1% RESISTORS
A_1, A_2 = DUAL-AMPLIFIER LT1002
T_1, T_2 = YELLOW SPRINGS INSTRUMENT CO THERMISTOR COMPOSITE #44018

Fig 6—Achieving a 50-MHz bandwidth and 2% accuracy, *this circuit measures the dc heating power of an input waveform. Crest factors as high as 100:1 contribute less than 0.1% additional error.*

and clean. Settling time in response to a full-scale step (**Fig 5**) is only 250 msec.

To use this circuit, first set the thermal-control loop by grounding Q_3's base and adjusting the 2-kΩ pot so that A_3's − input voltage is 55 mV higher than its + input voltage. That adjustment places the servo's set point at about 50°C, corresponding to a 25°C rise (2.2 mV/°C×25°C=55 mV) above a 25°C ambient temperature. To complete this first step, remove the ground from Q_3's base and the array will come to temperature.

Next, place the photodiode in a completely dark environment and adjust the 50-kΩ dark-trim pot so that A_2's output is 0V. Finally, either apply or electrically simulate (according to **Fig 4**'s response-data chart) a light level corresponding to 1 mW and adjust the 1-MΩ full-scale-trim pot for a 10V A_2 output. Once adjusted, the circuit responds logarithmically to light inputs from 10 nW to 1 mW with accuracy limited by the diode's 1% error.

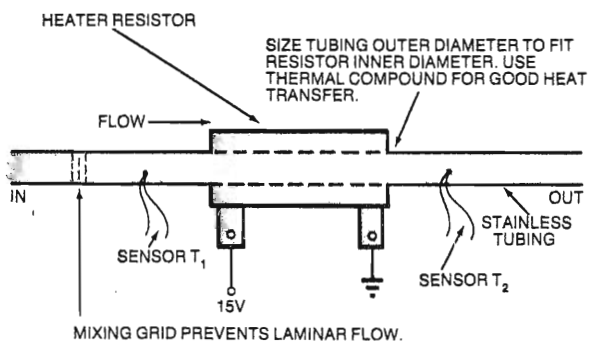


Fig 9—To measure a fluid's flow rate, *Fig 8's circuit depends on a heater to induce a temperature change in the fluid. Sensors on either side of the heater measure the induced change.*

Thermal rms/dc converter

A thermal rms/dc converter demonstrates another application for temperature control. Conversion of ac waveforms to their equivalent dc-power value is usually accomplished by rectifying and averaging or by analog computing methods. Rectification and averaging, however, work only for sinusoidal inputs. Moreover, analog computing methods generally aren't suitable at frequencies above 500 kHz, and crest factors greater than 10 can cause significant reading errors.

Overcoming these drawbacks, **Fig 6**'s circuit

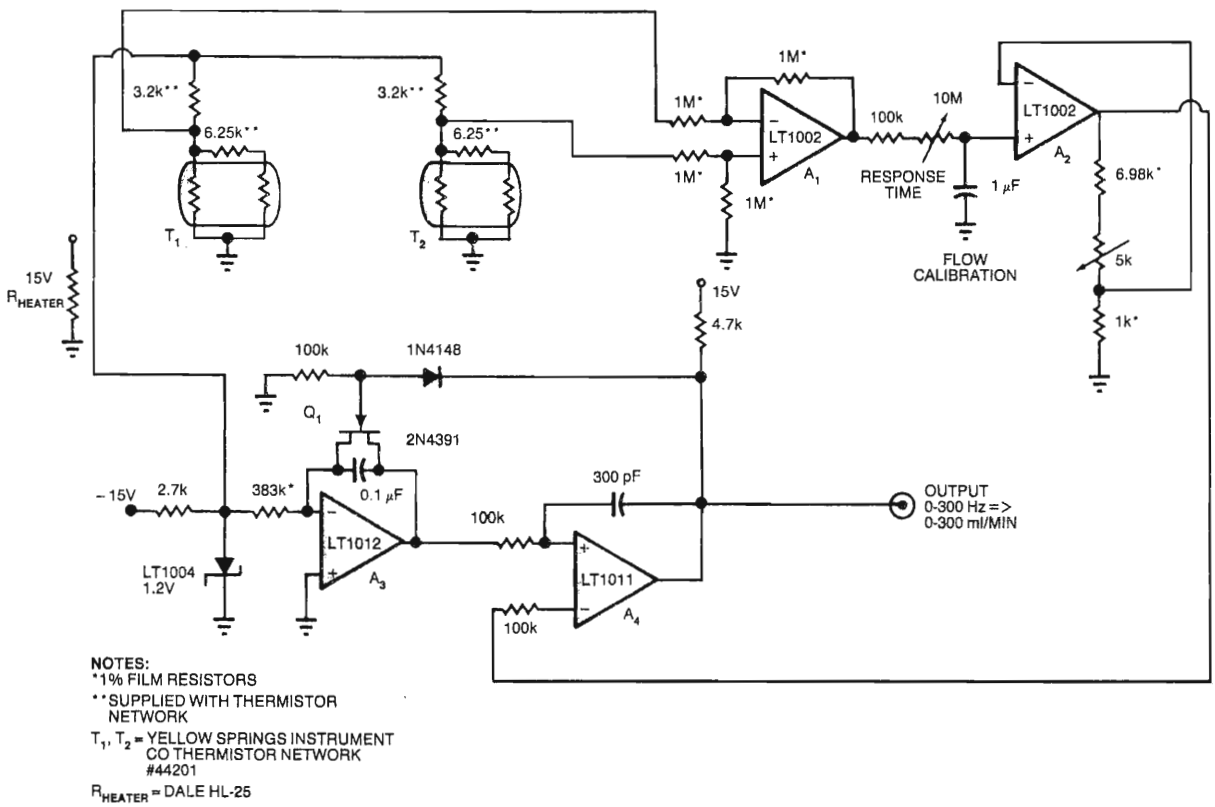


Fig 8—Overcoming the drawbacks of mechanical transducers, *this thermally based flow-meter circuit generates an output whose frequency is proportional to flow rates as low as 1 ml/min.*

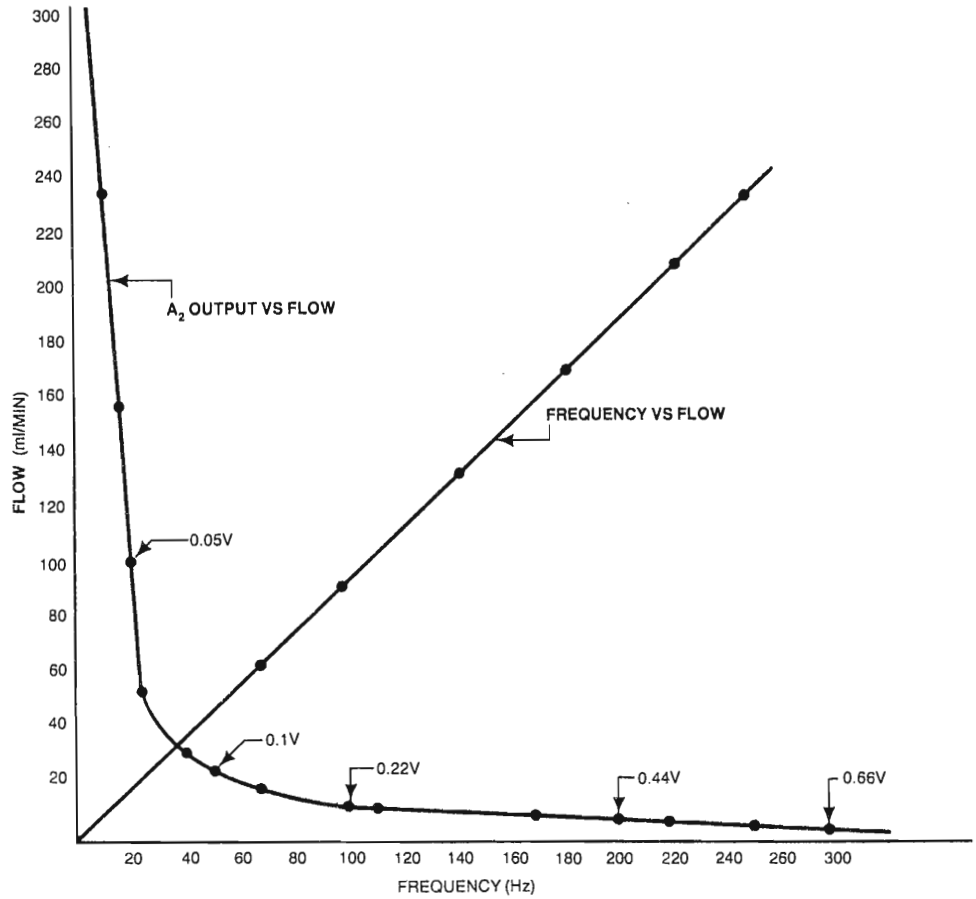


Fig 10—The temperature difference *detected by* ***Fig 8****'s sensors is inversely proportional to flow rate. Amplifiers* A_3 *and* A_4 *in* ***Fig 8*** *linearize this relationship.*

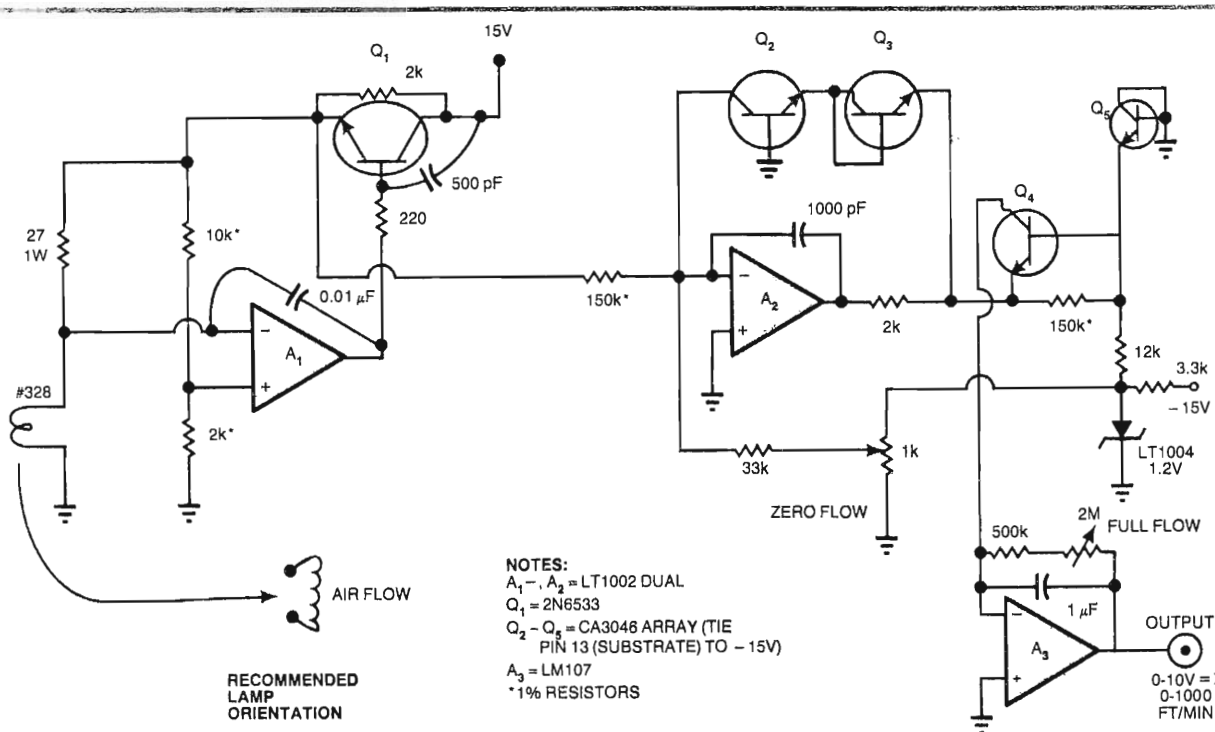


Fig 11—A lamp with its glass envelope removed *serves as the basis for a thermally based anemometer. The lamp's filament should be oriented 90° to the airflow direction.*

Thermal rms/dc converter tolerates 100:1 crest factors

achieves wide bandwidth and high crest-factor performance by directly measuring the dc heating power of the input waveform. Using thermal techniques to integrate the input waveform, it achieves a 50-MHz bandwidth with 2% accuracy. And because the thermal integrator's output is a low-frequency signal, the circuit uses standard components and requires no special trimming techniques.

The circuit works by measuring the amount of heat required to maintain two similar but thermally decoupled masses at the same temperature. The input signal is applied to T_1, a dual-thermistor bead. The power dissipated in one leg of this bead (T_{1A}) forces the other leg (T_{1B}) to shift down in value, unbalancing the bridge completed by the other bead and the 90-kΩ resistors. The A_1-A_2-A_3 combination amplifies this imbalance, and A_3's output, applied to T_{2A}, heats T_{2A} causing T_{2B} to decay in value. As T_{2B}'s resistance drops, the bridge balances, and A_3's output adjusts the drive to T_{2A} to maintain T_{1B} and T_{2B} at equal values.

Under this condition, the T_{2A} voltage should equal the rms value of the circuit's input, although in fact slight mass imbalances between T_1 and T_2 contribute a gain error, which A_4 corrects. RC filters at A_1 and A_2 and the 0.01-μF capacitor eliminate possible high-frequency error due to capacitive coupling between T_{1A} and T_{1B}. The diode in A_3's output line prevents latchup.

Fig 7 details the thermistor's recommended thermal arrangement. The Styrofoam blocks provide an isothermal environment, and coiling the thermistor leads attenuates heat-pipe effects to the outside ambient temperature. The 2-in. distance between the devices allows them to see identical thermal conditions without interacting.

To calibrate this circuit, apply 10V dc to the input and adjust the full-scale-trim pot for a 10V output at A_4. Accuracy remains within 2% from dc to 50 MHz for inputs from 300 mV to 10V. Crest factors as high as 100:1 contribute less than 0.1% additional error, and response time to within rated accuracy equals 5 sec.

Low flow-rate thermal flow meter

Another application for thermal-control techniques involves measuring low fluid flow rates, a task often fraught with difficulty. Paddlewheel and hinged-vane-type transducers, for example, have low, inaccurate outputs at low flow rates, and such transduction techniques become mechanically impractical for small-diameter tubing, such as that used in medical or biochemical work.

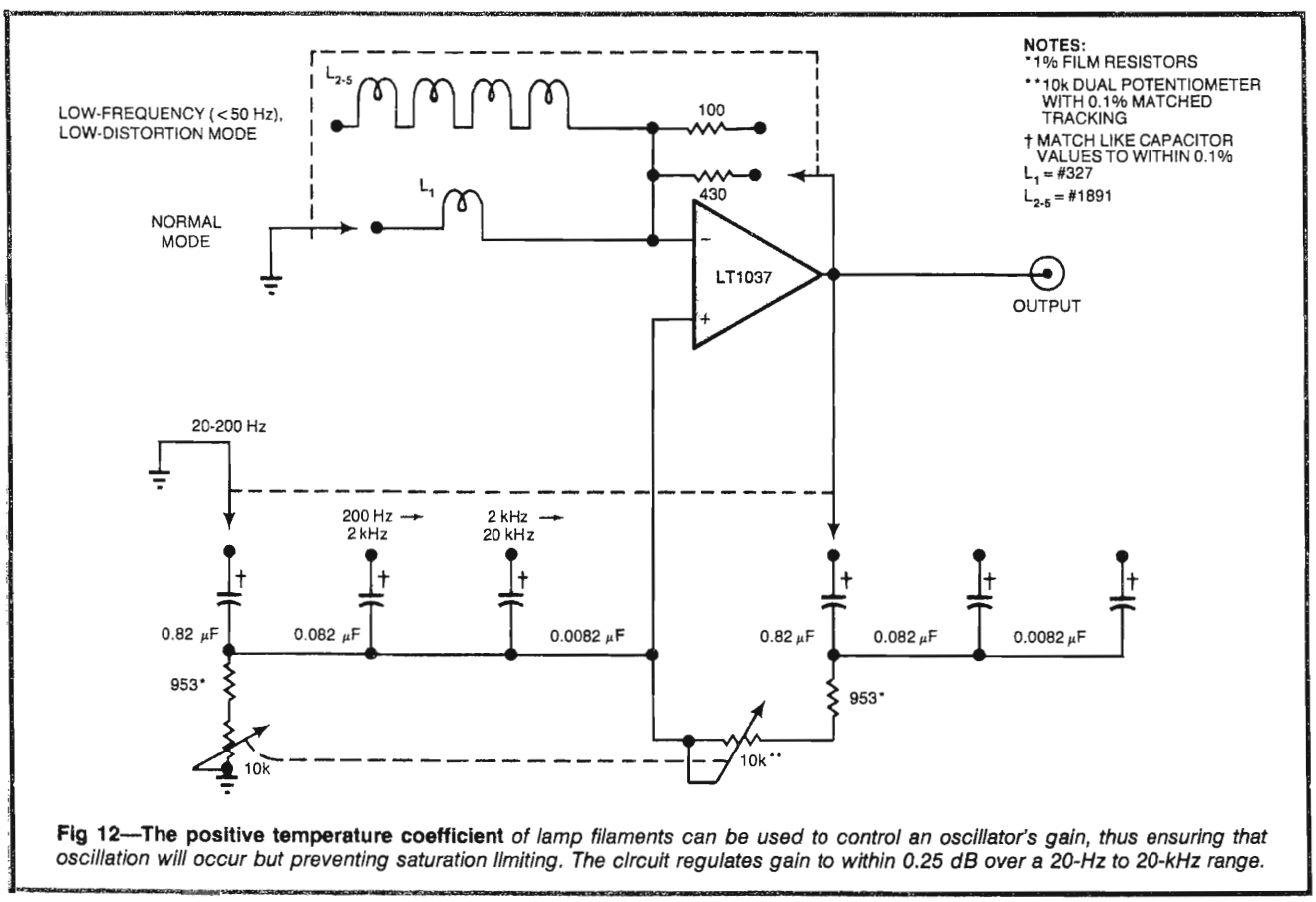


Fig 12—The positive temperature coefficient *of lamp filaments can be used to control an oscillator's gain, thus ensuring that oscillation will occur but preventing saturation limiting. The circuit regulates gain to within 0.25 dB over a 20-Hz to 20-kHz range.*

Thermal technique allows low flow-rate measurements

Fig 8 illustrates a convenient alternative technique; it generates an output whose frequency is a linear function of flow rate, and it achieves high accuracy at flow rates as low as 1 ml/min.

This circuit operates by measuring the differential temperature between two sensors arranged as shown in **Fig 9.** One sensor, T_1, measures the fluid's temperature before the fluid is heated by **Fig 8**'s 15Ω heater. The second sensor, T_2, measures the temperature rise induced into the fluid by the heater. The sensors' difference signal appears at A_1's output and is amplified by A_2, whose time constant is set via the 10-MΩ pot.

Fig 10 shows A_2's output vs flow rate—an inverse relationship. A_3 and A_4 linearize this relationship while providing a frequency output. A_3 functions as an integrator biased by the LT1004 diode and 383-kΩ input resistor; its output is compared with A_2's output at A_4. Large inputs from A_2 force the integrator to run for a long time before A_4 can go high, turning Q_1 On and resetting A_3. For small inputs from A_2, A_3 does not have to integrate very long before resetting action occurs. Thus, the configuration oscillates at a frequency inversely proportional to A_2's output voltage, yielding a frequency that linearly corresponds to flow rate.

This circuit requires attention to several thermal considerations. First, the amount of power dissipated into the fluid stream should be constant to maintain calibration. Ideally, you could measure the volt-ampere product at the heater resistor and construct a control loop to maintain constant dissipation. However, the resistor specified in **Fig 8** has a sufficiently small drift with temperature that you can assume constant dissipation with a fixed-voltage drive.

In addition, the fluid's specific heat affects calibration. **Fig 10**'s curves illustrate circuit performance for distilled water. To calibrate this circuit, set the flow rate to 10 ml/min and adjust the flow-calibration-trim pot for a 10-Hz output. The response-time adjustment allows you to filter out flow aberrations due to mechanical limitations in the pump driving the system.

A thermally based anemometer

Fig 11 shows another thermally based flow meter, but this design measures air or gas flow. It operates by measuring the energy required to maintain a heated resistance wire at a constant temperature. A type 328 lamp makes a good sensor for such a circuit because of the lamp's positive temperature coefficient and ready availability. The lamp is modified for this circuit by removal of its glass envelope.

The lamp forms one leg of a bridge, which amplifier A_1 monitors. Q_1 then current amplifies A_1's output and drives the bridge. The 500-pF and 0.01-μF capacitors and the 220Ω resistor ensure stability.

When power is applied to this circuit, the lamp's resistance is low, and Q_1 tries to turn full On. As current flows through the lamp its temperature quickly rises, forcing its resistance to increase, raising the voltage at A_1's minus (−) input. Q_1's emitter voltage then reduces, and the circuit finds a stable operating point. To keep the bridge balanced, A_1 attempts to force the lamp's resistance—and hence its temperature—to remain constant.

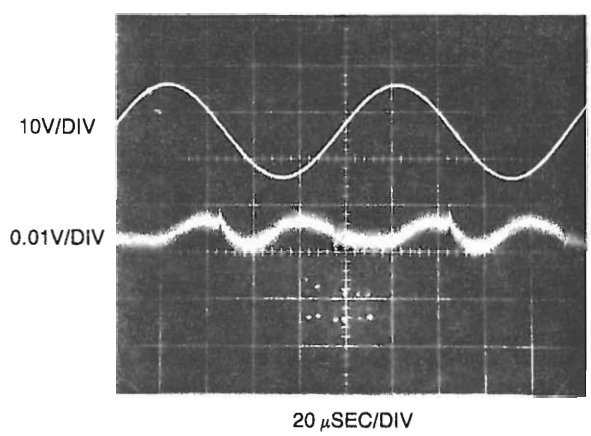


Fig 13—At a 10-kHz output, *the circuit in* ***Fig 12*** *exhibits less than 0.003% harmonic distortion. Most of this distortion is due to second-harmonic content, though some crossover disturbance is also noticeable.*

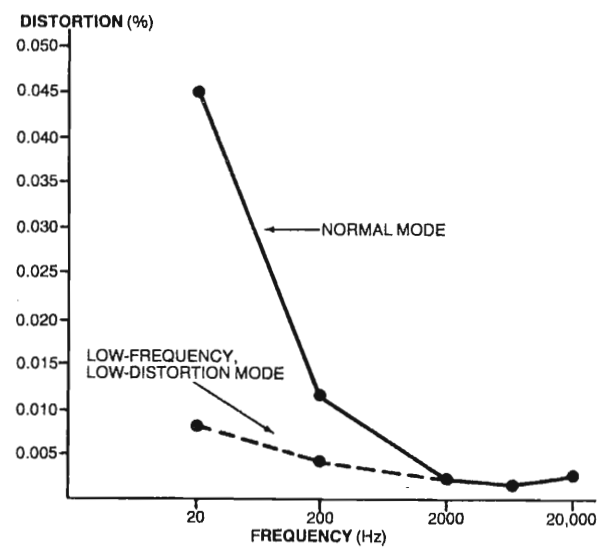


Fig 14—At low frequencies, *the* ***Fig 12*** *circuit's distortion increases. Achieving better distortion performance at the expense of reduced output amplitude, a low-frequency mode makes use of four lamps to increase the thermal time constant.*

A lamp filament can serve as an anemometer

The 10-kΩ and 2-kΩ bridge resistance values allow the lamp to operate just below the point of incandescence—a temperature sufficiently high to minimize the effect of ambient temperature shifts on circuit operation. Under these conditions, the only physical parameter that can influence the lamp's temperature is a change in the dissipation characteristic, and airflow provides such a change. Air moving past the lamp tends to cool it, and Q_1's emitter voltage must therefore increase to raise the lamp's temperature back up to its normal operating point. Q_1's emitter voltage is thus nonlinearly but predictably related to the airflow rate. A_2, A_3 and the array transistors form a circuit that squares and amplifies Q_1's emitter voltage to yield a linear, calibrated output vs airflow rate.

To use the circuit, place the lamp in the airflow so its filament is at a 90° angle to the flow direction. Next, either shut off the flow or shield the lamp from it and adjust the zero-flow pot for a 0V circuit output. Then, expose the lamp to a 1000-fpm airflow and adjust the full-flow pot for a 10V output. These adjustments influence each other and must be repeated until both end points are at the correct level. When adjustment is completed, the circuit is accurate to within 3% over the 0- to 1000-fpm range.

A thermally stabilized oscillator

Fig 12 employs the positive temperature coefficient of lamp filaments in a modern adaptation of a classic circuit. In any oscillator, it is necessary to control gain, as well as phase shift, at the frequency of interest. If gain is too low, oscillation won't occur, and too much gain can cause saturation limiting.

The circuit in **Fig 12** uses a variable Wien bridge to provide frequency tuning from 20 Hz to 20 kHz. The lamps' positive temperature coefficients furnish the gain control. When power is first applied in the normal mode, lamp L_1's resistance is low; thus gain is high, and the oscillation amplitude builds. As amplitude builds, though, the lamp current increases, causing heating and an increase in resistance. This resistance increase in turn reduces amplifier gain, and the circuit finds a stable operating point. The lamp's gain-regulating behavior is flat within 0.25 dB over the circuit's 20-Hz to 20-kHz range. **Fig 13**'s top trace shows circuit operation at 10 kHz.

The lower trace in **Fig 13** shows harmonic distortion, which is less than 0.003%. The distortion is primarily due to second-harmonic content, and some crossover disturbance is also noticeable. The low resistance values in the Wien network and the LT1037's 3.8-nV/$\sqrt{\text{Hz}}$ noise spec eliminate amplifier noise as an error term.

At low frequencies, the thermal time constant of the small L_1 lamp begins to introduce distortion levels higher than 0.01%. Such distortion is due to hunting as the oscillator's frequency nears a level corresponding to the lamp's thermal time constant. Switching to the low-frequency, low-distortion mode eliminates this effect at the expense of reduced output amplitude and longer amplitude settling time. This mode employs four larger lamps to provide a longer thermal time constant. **Fig 14** illustrates the performance of both modes. **EDN**

References

1. "Flowmeter," *Multiplier Application Guide,* Analog Devices Inc, Norwood, MA, pgs 7-9.
2. Olson, J V, "A High-stability Temperature-controlled Oven," SB Thesis, Massachusetts Institute of Technology, Cambridge, MA, 1974.
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Author's biography

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and -instrumentation design. He has served in related capacities at National Semiconductor Corp, Arthur D Little Inc and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art and collecting antique scientific instruments.

Monolithic power-buffer IC drives difficult loads

A high-speed monolithic buffer amplifier simplifies the driving of analog signals into nonlinear or reactive loads. Moreover, the IC's self-protection features cover a variety of possible output fault conditions.

Jim Williams, *Linear Technology Corp*

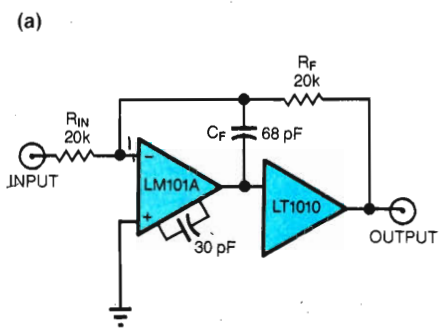
A frequent system requirement involves driving analog signals into nonlinear or reactive loads. Some examples of such difficult loads are cables, transformers, motors and sample/hold circuits. Although several power-buffer ICs are available, there are none optimized for driving problem loads.

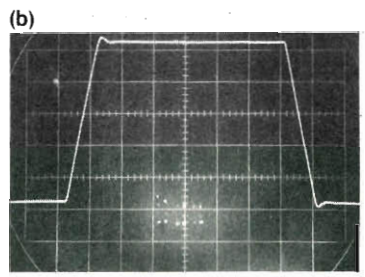
The Model LT1010 power-buffer IC, on the other hand, can isolate and drive almost any reactive load. What's more, the device includes current-limiting and thermal-overload protection, guarding the IC against fault conditions. The combination of high speed, output protection and reactive-load-driving capability (see **box,** "Physiology of the LT1010") make the device useful in a variety of practical situations.

Fig 1a shows the LT1010 inserted in an operational amplifier's feedback loop. At low frequencies, the buffer is effectively within the feedback loop; its offset voltage and gain error are negligible. At higher frequencies, however, feedback occurs through C_F. Therefore, the phase shift resulting from load capacitance acting in combination with the buffer's output resistance doesn't produce loop instability.

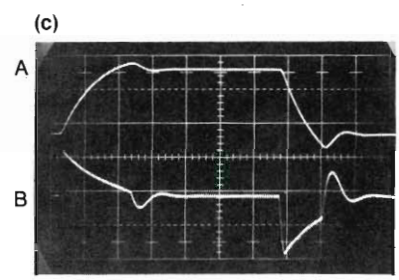
Fig 1b illustrates circuit performance when the LT1010 drives a 50Ω, 0.33-μF load. Even if you increase the load to a brutal 2 μF, the circuit is still stable, as borne out by trace A in (**c**). Trace B, however, shows that the large capacitance requires substantial current from the buffer. Note also that you can obtain improved damping by adjusting the R_FC_F time constant. Though this circuit is quite useful, its speed is limited by that of the op amp.

There are ways to overcome the op-amp limitation while maintaining good dc characteristics. In **Fig 2a,** the LT1010 combines with a wideband gain stage (Q_1





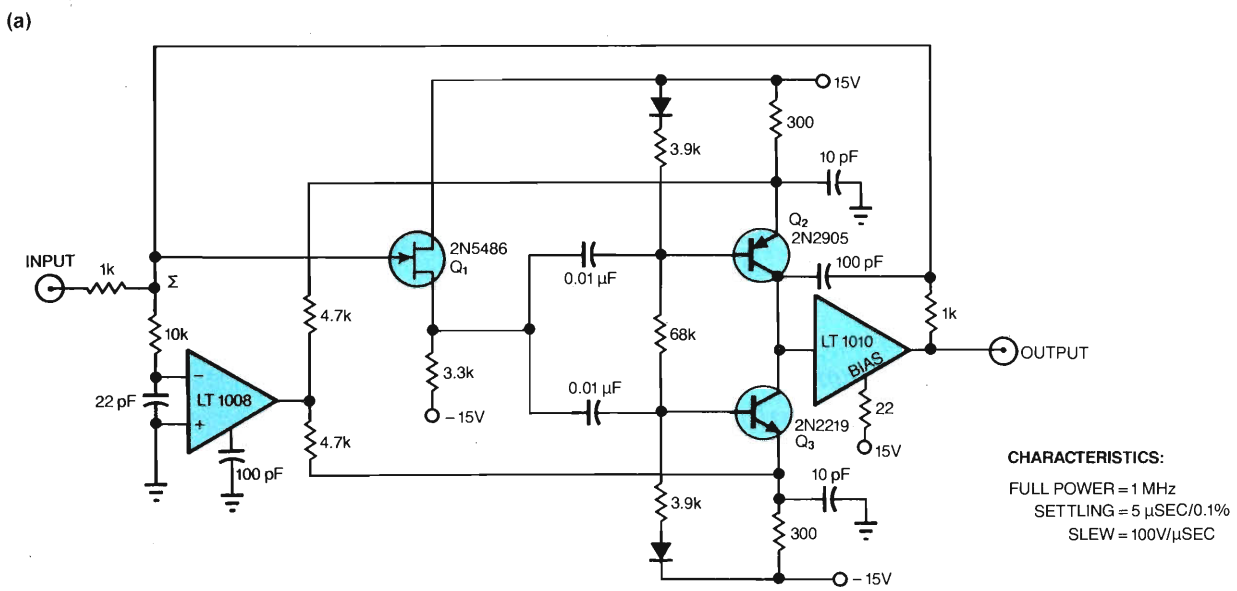
VERTICAL	HORIZONTAL
2V/DIV	20 μSEC/DIV



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	50 μSEC/DIV
B	200 mA/DIV	50 μSEC/DIV

Fig 1—Inserted in a feedback loop, *the LT1010 effectively isolates an operational amplifier from highly capacitive loads. The photos show the circuit's response with a 0.33-μF* **(b)** *and a 2-μF* **(c)** *load.*

Amplifier scoffs at reactive loads



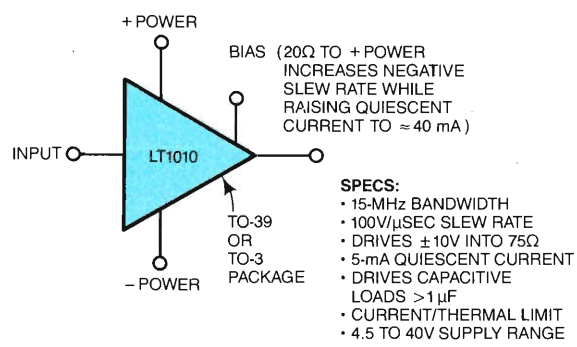
Physiology of the LT1010

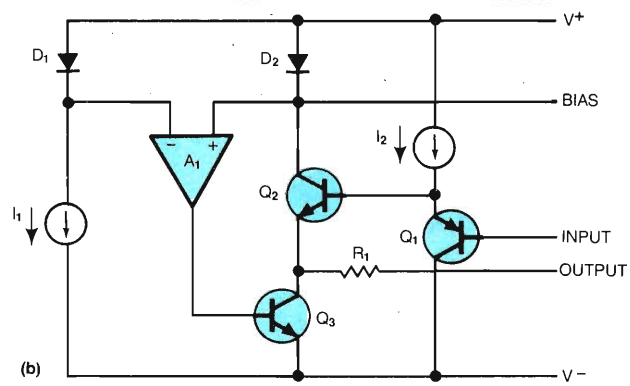
Bob Widlar, *Linear Technology Corp*

The schematic diagram in the **figure** shows the basic elements of the LT1010 buffer's design. The op amp drives the output sink transistor Q_3 so that the output follower's collector current never drops below the quiescent current (determined by the area ratio of D_1 and D_2). As a result, the high-frequency response is essentially that of a simple follower, even when Q_3 is supplying the load current. The internal feedback loop is isolated from the effects of capacitive loading in the output lead.

The scheme is not perfect; the rate of rise for sinking current is noticeably lower than that for sourcing current. You can mitigate this difference by connecting a resistor from the bias terminal to V^+, thereby raising quiescent current. One of the design's features is that the output resistance is largely independent of the follower's quiescent current or the output load current. Also, the output can swing to the negative rail, a particularly useful feature for single-supply operation.

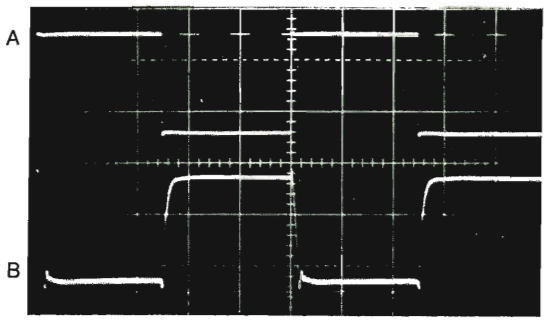
As far as stability is concerned, the buffer is no more sensitive to supply bypassing than slower op amps. The 0.01-µF ceramic capacitors usually recommended for op amps are adequate for low-frequency work. As always, it's prudent to keep capacitor leads short and to use a ground plane, especially when operating at high frequencies.





Featuring a bias pin to optimize negative slewing, *the LT1010 offers high speed and the capability to drive highly reactive loads. The device is available in a TO-39 package or the heftier TO-3 package.*

(b)



TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	1 μSEC/DIV
B	10V/DIV	1 μSEC/DIV

Fig 2—Faster than monolithic-op-amp configurations, *this discrete circuit offers good dc and high-speed characteristics. The configuration, a low-distortion, unity-gain inverting amplifier, is similar in concept to* ***Fig 1****'s circuit.*

through Q_3) to form a fast inverting configuration. The LT1010 dc-stabilizes the gain stage by biasing Q_2 and Q_3 emitters to force a 0V dc potential at the circuit's summing junction.

The frequency rolloffs of the fast stage and the op amp are the optimum values to provide smooth overall circuit response. A higher speed is possible because the circuit's dc-stabilization path is in parallel with the buffer. Even when this circuit drives a heavy 600Ω/2500-pF load, as **Fig 2b** illustrates, the output (trace B) faithfully follows the input (trace A).

Amplifier drives video lines

In many cases, dc stability is unimportant in applications requiring ac gain. **Fig 3a** shows how to combine the LT1010's load-handling capability with a fast discrete gain stage. Q_1 and Q_2 form a differential stage that drives the buffer IC in single-ended fashion. The capacitively terminated feedback divider establishes unity dc gain for the circuit while allowing ac gains as high as 10.

Inadequate supply bypassing can compromise the buffer's slew rate. With output current slewing much faster than 100 mA/μsec, the use of 10-μF solid-tantalum capacitors is a good practice, although in some applications bypassing from the positive to the negative supply will suffice.

When used in conjunction with an op amp and heavy resistive or capacitive loads, the buffer can couple into supply leads that are common to the op amp, thereby causing stability problems with the overall loop. The 10-μF tantalum capacitors can usually provide adequate bypassing in these situations. Another solution is to use smaller capacitors in conjunction with series decoupling resistors. Finally, note that some op amps have much better high-frequency rejection for one supply than for the other, so bypassing requirements are less stringent for this supply.

In many applications, the LT1010 requires heat-sinking. Thermal resistance from junction to still air is 150°C/W for the TO-39 package, 60°C/W for the TO-3 package. Circulating air, use of a heat sink or mounting of the TO-3 package to a pc board reduces thermal resistance. In dc circuits, it's easy to compute the buffer's dissipation. On the other hand, in ac circuits the signal waveshape and the nature of the load determine dissipation. For example, with reactive loads, peak dissipation can be several times the average value. It's particularly important to determine dissipation when driving large-load capacitances.

The LT1010 has both instantaneous current limiting and thermal-overload protection. The device doesn't use foldback limiting, and so allows the buffer to drive complex loads without limiting. Because of this feature, it's capable of dissipating power in excess of its continuous ratings.

Usually the thermal-overload protection limits the dissipation and prevents damage. However, with voltages higher than 30V across the conducting output transistor, the thermal limiting isn't fast enough to ensure protection. As long as the load current is limited to 150 mA, however, the thermal protection is effective with voltages to 40V across the conducting output transistor.

When driving capacitive loads, the LT1010 prefers to be driven from a low source impedance at high frequencies. Some low-power op amps are marginal in this respect. You might need to take some care to avoid oscillations, especially at low temperatures. Bypassing the buffer's input with 200 pF min solves the problem. Raising the IC's operating current is also effective, but this is only feasible with the TO-3-packaged version.

Bob Widlar is a design engineer for the Milpitas, CA-based company. For more information on the LT1010, **Circle No 725.**

Feedback buffer isolates op amp

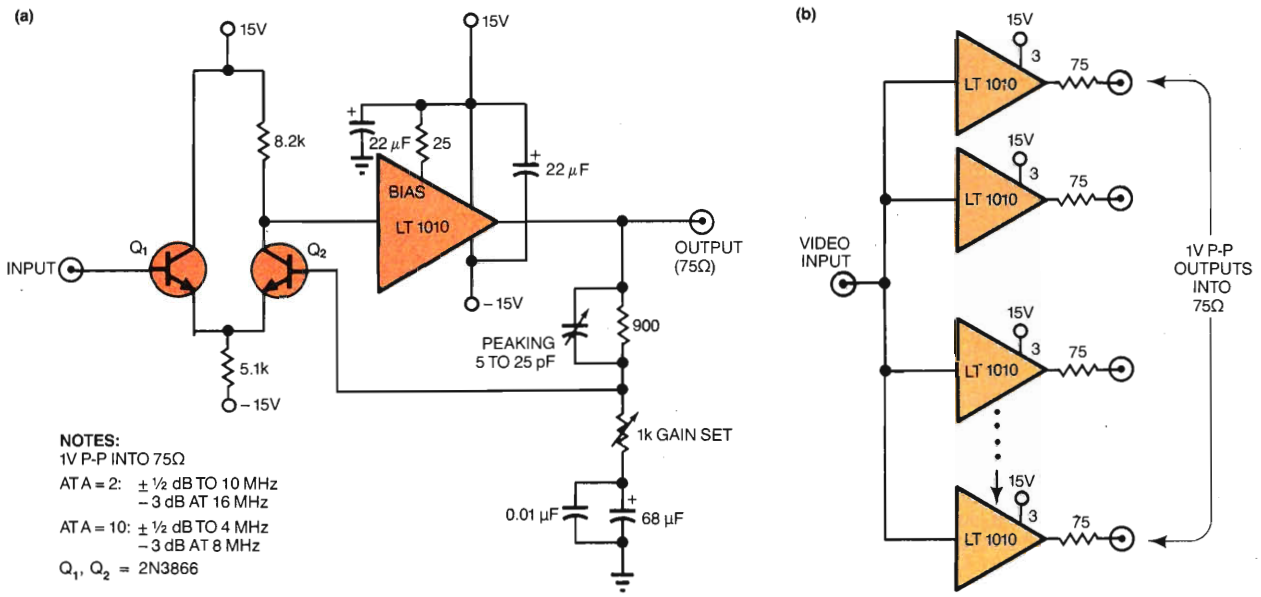


Fig 3—Suitable for video applications, *these circuits provide standard 1V p-p composite-video signals into 75Ω lines. The circuit in* ***(a)*** *provides variable gain. The one in* ***(b)*** *allows you to drive multiple video lines.*

Using a 20Ω bias resistor, the circuit delivers 1V p-p into a typical 75Ω video load. For applications sensitive to National Television Systems Committee (NTSC) requirements, reducing the bias resistor's value aids performance. For a gain of 2, the response is flat within ±0.5 dB to 10 MHz; the −3-dB point occurs at 16 MHz. At a gain of 10, the gain is flat within ±0.5 dB to 4 MHz; the −3-dB point is at 8 MHz. For best performance, optimize the peaking adjustment under loaded-output conditions.

Fig 3b shows a video-distribution amplifier. In this example, the resistors in series with the outputs serve to reduce reflections from unterminated lines. If you know the lines' characteristics, you can tailor the resistor values accordingly. The 3Ω bias resistors provide a minor boost characteristic that helps the circuit meet NTSC gain-phase requirements. Into a 75Ω load, each 1V p-p output response is flat within ±0.15 dB to 6 MHz.

Buffer suits track/hold circuits

A track/hold (T/H) amplifier—a good example of difficult driving conditions—requires high capacitive-load-driving capability to achieve fast acquisition times.

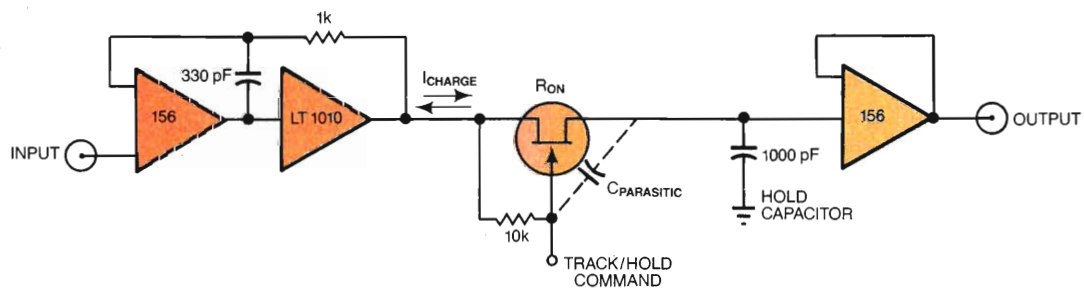


Fig 4—This basic T/H-amplifier design *presents conflicts between low pedestal (hold step) and fast acquisition time. A large hold capacitor reduces the former problem but increases the latter. The circuit also needs a fast level shifter to drive the FET's gate from TTL signals.*

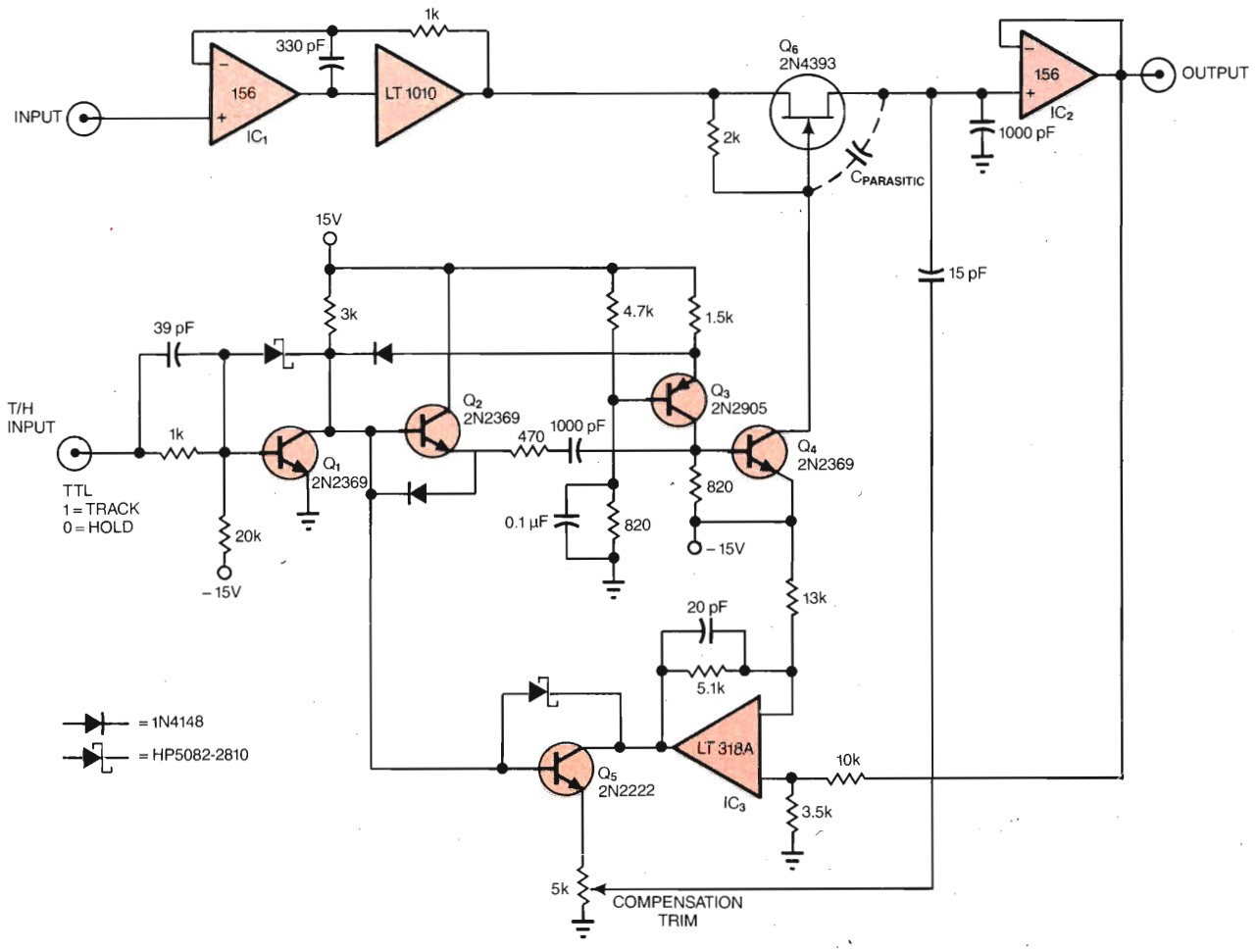


Fig 5—This fast, accurate T/H amplifier *uses discrete transistor circuitry to provide both low pedestal and fast acquisition time. It also features a very fast TTL-to-FET level shifter. The scheme uses a compensation technique to reduce parasitic-induced pedestal.*

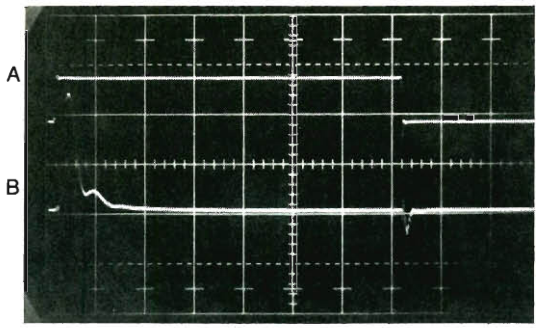
Moreover, you must consider other tradeoffs in developing a good design. The conceptual circuit in **Fig 4** illustrates some of the issues involved. Fast acquisition requires high charging currents and dynamic stability. To have a reasonable droop rate, the hold capacitor must be appropriately large. If it's too large, however, the On resistance of the FET switch will affect the acquisition time.

If you use FETs with low On resistance, the parasitic gate-source capacitance becomes significant, and a substantial amount of charge is removed from the hold capacitor when the gate switches off. This charge removal causes the stored voltage to change abruptly when the circuit switches into hold mode. This phenomenon, called "hold step" or "pedestal," limits the T/H amp's accuracy. You can reduce the effect by increasing the hold capacitor's value, but then (again) acquisition time suffers. Finally, because a TTL-compatible input is often desirable, the FET requires a level shifter. This level shifter must provide adequate pinchoff voltage over the entire range of circuit inputs. It must also be fast. Delays result in aperture errors and thereby introduce dynamic sampling inaccuracy.

Fig 5 shows a LT1010-based circuit that manifests fast, precise T/H performance. Q_1 through Q_4 form a high-speed TTL-compatible level shifter. The total delay, from the TTL input's switching into hold mode to Q_6's turn-off, is 16 nsec. Baker-clamped Q_1 biases Q_3's emitter to switch level shifter Q_4. Q_2 drives a heavy feed-forward network, speeding Q_4's switching. This stage minimizes aperture errors while providing the necessary level shifting for Q_6's gate. Q_5 and IC_3 compensate for the pedestal error that results from Q_6's parasitic gate-source capacitance.

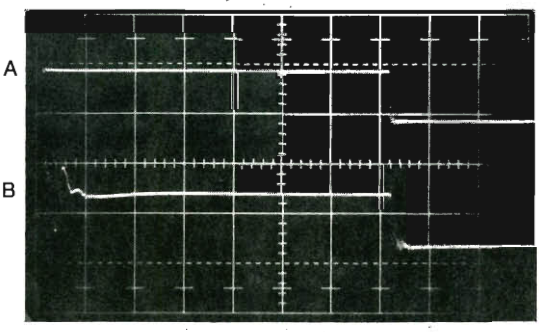
Video amplifiers deliver 1V p-p signals

(a)



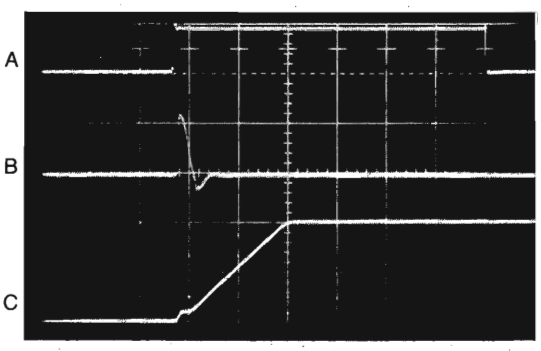
TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	500 nSEC/DIV
B	10 mV/DIV (AC COUPLED)	500 nSEC/DIV

(b)



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	500 nSEC/DIV
B	50 mV/DIV	500 nSEC/DIV

(c)



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	500 nSEC/DIV
B	100 mA/DIV	500 nSEC/DIV
C	5V/DIV	500 nSEC/DIV

Fig 6—Performance of Fig 5's T/H circuit *is evident in these scope photos. The hold step (pedestal) is seen with* **(a)** *and without* **(b)** *compensation. The LT1010's heavy current contribution to fast acquisition time is seen in* **(c).**

The amount of charge removed from the hold capacitor by the parasitic capacitance is signal dependent (Q=CV). To compensate for this error, IC_3 measures the circuit's output and biases the Q_5 switch. Each time the circuit switches into hold mode, a scaled amount of charge is delivered through the 5-kΩ/15-pF network in Q_5's emitter to compensate for the parasitic-related charge removal. Biasing of IC_3's inverting input is such that negative supply shifts (which alter the charge removed through the parasitic capacitance) are accounted for in the compensating charge. To set the compensation, you ground the signal input, clock the T/H line and adjust the pot for minimum disturbance at the circuit output.

Fig 6a depicts circuit performance. When the T/H input (trace A) goes into hold mode, charge cancellation occurs and the output (trace B) exhibits less than a 250-μV pedestal error within 100 nsec. Without compensation **(b)**, the error would be 50 mV (trace B). **Fig 6c** shows the LT1010's contribution to fast acquisition with a 10V step. Trace B shows the IC delivering more than 100 mA to the hold capacitor; trace C shows the output voltage slewing and settling to final value. Note that the acquisition time is limited by amplifier settling time, and not by capacitor charge time. The circuit features a 2-μsec acquisition time to a ±0.01% error band, a 100-nsec max hold settling time to a 1-mV error band, and a 16-nsec aperture time.

Because of their reactive nature, motors present tough driving problems. A motor/tachometer combina-

NOTES:
DIODES = 1N4002
MOTOR-GENERATOR = TRANSICOIL 1215-115
MOTOR = 12V/4500 RPM
TACH SLOPE = 1.9V/1000 RPM

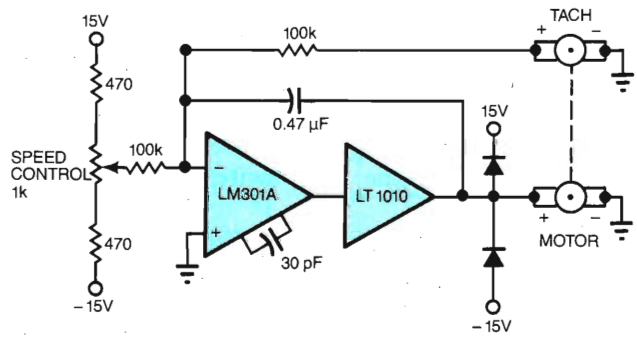


Fig 7—This simple motor-tachometer circuit *takes advantage of the LT1010's ability to drive heavy reactive loads. The circuit allows speed control in both directions, thanks to the tachometer's bipolar output.*

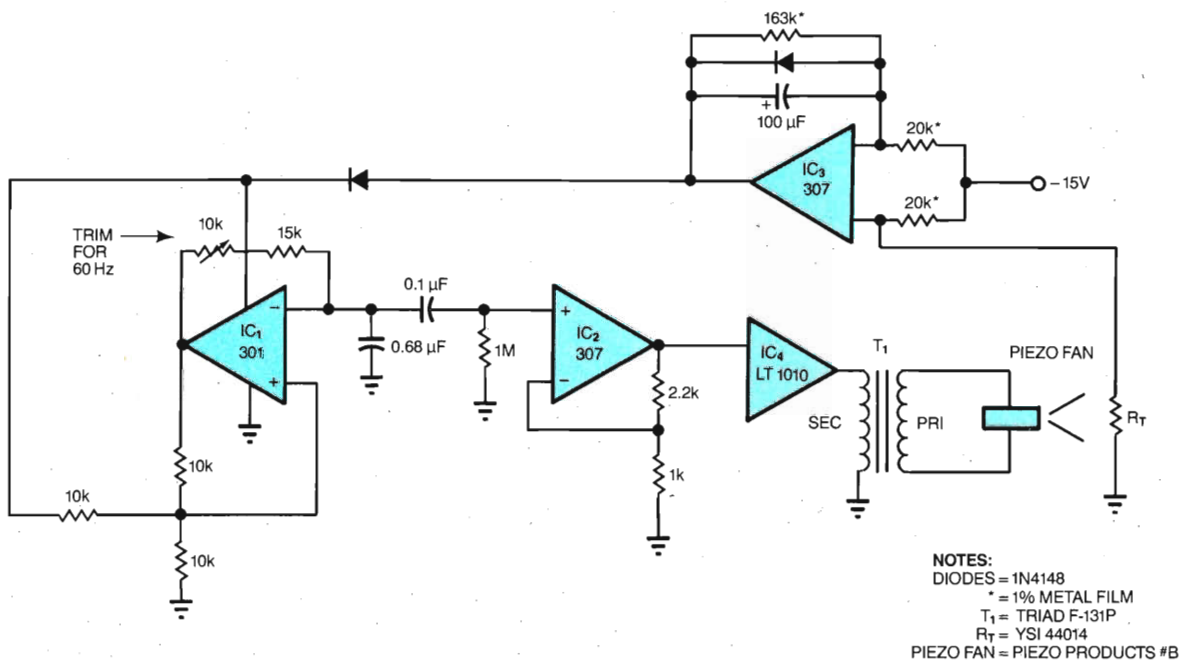


Fig 8—An instrumentation temperature controller is easy to build *with new electrostatic fans. The thermistor in the fan's exhaust stream is the temperature-sensing element. The circuit features a long time constant, to reduce audible and annoying hunting. The LT1010 easily handles the highly reactive transformer/piezo-fan load.*

tion (**Fig 7**) exemplifies such a problem. The tachometer signal feeds back for comparison with a reference current; the 301A amplifier closes a control loop. The 0.47-µF capacitor provides compensation for stability. Because the tachometer has a bipolar output, the speed is controllable in both directions with clean transitions through zero. The LT1010's thermal protection is particularly useful in this application, preventing IC destruction in the event of mechanical overload or malfunction.

The circuit shown in **Fig 8** controls a fan motor's speed in order to regulate instrument temperature. The fan in this example is a new electrostatic type that requires high-voltage drive. Upon power-up, the thermistor (located in the fan's exhaust stream) has a high value. This unbalances the IC_3-amplifier-driven bridge, IC_1 receives no power, and the fan doesn't run.

As the instrument enclosure warms up, the thermistor value decreases until IC_3 begins to oscillate. IC_2 provides isolation and gain, and IC_4 drives the transformer to generate high voltage for the fan. In this fashion, the loop acts to maintain a stable instrument temperature by controlling the fan's exhaust rate. The 100-µF capacitor across the error amplifier's pins is typical of such configurations. Fast time constants produce audible and annoying "hunting" in the servo. The optimum values for the time constant and stage gain depend on the thermal and airflow characteristics of the enclosure being controlled. **EDN**

Author's biography

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and -instrumentation design. He has served in related capacities at National Semiconductor Corp, Arthur D Little Inc and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art and collecting antique scientific instruments.

Article Interest Quotient (Circle One)
High 473 Medium 474 Low 475

Monolithic CMOS-switch IC suits diverse applications

Using a CMOS-switch building-block IC, you can take advantage of the special attributes of switch-based circuitry to produce a variety of high-performance, low-package-count circuits.

Jim Williams, *Linear Technology Corp*

CMOS analog-IC design is largely based on charge manipulation. Switches and capacitors are the elements used to control and distribute the charge. For example, monolithic filters, data converters and voltage-level converters rely on the excellent characteristics of CMOS-switch ICs. These techniques, heretofore inherent only in the internal construction of various ICs, are now exploitable at the board level, thanks to a CMOS-switch IC, the LTC1043. This device, which features multipole switching and a self-driven nonoverlapping clock, is suitable for use in a wide variety of circuit configurations that are impractical to realize with other switches. An in-depth look at a sampling of circuits that take advantage of this IC helps illustrate important features of the device.

What's in a CMOS-switch IC?

Before we examine specific application examples, it's useful to take a look at what's on the LTC1043's chip. **Fig 1** shows the device's block diagram. The oscillator, free-running by default at 200 kHz, drives a nonoverlapping clock. Placing a capacitor from pin 16 to ground shifts the oscillator frequency downward to any desired value. You can also drive the pin from any available source, thereby synchronizing the switches to external circuitry.

The nonoverlapping clock controls both dpdt switch sections. The nonoverlapping character of the drive prevents simultaneous conduction in the series-connected switch sections. Charge-balancing circuitry cancels the effects of stray capacitance. You can use pins 1 and 10 as guards for pins 3 and 12 in particularly sensitive applications.

Although the device's operation appears simple, it permits surprisingly sophisticated circuit functions. Additionally, the IC's carefully controlled switching characteristics make it relatively easy to implement such functions. What's more, the circuit permits the elimination of discrete timing and charge-balancing compensation networks, thereby minimizing component count and trimming requirements.

Classic analog circuits work by using continuous functions; you usually describe their operation in terms of voltage and current. On the other hand, circuits based on switched-capacitor technology are sampled-data systems that approximate continuous functions; bandwidth is limited by the sampling frequency. The distribution of charge over time better describes their operation. To better understand the circuits that follow, keep this distinction in mind.

Analog sampled-data and carrier-based systems are less common than true continuous approaches, and developing a working familiarity with them requires some thought. Switched-capacitor approaches have greatly aided analog MOS-IC design. The switch IC used in this article's designs brings many of the freedoms and advantages of CMOS-IC switched-capacitor circuits to the board level, thereby providing a valuable addition to available design techniques.

For the first example, the circuit in **Fig 2** uses the

CMOS-switch IC reduces parts count

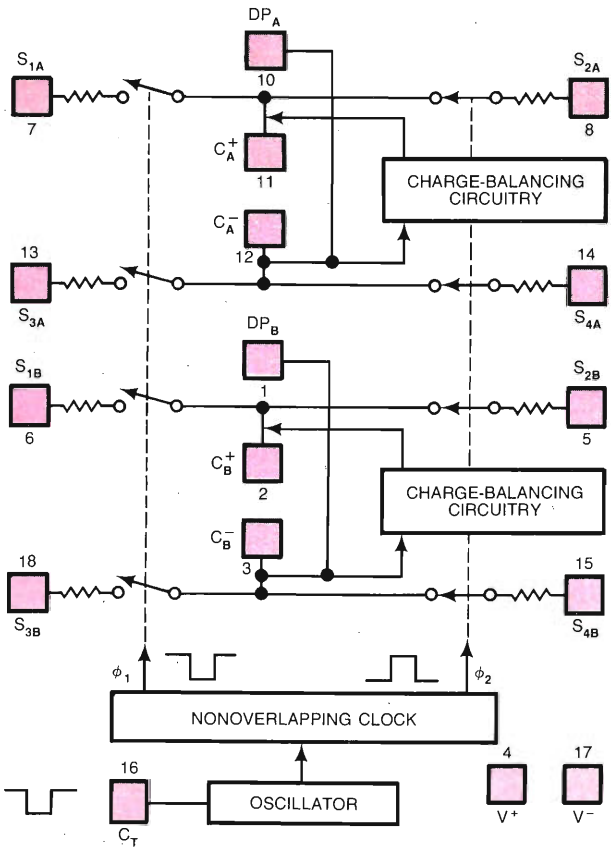


Fig 1—A CMOS quad-switch IC, *the LTC1043 features a nonoverlapping clock that prevents simultaneous conduction in its series-connected switch sections. Its free-running clock frequency is 200 kHz; you can, however, adjust this rate downward or run the IC from an external clock.*

LTC1043 to build a simple, precise instrumentation amplifier. Using the quad-switch IC and an LT1013 dual op amp, the circuit produces a dual instrumentation amplifier with just two packages (the schematic shows one half of the dual). A single dpdt section converts the differential input signal to a ground-referenced, single-ended signal at the op amp's input. With the input switches closed, C_1 acquires the input signal.

When the input switches open, C_2's switches close and C_2 receives its charge. Continuous clocking forces the voltage on C_2 to equal the difference between the circuit's inputs. The 0.01-μF capacitor at pin 16 sets the switching frequency at 500 Hz. The amplifier's common-mode-rejection ratio (CMRR) exceeds 120 dB. Resistors R_1 and R_2 set the amplifier's gain in the conventional manner. Note that the action of the LTC1043 constitutes a switched capacitor lowpass filter, resulting in excellent high-frequency CMRR.

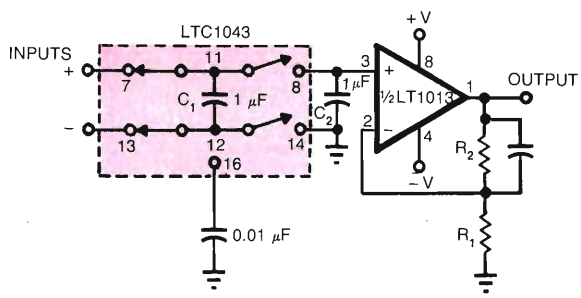
The circuit represents a simple, economical way to build a high-performance instrumentation amplifier. Its dc characteristics rival those of any hybrid or monolithic unit; moreover, it can operate from one 5V supply. The common-mode range includes the supply rails, allowing the circuit to read across shunts in the supply lines. The amplifier's specs are shown in **Fig 2.**

High-performance instrument amp

The circuit in **Fig 3** is similar to the preceding one, but it uses the LTC1043's remaining switches to construct a low-drift chopper amplifier. This approach maintains the true differential-input configuration, and achieves 0.1-μV/°C drift. As before, the differential input is converted to a single-ended potential at the switch IC's pin 7. The switching action at pins 7, 11 and 8 chops the voltage into a 500-Hz square wave; the ac-coupled IC_1 amplifies this chopped signal.

The switches at pins 12, 14 and 13 synchronously demodulate IC_1's ac-coupled, square-wave output. Because this switch section is driven synchronously with the input chopper, IC_2, the direct-coupled output amplifier receives proper amplitude and polarity information. This stage integrates the square wave into a dc voltage output. The divided output feeds back to pin 8 of the input chopper, where it serves as the zero-signal reference. Because the main amplifier is ac coupled, its dc terms do not affect overall circuit offset, resulting in the extremely low offset and drift noted in the specs. This circuit has lower offset and drift than any commercially available instrumentation amplifier.

You can use the ac-carrier approach of **Fig 3**'s circuit to make a lock-in amplifier. This circuit works by



SPECS:
OFFSET = 150μV
OFFSET DRIFT = 2 μV/°C
INPUT BIAS = 25 nA
GAIN = 1 + R_2/R_1
CMRR ≥ 120 dB FROM DC TO 20 kHz
COMMON-MODE RANGE = ±SUPPLIES
SUPPLY RANGE = +5V TO ±5V
SUPPLY CURRENT = 600 μA

Fig 2—This fully differential instrumentation amplifier *uses only one op amp, instead of the classic 3-op-amp connection. Its drift, offset and drift performance rival that of expensive hybrid and monolithic units.*

synchronously detecting the carrier-modulated output of the signal source. Because the desired signal information is contained within the carrier, the system constitutes an amplifier with an extremely narrow band. Components unrelated to the carrier are rejected; the amplifier only passes signals that are coherent with the carrier. In practice, lock-in amplifiers can extract signals 120 dB below the noise level.

Fig 4 shows a lock-in amplifier that uses a single LTC1043 section. In this application the signal source is a thermistor bridge that detects extremely small temperature shifts in a biochemical microcalorimetry reaction chamber. The 500-Hz carrier is applied at T_1's input. The transformer's output drives the thermistor bridge, which presents a single-ended output to IC_1.

A 60-Hz broadband noise source is also deliberately injected into IC_1's input (**Fig 5,** trace B). IC_4 detects the carrier's zero crossings; this IC's output clocks the LTC1043 (trace C). IC_1's output (trace D) shows the desired 500-Hz signal buried within the 60-Hz noise signal. The LTC1043's zero-crossing-synchronized switching at IC_2's positive input (trace E) causes IC_2's gain to alternate between plus and minus one.

As a result, IC_2 synchronously demodulates IC_1's output. IC_2's output comprises the demodulated carrier signal and noncoherent components. The desired carrier-amplitude and polarity information is discernible in IC_2's output; filtering at IC_3 extracts the information. To trim the circuit, adjust the phase potentiometer so that IC_4 switches when the carrier crosses through zero.

Control gain digitally

Besides low drift and high noise rejection, another area in amplifier design that can profit from switching technology is variable gain. It's a difficult task to design a wide-range, variable-gain block with good dc stability. Such configurations usually require relays or temperature-compensated FET networks in relatively expensive and complicated arrangements. The circuit in **Fig 6** uses the LTC1043 in a variable-gain amplifier that features continuously variable gain that's adjustable from zero to 1000. Other features are 20-ppm/°C gain stability and single-ended or differential inputs.

The circuit uses two LTC1043s. Frequency input F_{IN}, possibly generated by a host processor, clocks unit A; a 1-kHz source clocks unit B continuously. Both LTC1043s function as the sampled-data equivalent of a resistor, within the bandwidth set by unit A's 0.01-μF feedback capacitor. The time-averaged current delivered to the op amp's summing point by unit A is a function of the 0.01-μF capacitor's input-derived voltage and the commutation frequency at unit B, pin 16.

Low commutation frequencies result in small time-averaged current values; this situation produces the approximation of a large input resistor. Higher fre-

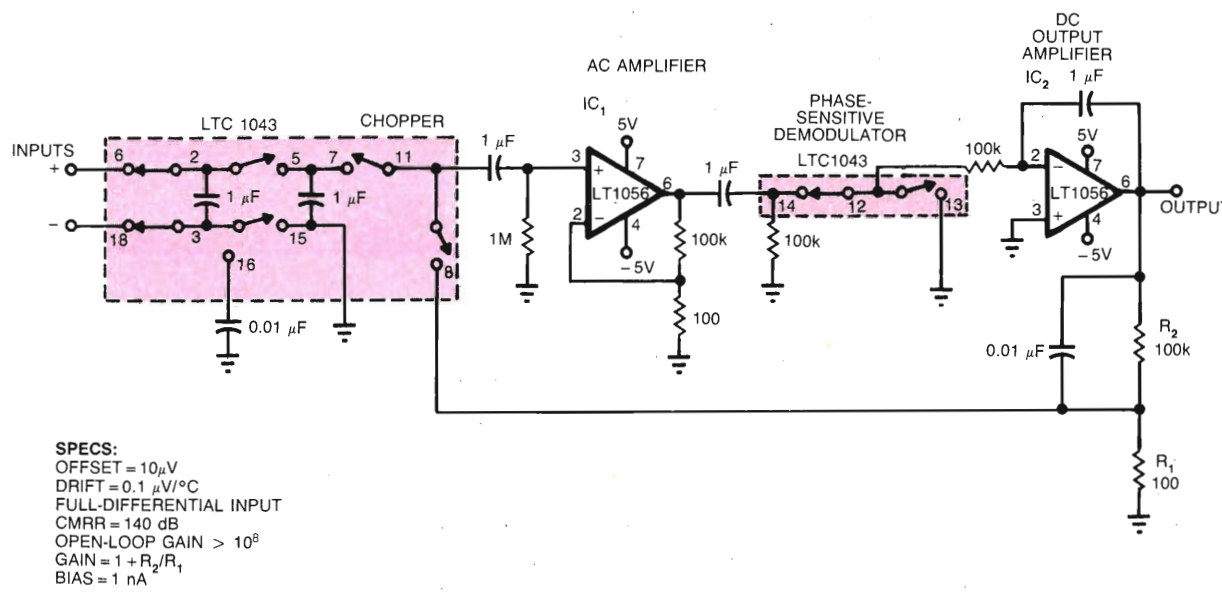


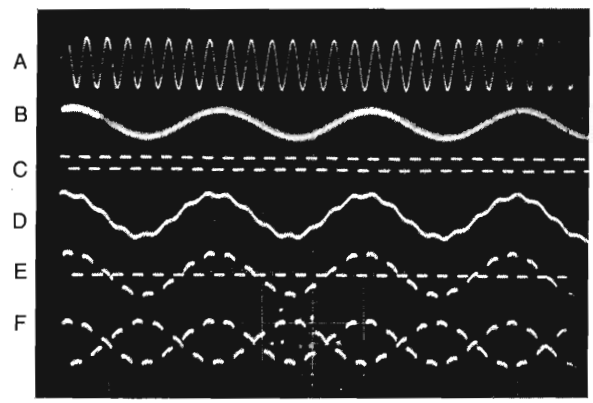
Fig 3—A chopper-stabilized configuration *allows this simple instrumentation amplifier to achieve 10-μV offset and 0.1-μV/°C drift. The fully differential circuit's other specs are impressive, too—140-dB common-mode rejection and 10^8 open-loop gain.*

quencies, on the other hand, produce a small equivalent input resistor. Unit B, in IC_1's feedback path, acts in a similar fashion. For the circuit values shown, the gain is $G=F_{IN}\div 10$.

Gain stability depends on the ratiometric stability between the 1-kHz and variable clocks (which could derive from a common source) and the ratio stability of the capacitors. For polystyrene types, the stability is typically 20 ppm/°C. The circuit's input, determined by the pin connections shown in **Fig 6,** can be either single ended or differential. What's more, although IC_1 is connected as an inverter, the circuit's overall transfer function can be either positive or negative in polarity. As shown, with pins 13A and 17A grounded and the input applied to pin 8A, the polarity is negative.

Linearize a platinum RTD

In another useful application, the LTC1043 can simplify the circuitry needed to condition and linearize a platinum RTD's output. The circuit shown in **Fig 7** is considerably simpler than instrumentation-amplifier designs; moreover, it operates from one 5V supply. By sensing the differential voltage across the 887Ω feedback resistor, IC_1 serves as a voltage-controlled, ground-referred current source. The LTC1043 section that performs this role presents a single-ended signal to IC_1's noninverting input, thereby closing the loop.



TRACE	VERTICAL	HORIZONTAL
A	2V/DIV	5 mSEC/DIV
B	2V/DIV	5 mSEC/DIV
C	50V/DIV	5 mSEC/DIV
D	5V/DIV	5 mSEC/DIV
E	5V/DIV	5 mSEC/DIV
F	5V/DIV	5 mSEC/DIV

Fig 5—These lock-in-amplifier waveforms *show what's happening in the circuit in* ***Fig 4.*** *By filter averaging the circuit's output (trace F), you can extract the modulated carrier's amplitude and polarity information, thereby eliminating the deleterious effects of the deliberately introduced 60-Hz noise in trace B.*

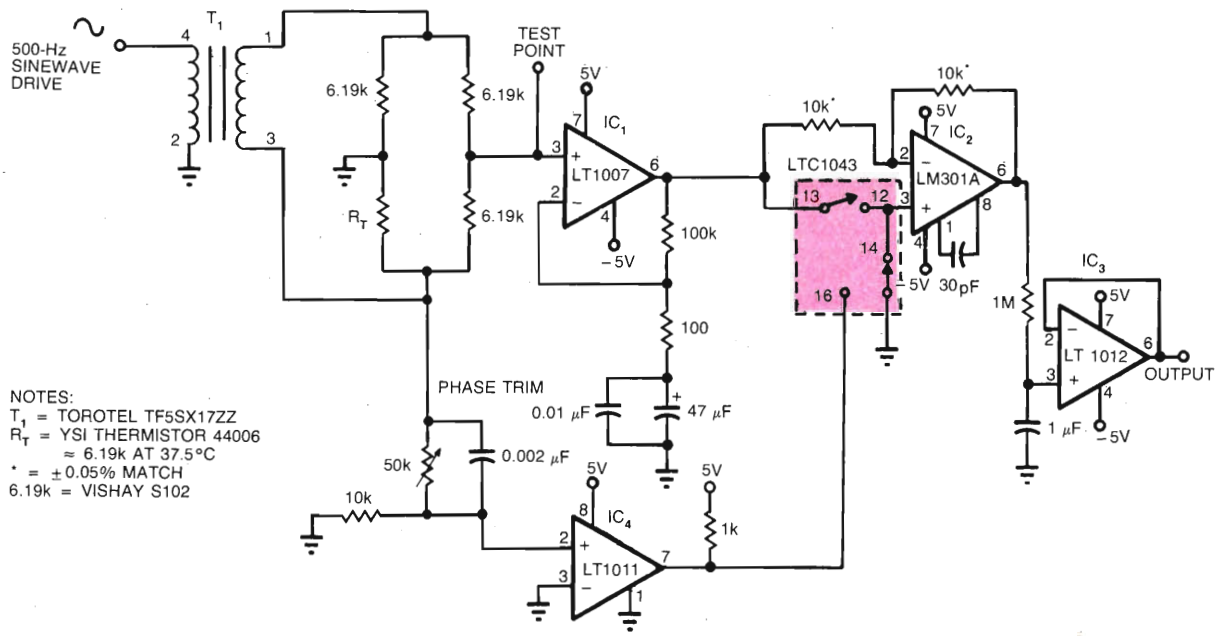


Fig 4—Using carrier modulation of the signal source, *this lock-in amplifier can extract signals 120 dB below noise level. The circuit uses a thermistor to detect extremely small temperature shifts. The amplifier rejects any signal components not related to the carrier frequency.*

The 2-kΩ, 0.1-μF combination sets amplifier rolloff well below the LTC1043's switching frequency, so the configuration is stable. Because IC_1's loop forces a fixed voltage across the 887Ω resistor, the current through R_P is constant. The 2.5V LT1009 reference fixes IC_1's operating point. The RTD's constant current forces the voltage across it to vary directly with its resistance, this parameter possessing a nearly linear, positive temperature coefficient.

The RTD's inherent nonlinearity could cause several degrees of error over the circuit's 0 to 400°C operating range. To counter this, IC_2 amplifies R_P's output while simultaneously supplying a nonlinearity correction. The portion of IC_2's output that feeds back to IC_1 (via the 10-kΩ/250-kΩ divider) effects the correction. This action causes the current supplied to R_P to shift slightly in its operating point, compensating (within ±0.05°C) for the sensor's nonlinearity.

The remaining LTC1043 section supplies a differential input to IC_2. This action permits the subtraction of an offsetting potential, derived from the LT1009, from

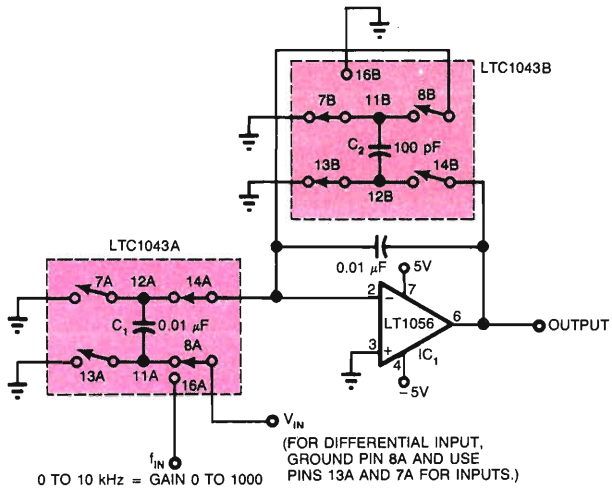


Fig 6—Featuring low drift and digitally controlled gain, *this amplifier uses switched-capacitor technology to allow continuously variable, selectable gains from zero to 1000. The switched-capacitor sections produce sampled-data equivalents of resistors.*

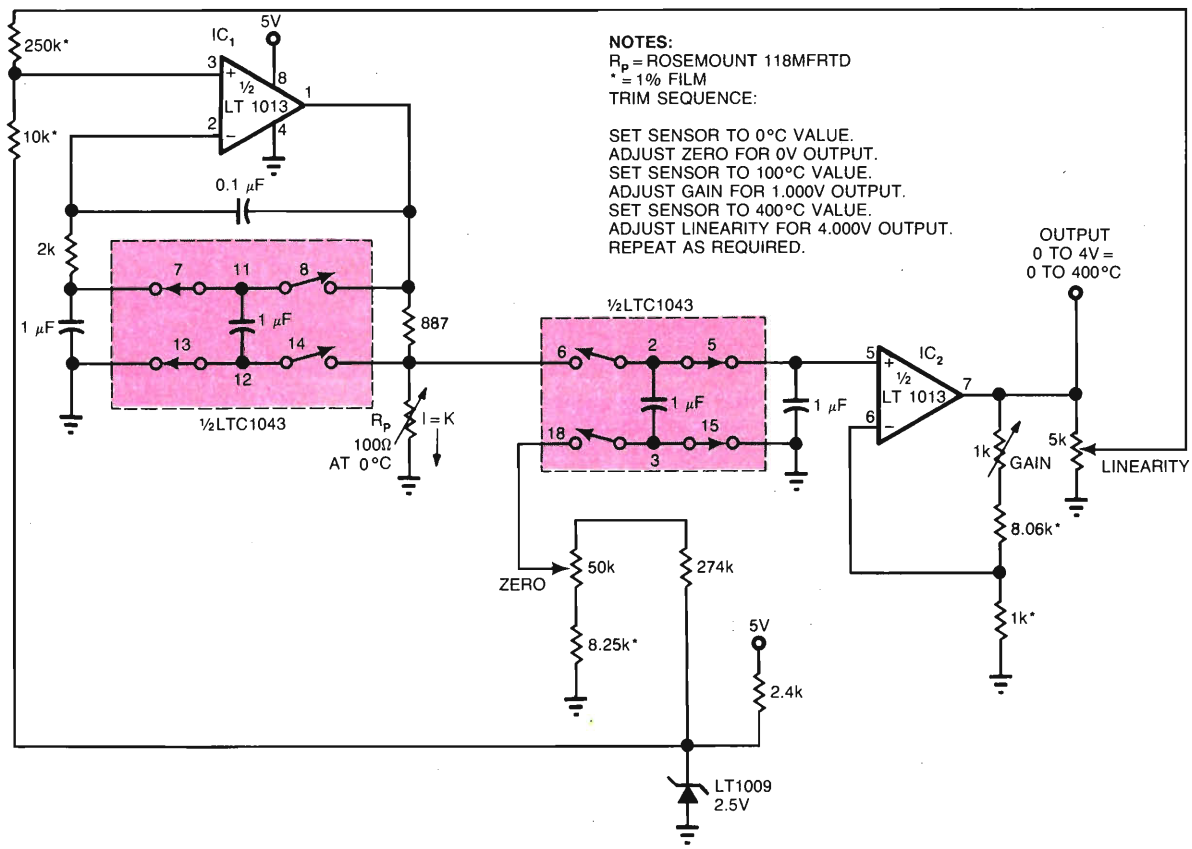


Fig 7—Demonstrating one way to linearize a platinum RTD element, *this circuit allows you to ground one side of the RTD to minimize noise. The circuit is simpler than instrumentation-amplifier designs and operates from one 5V supply; it features ±0.05°C accuracy.*

R_P's output. The scaling is such that 0°C produces 0V at IC_2's output. IC_2's feedback-component values set the gain; linearity correction derives from the output.

To calibrate this circuit, substitute a precision decade box for R_P. Set the box to the 0°C value (100.00Ω), then adjust the zero trim for 0.00V output. Next, set the decade box for 140°C output (154.26Ω) and adjust the gain trim for 1.400V output. Finally, set the box for 249.00Ω (400.00°C) and trim the linearity adjustments for 4.000V output. Reiterate this sequence until all

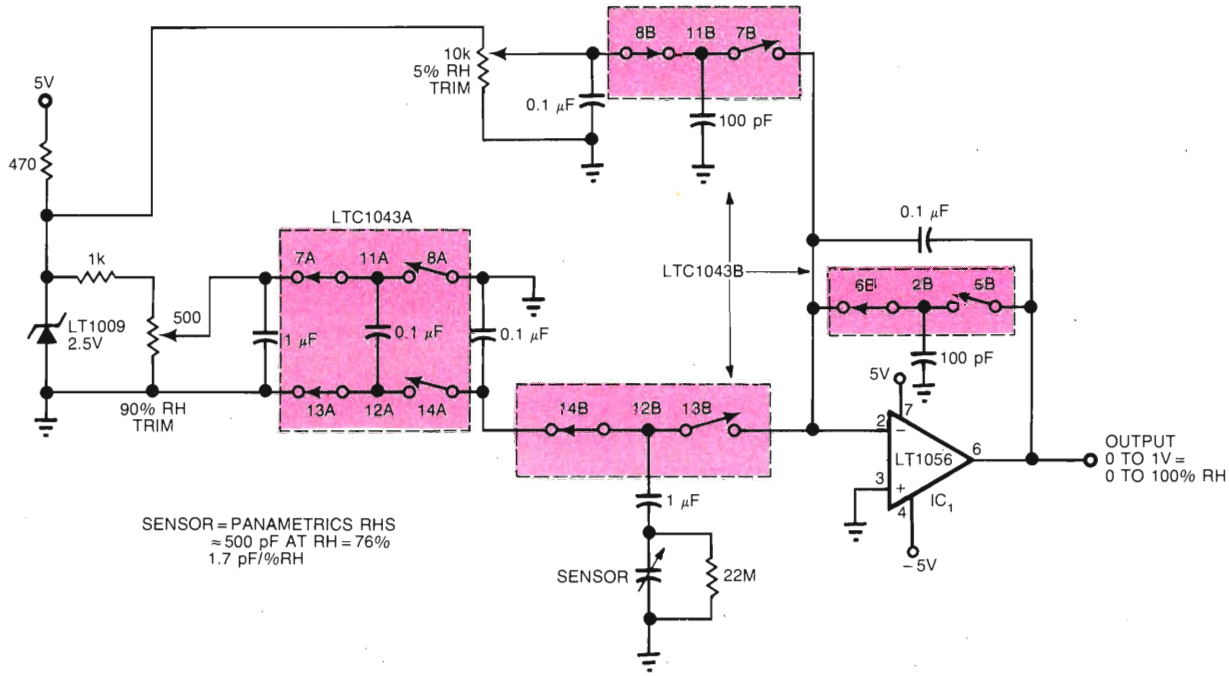


Fig 8—This circuit provides signal conditioning for a relative-humidity transducer, *a function that is usually difficult to realize. The circuit is accurate to within ±2% in the 5 to 90% humidity range.*

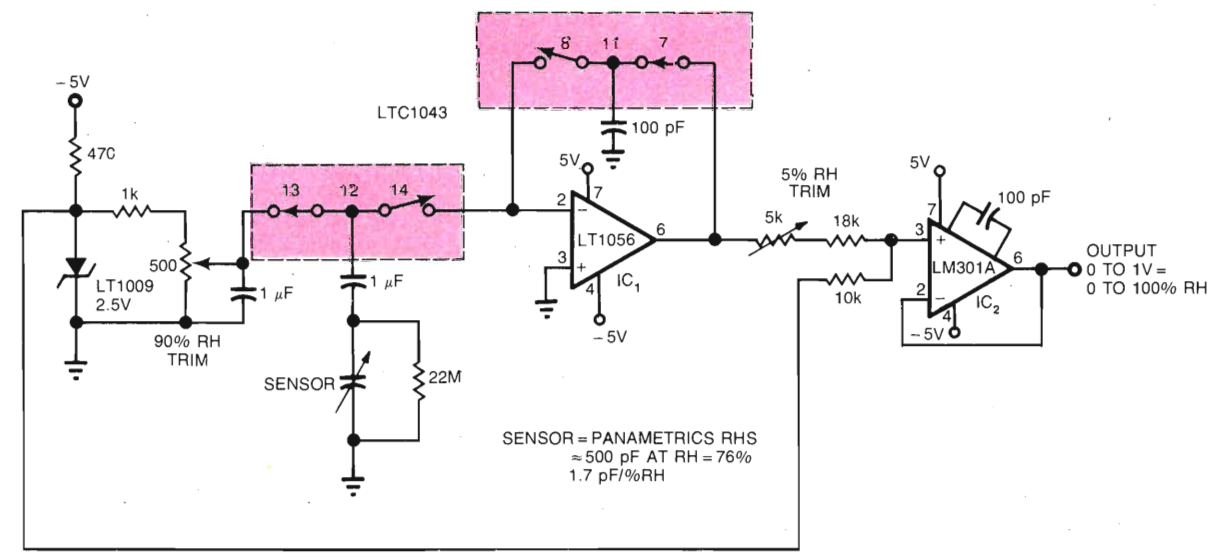
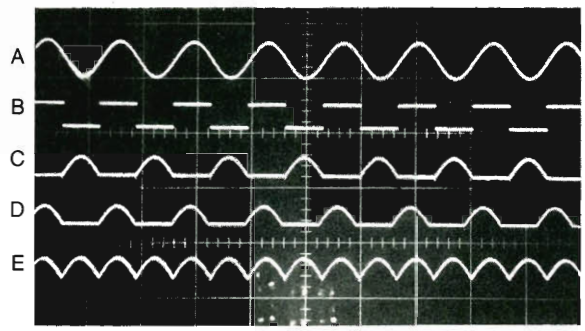


Fig 9—An alternative to Fig 8's circuit, *this configuration uses two op amps and one CMOS-switch IC. The circuit is insensitive to clock frequency; you trim its dc offset by injecting a current into IC_2's summing junction.*

three points are fixed. Total error over the entire range is now within ±0.05°C.

The resistance values given are for a nominal 100.00Ω (0°C) sensor. You can use sensors that differ from this nominal value by factoring in the deviation from the 100.00Ω value. This deviation, specified by the RTD manufacturer for each sensor, is an offset term that accrues from the winding tolerances during the RTD's fabrication. The platinum element's gain slope—a very small error term—is primarily fixed by the purity of the material. Note that IC_1 constitutes a voltage-controlled current source with both input and output referred to ground—this is usually a difficult function to realize.



TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	500 μSEC/DIV
B	10V/DIV	500 μSEC/DIV
C	0.2V/DIV	500 μSEC/DIV
D	0.2V/DIV	500 μSEC/DIV
E	0.2V/DIV	500 μSEC/DIV

Fig 11—Waveforms for Fig 10's LVDT-conditioning circuit *show the stabilized sine wave (trace A) applied to the transformer's primary. Summing the half-wave-rectified secondary outputs seen in traces C and D results in the output (trace E).*

Conditioning an RH sensor

Moving from temperature to relative humidity, note that the latter is a difficult parameter to transduce and that most available transducers require fairly complex signal-conditioning circuitry. The circuit in **Fig 8** combines two LTC1043s with a recently introduced, capacitance-based humidity transducer in a simple charge-pump circuit.

The specified sensor has a nominal 500-pF capacitance at RH=76%, and a transfer-function slope of 1.7 pF/%RH. The average voltage across the device must be 0V; this provision prevents deleterious electrochemical migration in the sensor. LTC1043A inverts a resistively scaled portion of the LT1009-produced reference voltage, thereby generating a negative potential at pin 14A. LTC1043B alternately charges and discharges the humidity sensor via pins 12B, 13B and 14B.

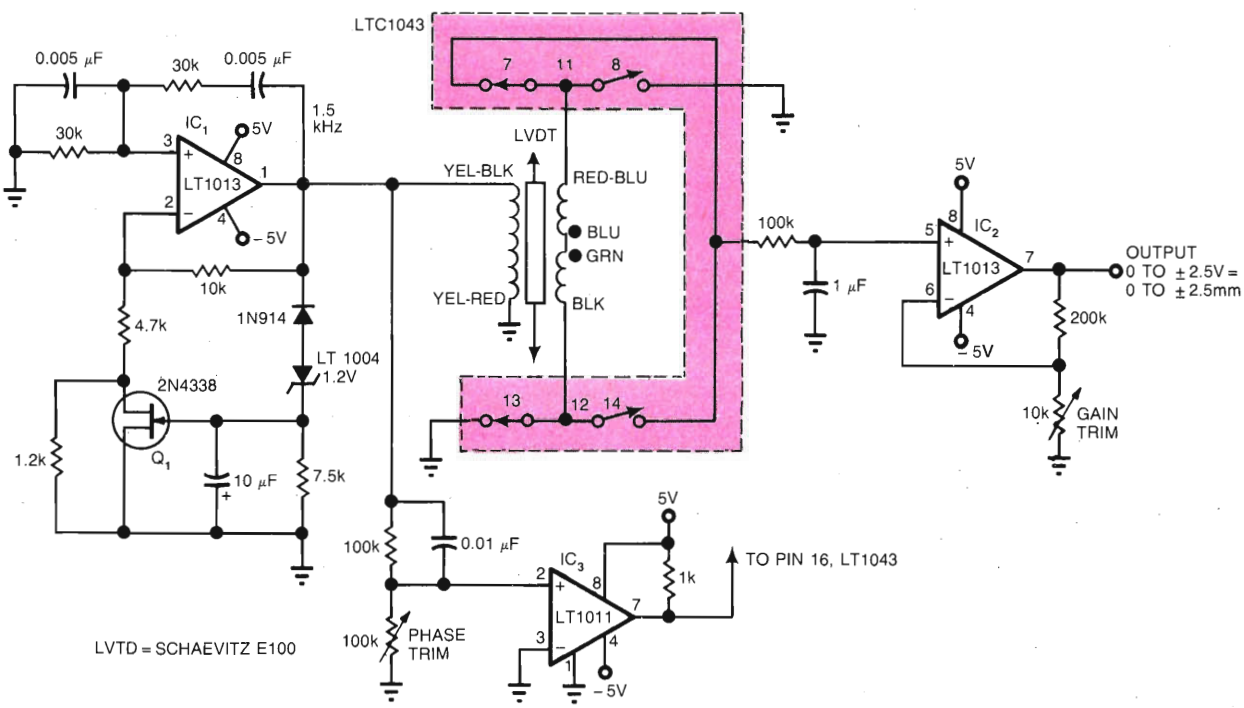


Fig 10—This position-sensing circuit *uses an LVDT to detect the displacement of the transformer's core from magnetic center. The circuit produces ±2.5V output for displacements of ±2.5 mm.*

Lock-in amplifier extracts buried signals

With pins 14B and 12B connected, the sensor charges (via the 1-μF capacitor) to the negative potential at pin 14A. When the 14B-12B connection opens, 12B connects to IC_1's summing point through the 1-μF capacitor. Because the charge voltage is fixed, the average current into the summing point is determined by the sensor's humidity-related value. The capacitor ac couples the sensor to the charge/discharge path, maintaining the required 0V average voltage across the device.

The 22-MΩ resistor prevents charge accumulation that would stop current flow. The average current into IC_1's summing junction is balanced by packets of charge delivered by the switched-capacitor network in IC_1's feedback loop. The 0.1-μF capacitor imparts an integrator-like response to IC_1; the amplifier thus yields a dc output. To make 0% RH correspond to 0V, it's necessary to introduce offsetting.

The signal and feedback terms biasing the summing point are expressed in charge form, so the offsetting signal delivered to the summing junction must also be in the form of charge, instead of a simple dc current. Failing this, frequency drift of the LTC1043B's oscillator will affect the circuit. Switch section 8B-11B-7B serves this charge-dispensing function, delivering the LT1009-referenced offsetting charge to IC_1.

Drift contributors in this circuit include the LT1009 and the ratio stabilities of the sensor and the 100-pF capacitors. These terms are well within the sensor's 2%-accuracy specification; therefore, temperature compensation is unnecessary. To calibrate the circuit, place

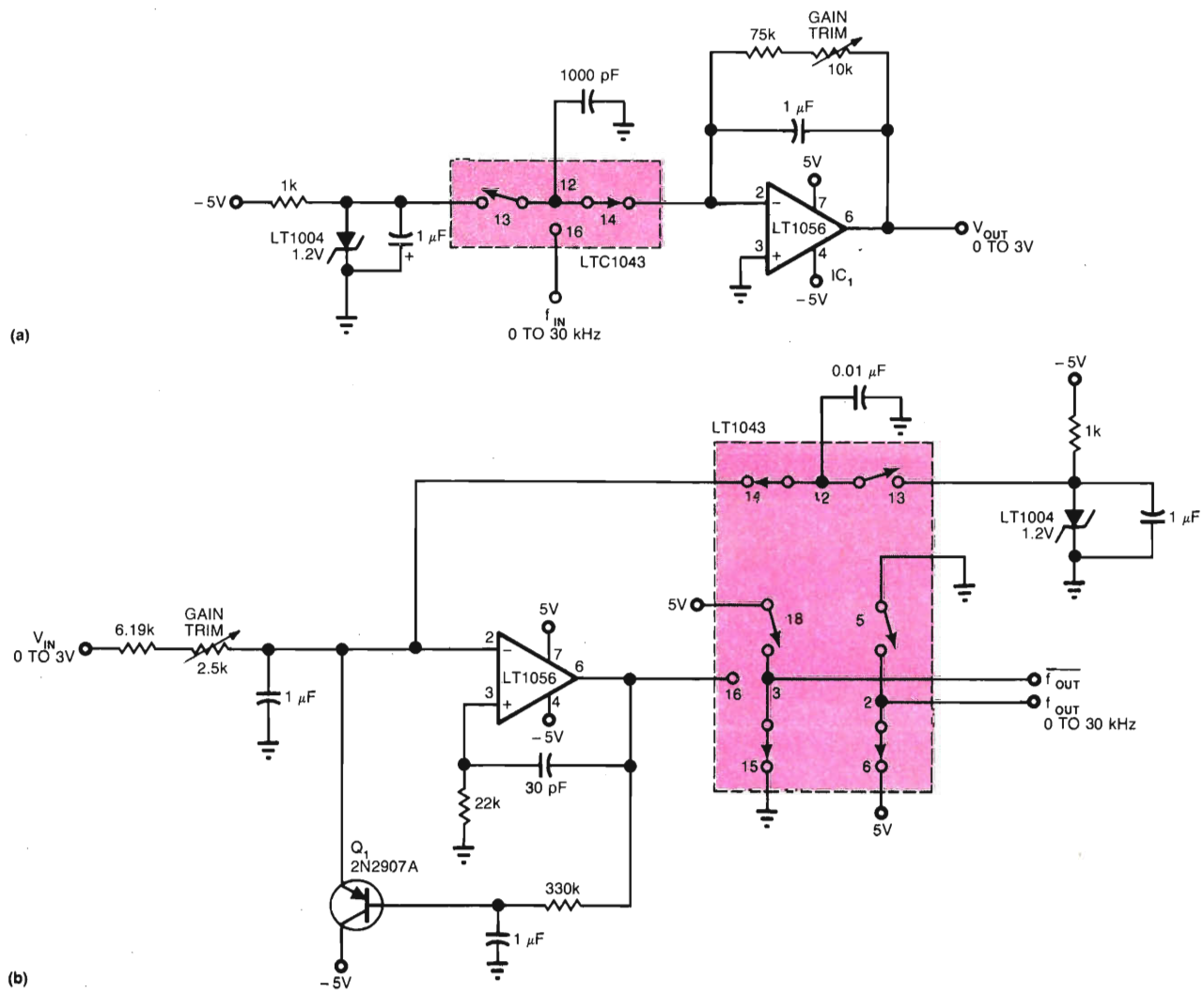


Fig 12—Simplifications of classic F/V and V/F converters, *these circuits feature low component count and 0.005% linearity. The F/V* ***(a)*** *and V/F* ***(b)*** *circuits are mirror images of each other; in the latter, the switched-capacitor network appears in the op amp's feedback network.*

the sensor in a known 5%-RH environment and adjust the potentiometer labeled "5%-RH trim" for 0.05V output. Next, place the sensor in a 90%-RH environment and set the "90%-RH trim" for 900-mV output.

Reiterate the procedure until both points are fixed. Once calibrated, this circuit is accurate within 2% in the 5 to 90% relative-humidity range. **Fig 9** shows an alternate circuit, requiring two op amps but only one LTC1043. This circuit maintains insensitivity to the clock frequency while permitting a dc-offset trim. You can effect the trim by summing in the offset current after IC_1.

Switch out LVDT errors

Another transducer that's eligible for signal conditioning by switching techniques is the linear variable differential transformer (LVDT). This device is a transformer with a mechanically actuated core. A sine wave (usually amplitude stabilized) drives the primary; sinusoidal drive eliminates error-inducing harmonics in the transformer. The two secondaries are connected in opposing phase. When the core is in the transformer's magnetic center, the secondary outputs cancel, producing net zero output. Moving the core away from center position unbalances the flux ratio between the secondaries, resulting in a voltage output.

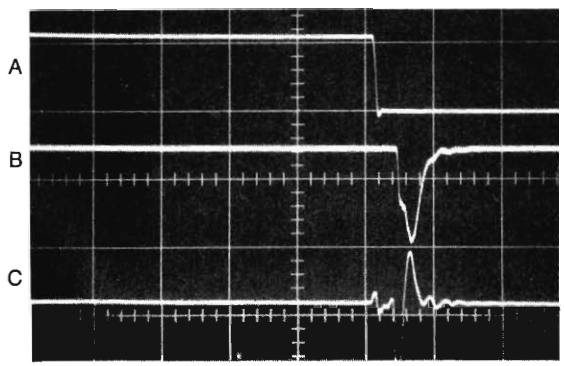
Fig 10 shows an LTC1043-based LVDT signal conditioner. IC_1 and its associated components supply the amplitude-stabilized, sine-wave source. The op amp's positive-feedback path constitutes a Wein bridge, tuned for 1.5 kHz. Q_1, the LT1004 reference and some additional components in IC_1's negative-feedback loop stabilize the amplifier at unity gain.

IC_1's output (**Fig 11,** trace A), an amplitude-stabilized sine wave, drives the LVDT. IC_3 detects zero crossings and drives the LTC1043's clock pin (trace B). A speed-up network at IC_3's input compensates for LVDT phase shift, synchronizing the LTC1043's clock to the transformer output's zero crossings. The LTC1043 alternately connects each end of the transformer to ground, resulting in positive half-wave rectification at pins 7 and 14 (traces C and D). These points are summed (trace E) in a lowpass filter at IC_2's input; this op amp supplies gain scaling at the circuit's output.

The synchronized clocking of the LTC1043 causes the information presented to the lowpass filter to be amplitude and phase sensitive. The circuit output indicates how far the core is from center, and on which side. To calibrate the circuit, center the LVDT's core in the transformer and adjust the phase trim for 0V output. Next, move the core to either extreme position and set the gain trim for the desired 2.50V full-scale output.

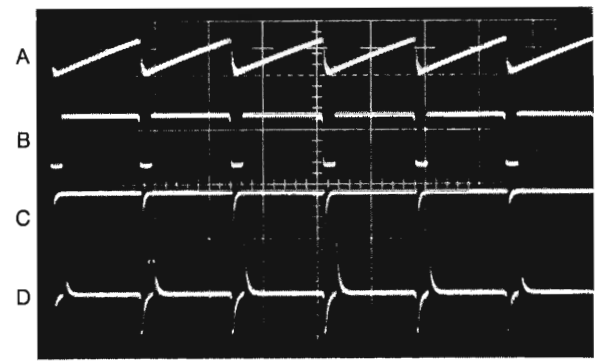
Convert F to V and V to F

As additional examples of how a CMOS-switch IC can simplify precision circuit functions, consider the two related circuits of **Fig 12.** These circuits equal the performance of charge-pump frequency-to-voltage



TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	50 nSEC/DIV
B	5 mA/DIV	50 nSEC/DIV
C	0.5V/DIV (AC COUPLED)	50 nSEC/DIV

Fig 13—The F/V converter of Fig 12a *produces these waveforms. The 1000-pF capacitor removes current from IC_1's summing node (trace B), forcing the op amp's output to swing negative (trace C). The amplifier recovers and resets its summing node to zero.*



TRACE	VERTICAL	HORIZONTAL
A	20 mV/DIV	20 μSEC/DIV
B	10V/DIV	20 μSEC/DIV
C	20 mA/DIV	20 μSEC/DIV
D	5V/DIV	20 μSEC/DIV

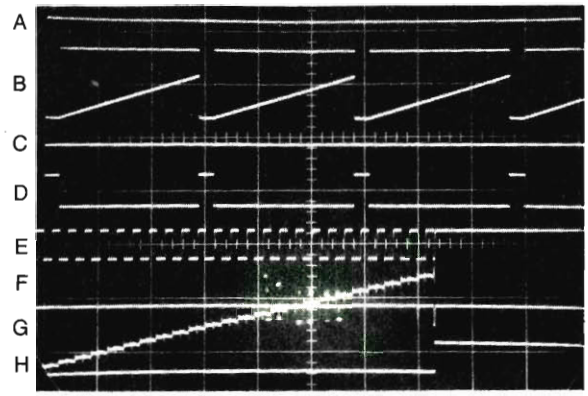
Fig 14—These waveforms show voltage and current relationships *in the V/F converter in* ***Fig 12b.*** *The circuit works by reversing an LTC1043's switch states, causing current to flow from the op amp's summing node into a 0.01-μF capacitor (trace C).*

Switched-capacitor circuits make signal conditioning easy

(F/V) and voltage-to-frequency (V/F) converters, respectively, but don't require the compensation the earlier circuits need for nonideal charge-gating behavior. The circuits are economical and have low component count, and their 0.005% transfer-function linearity equals that of more complex designs.

In the F/V converter (**a**), the input (**Fig 13,** trace A) drives the LTC1043's clock pin. With the input high, pins 12 and 13 are shorted and pin 14 is open. The 1000-pF capacitor receives charge from the 1-μF unit, which is biased by the LT1004. At the input's negative-going edge, the 12-13 switch opens and 12-14 closes. The 1000-pF capacitor quickly removes current (trace B) from IC_1's summing node. Initially, current transfer occurs through IC_1's feedback capacitor, and the amplifier's output swings negative (trace C).

When IC_1 recovers, it slews in a positive sense to a level that resets the summing junction to zero. IC_1's 1-μF feedback capacitor averages this action over many cycles; the circuit's output is, therefore, a dc level linearly related to frequency. IC_1's feedback resistors set the circuit's dc gain. To trim the circuit, apply a



TRACE	VERTICAL	HORIZONTAL
A	20V/DIV	500 μSEC/DIV
B	0.2V/DIV	500 μSEC/DIV
C	20V/DIV	500 μSEC/DIV
D	20V/DIV	500 μSEC/DIV
E	20V/DIV	20 μSEC/DIV
F	0.1V/DIV	20 μSEC/DIV
G	20V/DIV	20 μSEC/DIV
H	20V/DIV	20 μSEC/DIV

Fig 16—The A/D conversion in Fig 15's circuit *is seen in these waveforms. Note the staircase in trace F, which clearly indicates the charge-pumping action at the input op amp's summing junction.*

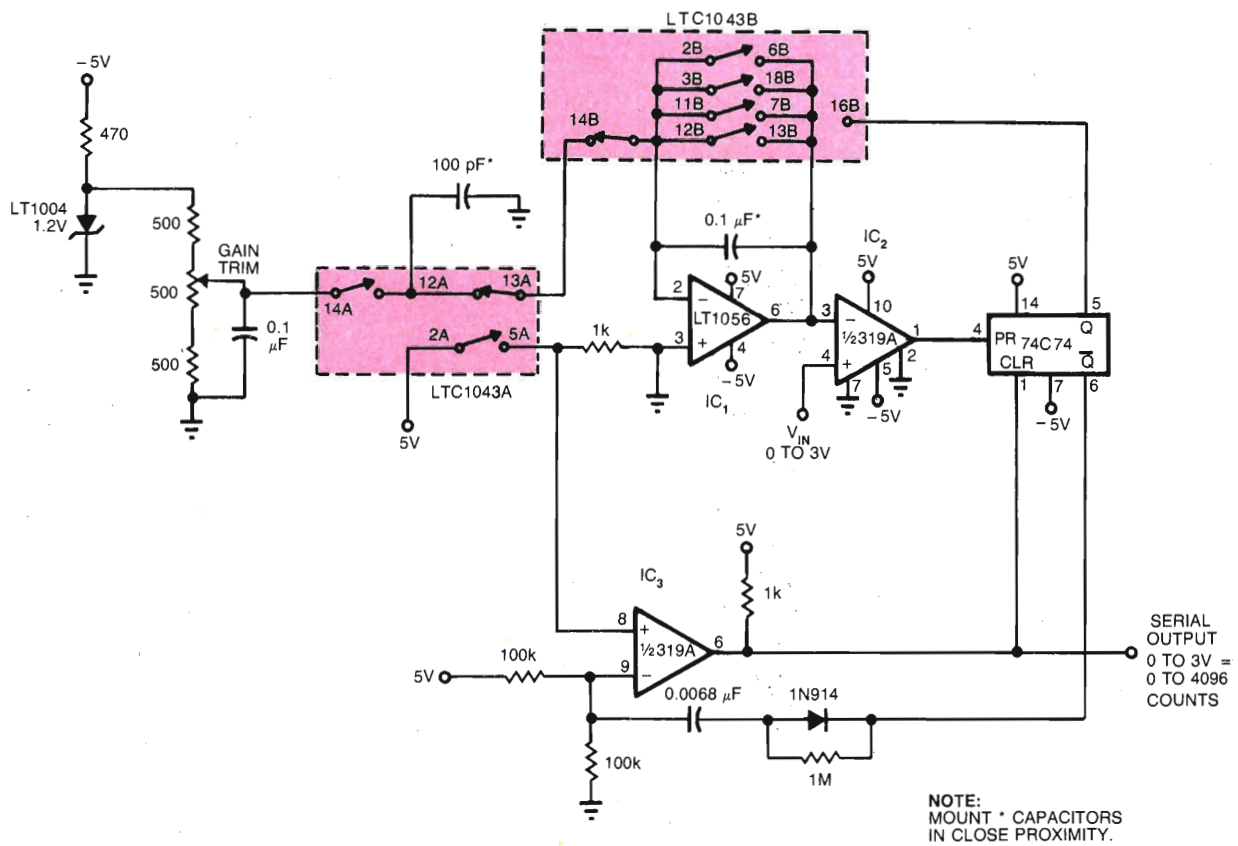


Fig 15—This inexpensive 12-bit A/D converter *is an integrating type. The number of pulses between resets represents the binary equivalent of the analog input. The self-clocking circuit converts a full-scale input in 25 msec.*

30-kHz input and set the 10-kΩ gain-trim potentiometer for exactly 3V output.

The primary drift contributor in this circuit is the −120-ppm/°C temperature coefficient of the 1000-pF capacitor (preferably a polystyrene unit). You can reduce this term to less than 20 ppm/°C by using a feedback resistor with an opposing temperature coefficient (eg, a TRW MTR-5/+120 ppm). You must hold the input pulse low for at least 100 nsec in order to allow complete discharge of the 1000-pF capacitor.

In the circuit in **Fig 12b,** the LTC1043-based charge pump is in IC_1's feedback loop, resulting in a V/F converter. IC_1's output drives the clock pin. Assume that IC_1's inverting input is just below 0V; the op amp's output is therefore positive. Under these conditions, the LTC1043's pins 12 and 13 are shorted and pin 14 is open, allowing the 0.01-μF capacitor to charge toward the −1.2V LTC1004. When the input-voltage-derived current forces IC_1's summing point positive (**Fig 14,** trace A), the amp's output swings negative (trace B).

This transition reverses the LTC1043's switch states, connecting pins 12 and 14. Current flows from the summing point into the 0.01-μF capacitor (trace C). The 30-pF, 22-kΩ combination at IC_1's noninverting input (trace D) ensures that IC_1's output remains low long enough for the 0.01-μF capacitor to reset to zero. When this RC positive-feedback path decays, the op amp's output returns to a positive level and the entire cycle repeats. The oscillating frequency of this arrangement is directly related to the input voltage, with 0.005% transfer-function linearity.

Start-up or overdrive conditions could force IC_1's output to go to the negative rail and stay there. Q_1 prevents this condition by pulling the summing point negative if the op amp's output stays low long enough to charge the 1-μF, 330-kΩ network. Two LTC1043 switch sections provide complementary sink/source outputs. As in the F/V converter, the 0.01-μF contributes the primary drift term; the resistor type noted earlier provides optimum temperature-coefficient cancellation. To calibrate this circuit, apply 3V to the input and adjust the gain-trim potentiometer for 30-kHz output.

A/D converter offers simplicity

As a final example of the utility of a CMOS-switch IC, consider the use of the IC in an economical, counter-type A/D converter. The circuit (**Fig 15**) is self clocking, has a serial output and completes a full-scale conversion in 25 msec. The design uses two LTC1043s. Unit A is free running, alternately charging the 100-pF capacitor from the LT1004 reference source, then dumping it into IC_1's summing junction. IC_1, connected as an integrator, responds with a linear-ramp output (**Fig 16,** trace B).

IC_2 compares the ramp with the input voltage. When the crossing occurs, IC_2's output switches low (trace C), setting the flip flop's Q output to logic One (trace D). This action pulls pin 16B high, resetting IC_1's integrator capacitor via the paralleled switches. Simultaneously, pin 14B opens, preventing the delivery of charge to IC_1's summing point during the reset.

The flip flop's $\overline{Q}$ output, at logic Zero during this interval, produces an ac-coupled, negative-going pulse at IC_3's inverting input. This spike forces IC_3's output high, inserting a gap in the output clock-pulse stream (trace A). The width of this gap, set by the components at IC_3's inverting input, is sufficiently great to allow a complete reset of IC_1's integrating capacitor. The number of pulses between gaps is directly related to the input voltage.

The actual conversion begins at the gap's negative-going edge and ends at its positive-going edge. The flip flop can serve a reset function. Alternatively, a processor-driven time-out routine can determine the end of conversion. Traces E through H offer expanded-scale versions of traces A through D. The staircase detail of IC_1's ramp output reflects the charge-pumping action at the op amp's summing point.

Note that the drift in the 100-pF and 0.1-μF capacitors (again, preferably polystyrene) cancels ratiometrically. Full-scale drift for this circuit is typically 20 ppm/°C, allowing it to hold 12-bit accuracy over 25°C±10°C. To calibrate the circuit, apply 3V input and trim the gain potentiometer for 4096 output pulses between data-stream gaps. EDN

Author's biography

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and -instrumentation design. He has served in related capacities at National Semiconductor Corp, Arthur D Little Inc and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art and collecting antique scientific instruments.

Use low-power design methods to condition battery outputs

By applying some simple battery-regulator design techniques, you can condition battery voltages without consuming the large amounts of power typical in regulator circuitry.

Jim Williams, *Linear Technology Corp*

Most IC regulators are not suitable as battery regulators because they either draw too much quiescent current or can't operate at low input voltages, or both. For example, some switching regulators consume 20 mA—far more current than low-power systems draw. This article contains a variety of circuit-design ideas for conditioning power without draining your batteries unnecessarily.

When you design battery regulators, you must consider efficiency, power output, battery life, circuit complexity, pc-board space and cost. You can apply various linear and switching regulation techniques, depending on your specific requirements. General classes of regulators include voltage inverters, step-down circuits and step-up converters. Usually, you will use dc exclusively, but sometimes you will need ac. So you should understand how to design for both.

Generate negative and positive voltages

You will often have to generate a negative voltage. **Fig 1a** shows a simple way to do this. The LTC1044 switched-capacitor voltage converter's internal switches transfer charge sequentially from C_1 to C_2, the output capacitor. When SW_1 is closed, C_1 charges to 9V. When SW_1 opens, SW_2 closes, charging C_2 and giving it a negative potential with respect to ground. Continuous clocking keeps V_{OUT} at dc.

Because of the chip's finite output impedance, loading its output causes a voltage drop. **Fig 1b** plots output voltage versus load current. In low-current applications or in applications where regulation isn't critical, the circuit in **Fig 1a** proves adequate. If you need to improve the regulation, you must decrease the circuit's output impedance. **Fig 1c** puts the LTC1044 in a feedback loop with an LM10's op amps (the remaining section serves as a reference-voltage source). Because the LTC1044 is a voltage inverter, the loop closes at the op amp's positive input. Consequently, increased drive from the LM10 compensates for the voltage converter's droop under load.

The 0.1-μF capacitor stabilizes the loop. Because the LM10's output impedance rises with frequency, you need the 47-μF capacitor on the chip's output to isolate it from the high-frequency input pulses of the LTC1044. The LM10's output-swing restrictions limit circuit output to 8.5V. You can see in **Fig 1b** the improvement in

CMOS voltage converter regulates efficiently

the output regulation over the basic circuit in **Fig 1a**.

You will often need to get positive and negative supplies from a single battery. If your current requirements are small, the circuit shown in **Fig 2a** is a simple solution. It provides symmetrical positive and negative output voltages, each equal to half the input voltage. The output voltages get referenced to pin 3 (output common). If the input voltage between pin 8 and pin 5 exceeds 6V, you should also connect pin 6 to pin 3, as shown by the dashed line.

The LT1010 buffer handles higher currents. **Fig 2b** shows a splitter circuit that can source or sink as much as ±150 mA with only 5-mA quiescent current. You can make the output capacitor as large as is necessary to absorb current transients. An input capacitor across the battery prevents the high frequency instability that a high source impedance can cause.

Regulators have low dropout rate

Switching regulators aren't the only type that suit battery power. Linear regulators for batteries provide both low noise and fast transient response. To maximize battery life, you will want a very low regulator-dropout voltage. You could do this with pnp pass elements, but

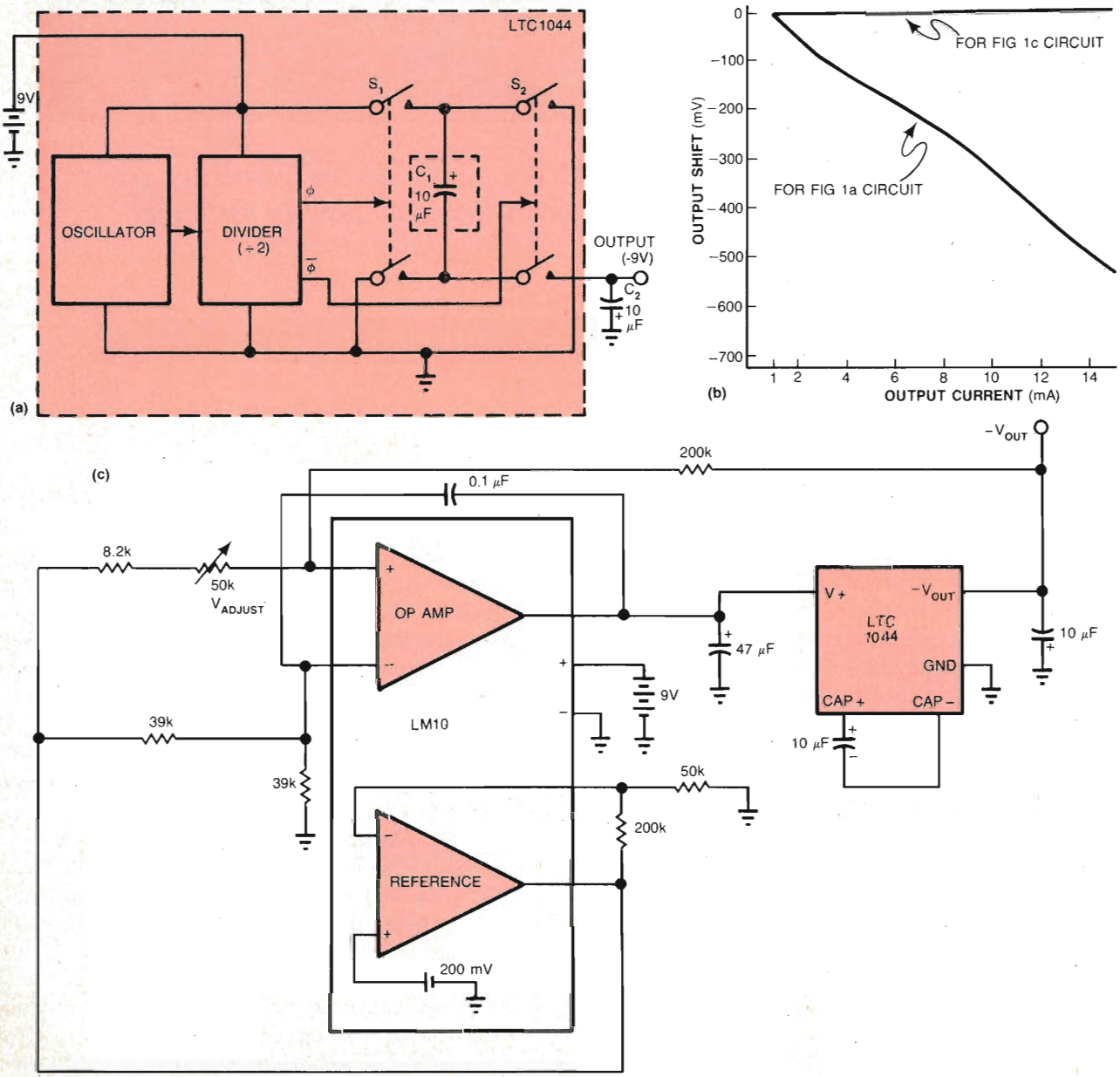


Fig 1—To generate a negative voltage, *you can use the circuit in* **(a),** *which includes the block diagram of an LTC1044;* **(b)** *plots the voltage-deviation/load-current characteristics of* **(a)** *and of an improved version that includes an op amp, shown in* **(c).**

their base current never arrives at the load, which decreases efficiency. The pnp's voltage gain also complicates loop dynamics, often leading to a relatively poor transient response.

The circuit illustrated in **Fig 3a** offers low dropout and the fast transient response of an npn pass element. Normally, npn pass-based regulators have high dropout voltages because of voltage drops in the emitter-follower connected pass transistor. This design drives the npn pass base from a 12V source generated by the LTC1044 voltage converter from the circuit's 6V-input. The transistor operates as a voltage-overdriven emitter follower. Only $V_{CE(SAT)}$ limits the emitter's ability to follow the collector. The voltage-overdriven base re-

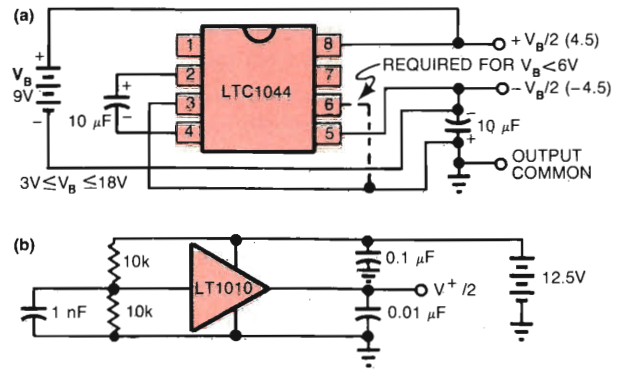


Fig 2—The switched-capacitor voltage-converter design ***(a)*** *and the high-current power-buffer circuit* ***(b)*** *produce positive and negative voltages, with low quiescent currents.*

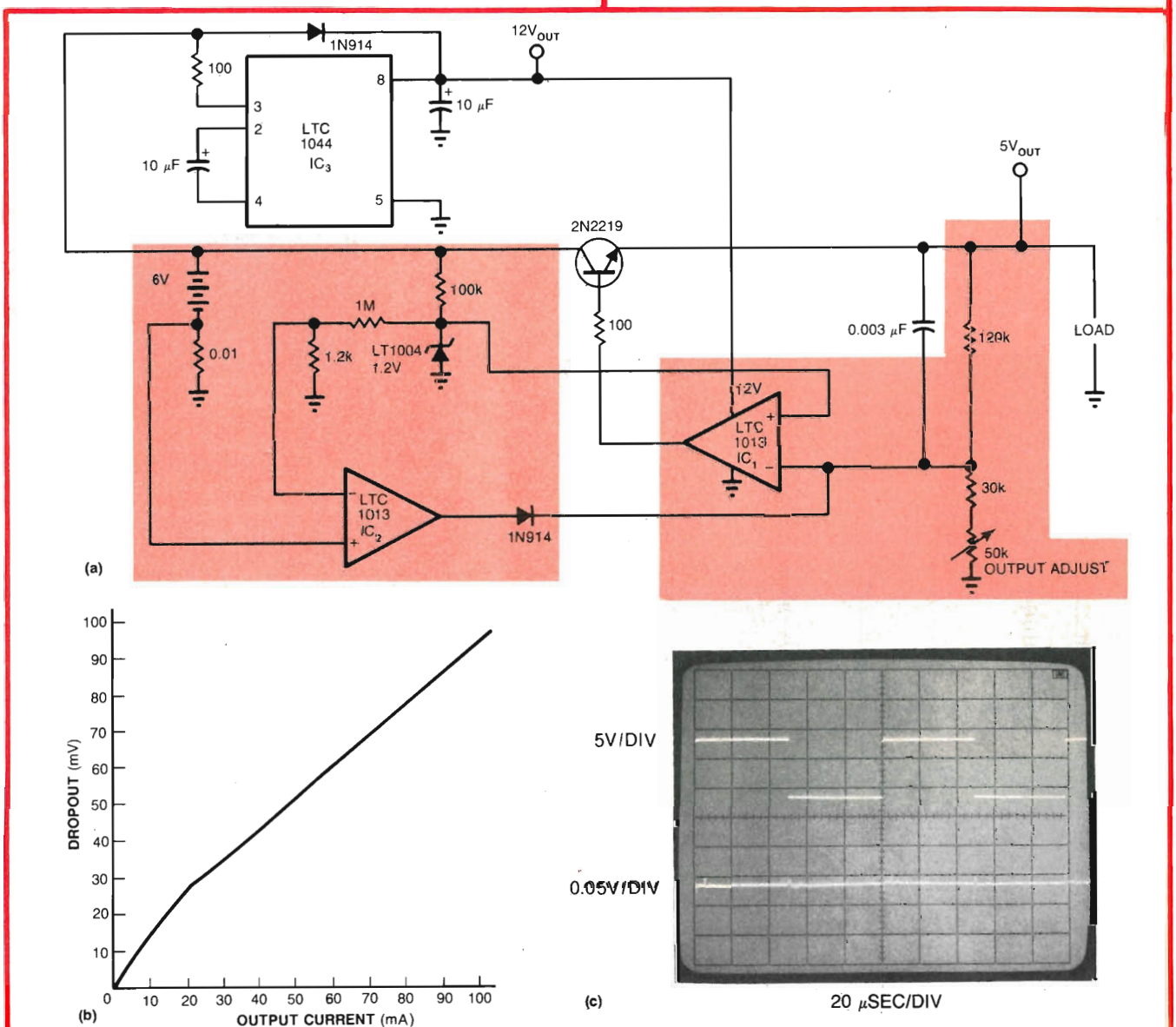


Fig 3—An npn pass transistor *gives the circuit in* ***(a)*** *low dropout, as plotted in* ***(b),*** *and fast transient response, as shown in the scope photos* ***(c).*** *The quiescent current is held down to 760 μA, and the output capacity is 100 mA.*

Regulator minimizes dropout voltage

moves the V_{BE} drop, normally the dominant loss, as a consideration. The LTC1044 that doubles the battery voltage powers the LT1013 dual op amp. The circuit's quiescent current is 760 μA and its 100-mA-capacity output is short-circuit protected.

IC_1, with 12V-output capability, provides the feedback that controls the 6V collector-biased transistor. The 100Ω resistor prevents parasitic high frequency oscillation and the LT1004 is a voltage reference. Varying IC_1's feedback divider trims the output, and the 0.003-μF capacitor compensates the loop. IC_2 provides short-circuit protection by forcing IC_1's output low if battery current exceeds 150 mA. IC_2's low offset and high open-loop gain allow it to use the very small 0.01Ω current sense resistor, reducing voltage-drop losses. At 100-mA output, the shunt has only 1 mV across it.

Fig 3b illustrates dropout data for the regulator. For a 10-mA load, dropout is only 0.016V, with 0.094V occurring at 100-mA loading. **Fig 3c** shows the circuit's transient response. The top trace shows a variable load on the output, which is either zero or 100 mA. The bottom trace is the regulator's output (ac coupled). Transient response is clean and quick, with little tailing or aberration.

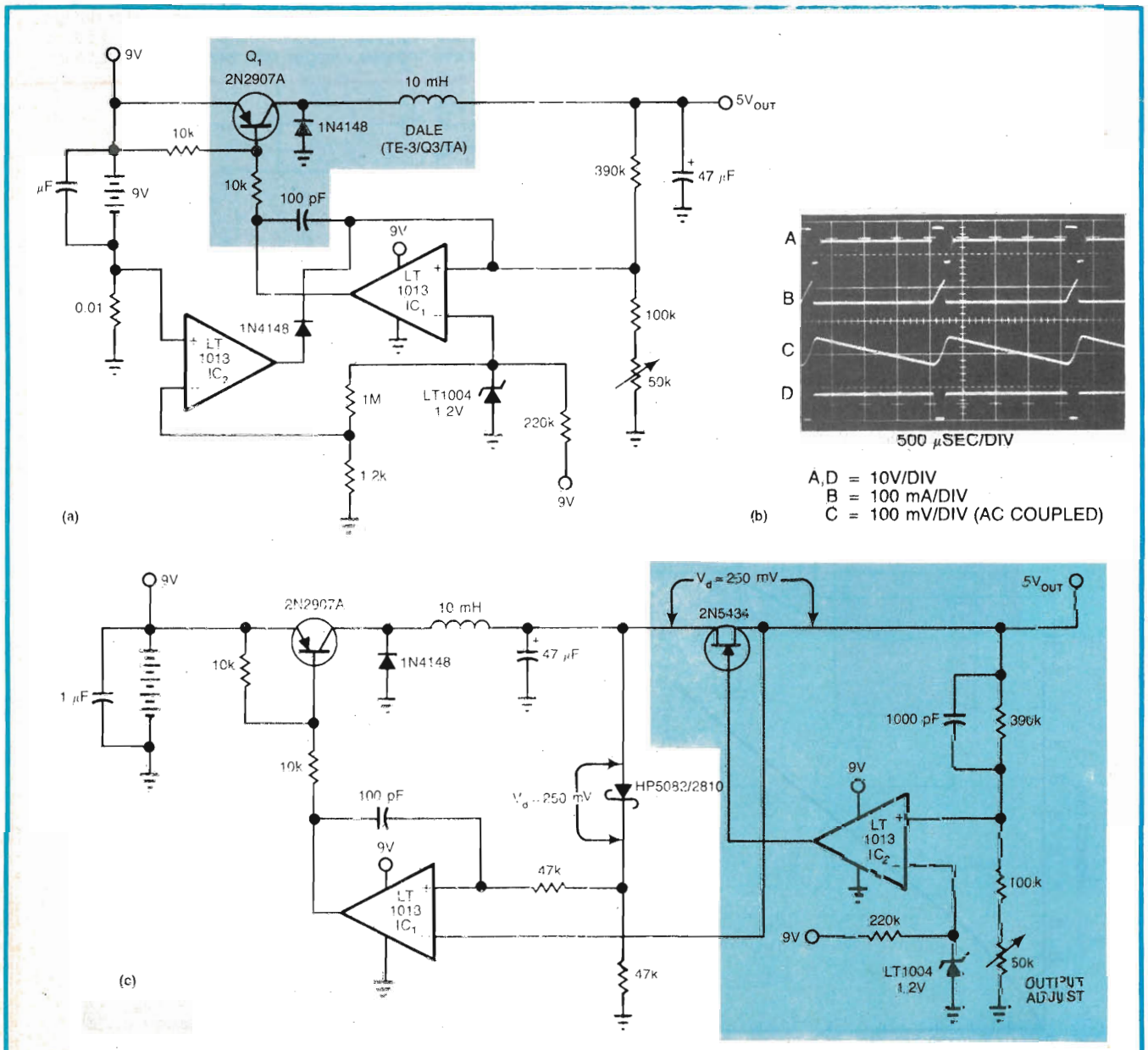


Fig 4—If the voltage drop between the input and the output *of the regulator is sizable, using* ***(a)*** *keeps efficiency at 80% with 50-mA output capability. The switching in* ***(b)*** *is clean, but this switching can still cause excessive noise. The design in* ***(c)*** *eliminates the noise problem.*

The low-dropout linear regulator is efficient only when its input and output voltages are close. Situations requiring substantial voltage drop to achieve the desired regulated output need switching techniques to maintain good efficiency. **Fig 4a** shows a simple battery-powered switching regulator. It supplies 5V from a 9V source with 80% efficiency and 50-mA output.

To understand the circuit's operation, assume that the transistor, Q_1 in **Fig 4a,** is on. Its collector's (top trace, **Fig 4b**) voltage rises, forcing current (second trace) through the inductor. The output voltage (third trace) rises, causing IC_1's output to rise. Q_1 cuts off and the stored energy in the inductor discharges through the load (the 1N4148 is a flyback diode). The 100-pF capacitor ensures clean switching. The cycle repeats when the output drops low enough for IC_1 to turn on Q_1. The 1-μF capacitor ensures low battery impedance at high frequencies, preventing sag during switching. Short-circuit protection is the same as that in **Fig 3a**'s circuit.

In some applications, the switching noise on the regulated output may be troublesome. **Fig 4c** eliminates the noise by adding a low-dropout series regulator at the switching circuit's output. The operation of the switching loop is similar to that in **Fig 4a**, except that in **Fig 4c** the loop also controls the voltage across the 2N5434 FET series-pass element. The switching loop forces the voltage across the FET to equal the voltage across the Schottky diode (V_d=250 mV), regardless of input or loading conditions. The FET, a low-$R_{DS(ON)}$, low pinch-off unit, combines with IC_2 to form a simple, low-dropout series-pass regulator. The LT1004 is the reference, and the 1000-pF capacitor provides roll-off. This circuit will supply 25 mA of noise-free, regulated power with short-circuit current set by the FET's 30-mA I_{DSS}. The overall 75% efficiency of **Fig 4c**'s circuit is not as good as that of the basic switching circuit in **Fig 4a** because of the 6 mW (0.250V×0.025A) dissipated in the FET.

Fig 5a shows another high-efficiency battery-driven

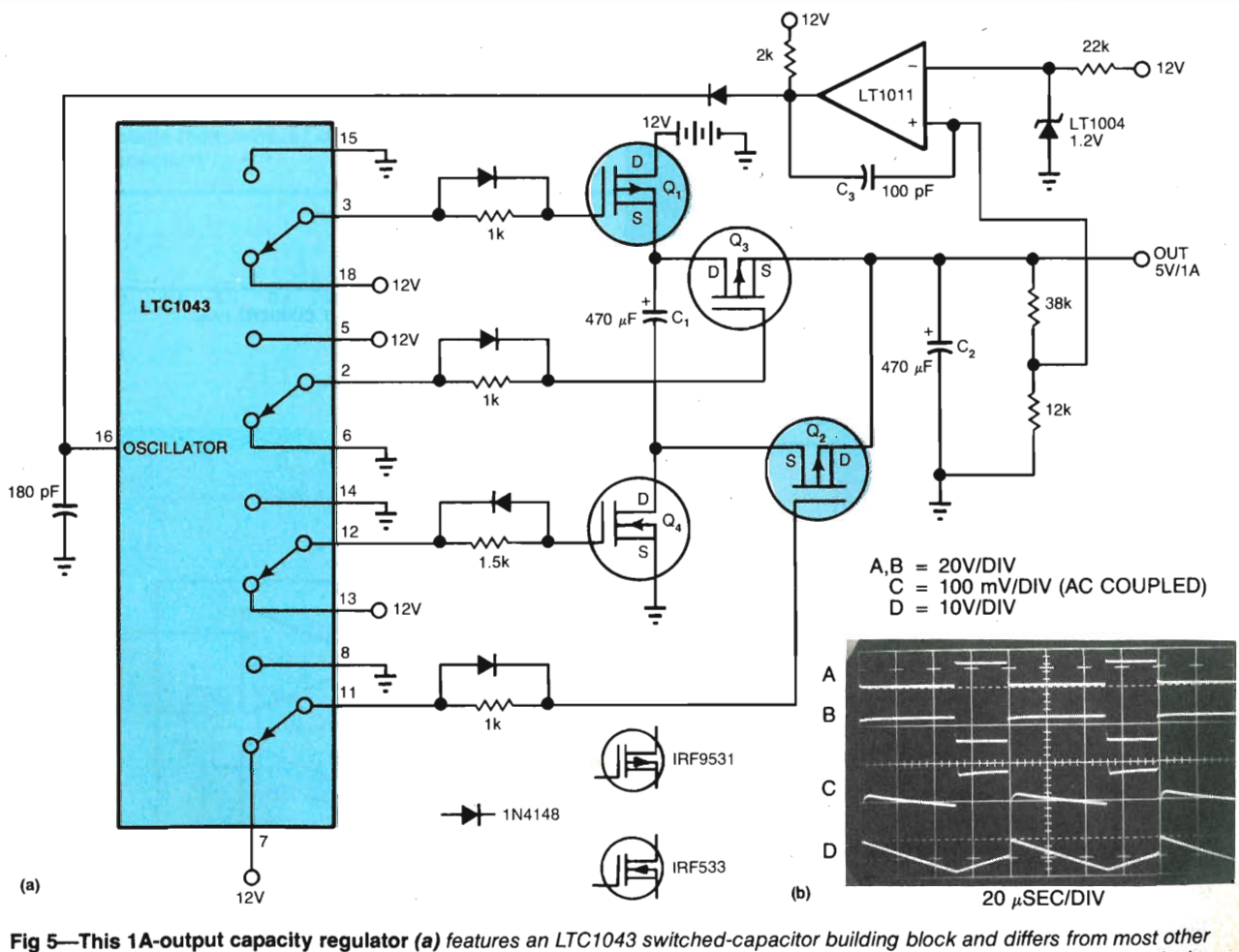


Fig 5—This 1A-output capacity regulator ***(a)*** *features an LTC1043 switched-capacitor building block and differs from most other high-current designs in that it doesn't require an inductor. The top two traces* **(b)** *display transistor drives, and the third trace is the output voltage.*

Switching circuit conserves power

regulator that puts out 1A. It does not require an inductor—an unusual feature for a switching regulator operating at this current level.

The LTC1043 switched-capacitor building block provides nonoverlapping complementary drive to the Q_1 to Q_2 power MOSFETS. The MOSFETS alternately place C_1 and C_2 first in series and then in parallel. During the series phase, the 12V battery charges both capacitors and furnishes load current. During the parallel phase, both capacitors deliver current to the load.

The top and second traces (**Fig 5b**) are the LTC1043-supplied drives to Q_3 and Q_4, respectively. (Q_1 and Q_2 receive similar drive from pins 3 and 11.) The diode-resistor networks enhance the nonoverlapping drive, preventing simultaneous drive to the series/parallel-phase switches. Normally, the output would be one-half of the supply voltage, but C_1 and its associated components close a feedback loop, forcing the output to 5V. With the circuit in the series phase, the output (third trace) heads rapidly in the positive direction. When the output exceeds 5V, the comparator-configured op amp trips, forcing the LTC1043 oscillator pin (bottom trace) high. This truncates the LTC1043's triangle-wave oscillator cycle.

Disabling the oscillator forces the circuit into the parallel phase, and the output coasts down slowly until the next LTC1043 clock cycle begins. The comparator's output diode prevents the triangle down-slope from being affected and the 100-pF capacitor provides sharp transitions. The loop regulates the output to 5V by controlling (with feedback) the turn-off point of the series phase. The circuit constitutes a large-scale

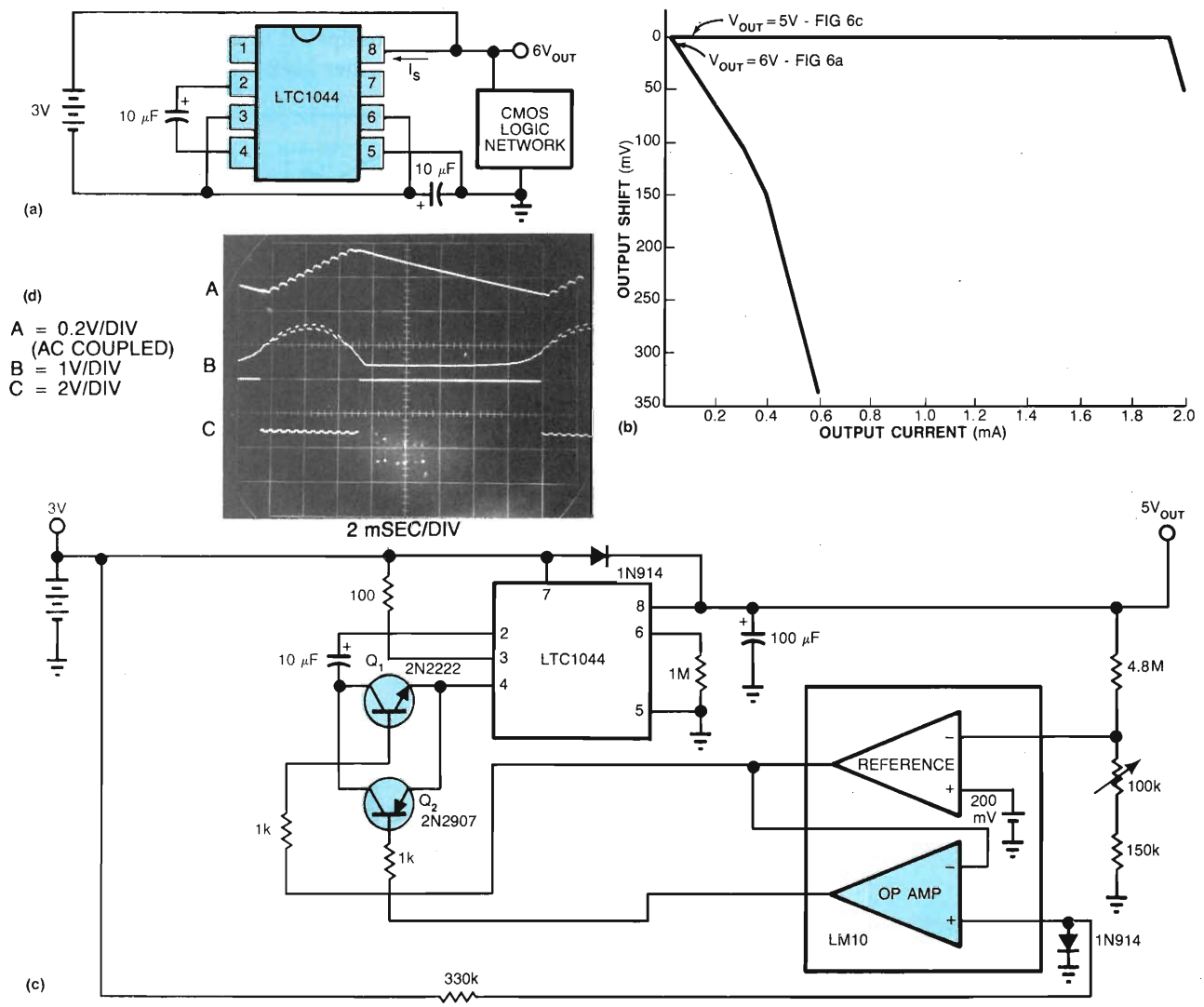


Fig 6—This simple application of the LTC1044 voltage converter ***(a)*** *produces an output voltage of twice the input voltage. As the load current increases, the voltage output falls off* ***(b)****—a problem that the op-amp design in* ***(c)*** *solves. If the output voltage declines (top trace* ***(d)****), the amp (bottom trace) goes negative, turning on the switching transistors and bringing the output voltage back up.*

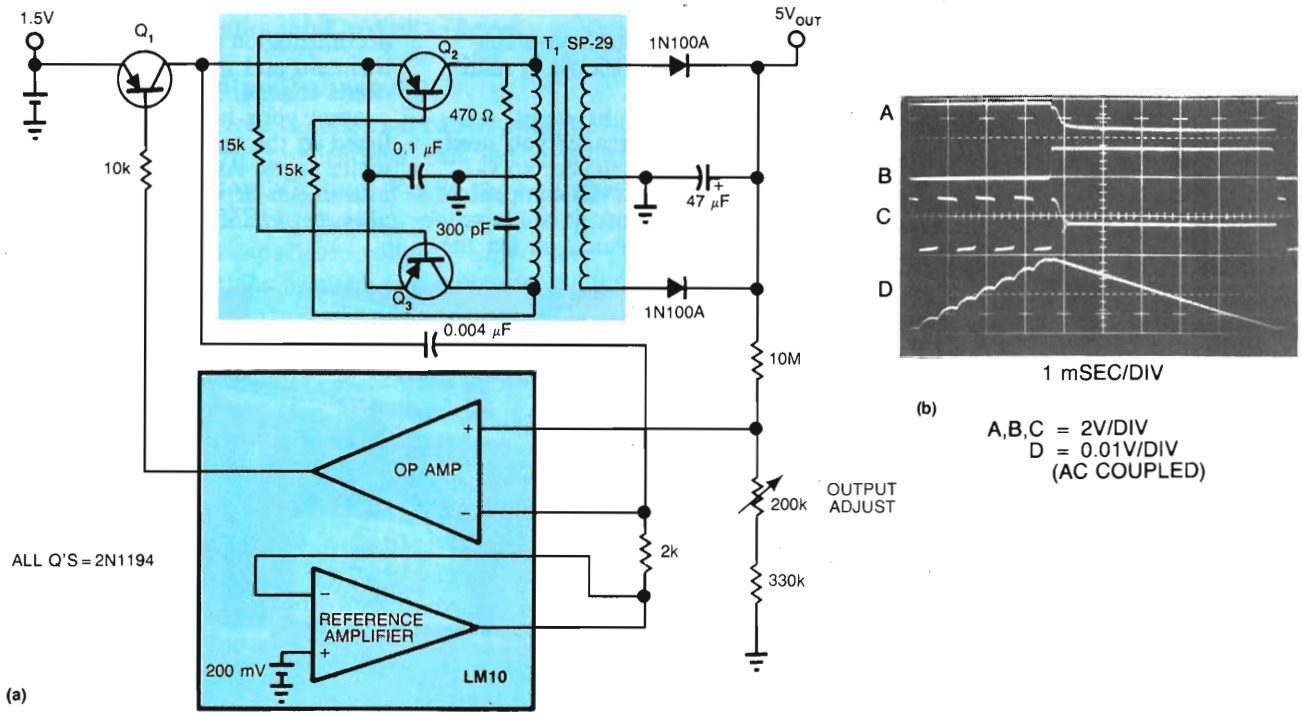


Fig 7—By including a transformer, (a) *has a voltage gain of more than a factor of two. Q_1's collector (top trace,* ***(b)****) goes high when the output voltage (bottom trace) falls lower than the loop's set point. The second and third traces display the LM10 output and Q_2's collector, respectively.*

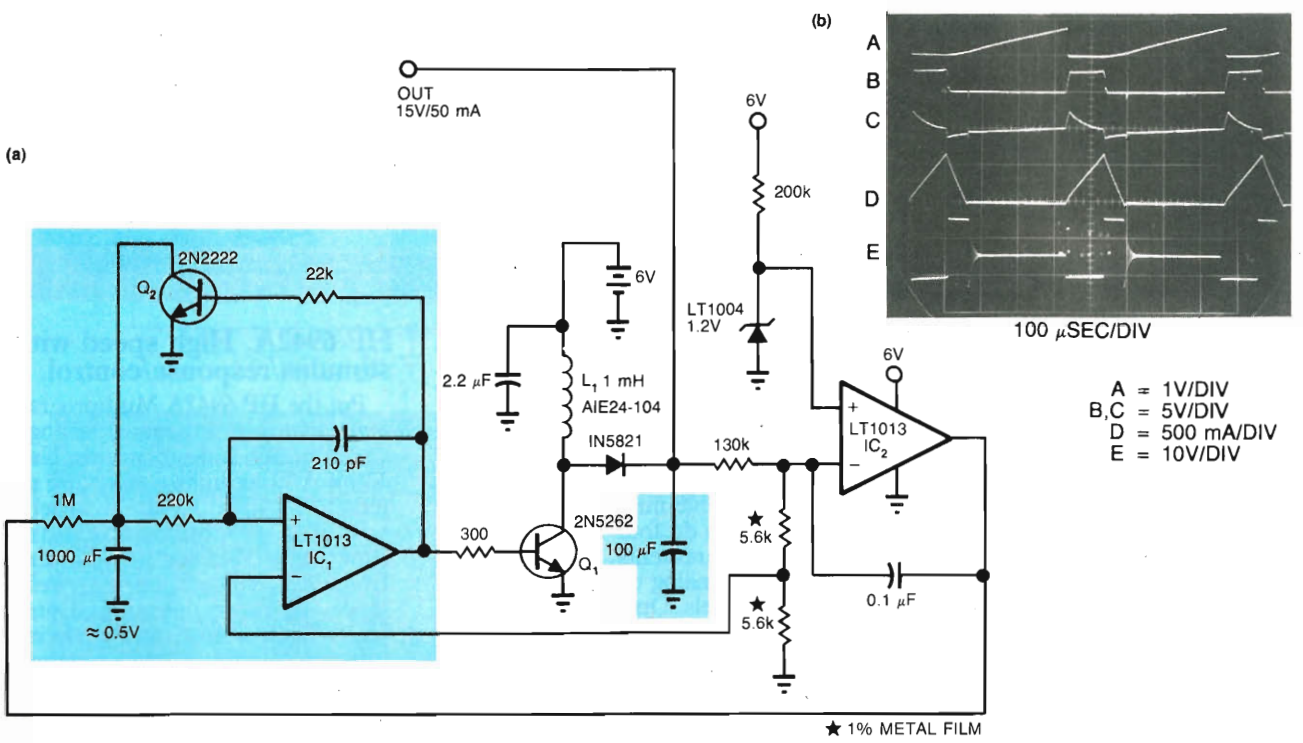


Fig 8—This flyback-class converter (a) *delivers 15V from a 6V battery. With an efficiency of 78%, this circuit can supply 50 mA, regulated within 0.05%.*

switched-capacitor voltage divider that never completes a full cycle. Power MOSFETs easily handle the high transient currents, and overall efficiency is 83%.

Circuits step up output voltage

All the previous circuits condition battery output to a lower voltage. Many applications call for a voltage higher than the battery's output. **Fig 6a** shows a simple way to double available battery voltage using the LTC1044 switched-capacitor voltage converter. As shown, the IC functions in much the same way as does **Fig 5a**'s circuit, but at greatly reduced power levels. This circuit will drive low-power 74-CMOS loads for long times from two small cells, which supply 3 to 15V. Efficiency exceeds 90% for load currents below 1.75 mA. **Fig 6b** plots output voltage vs loading.

Fig 6c fixes the problem of **Fig 6a**'s drop in regulation. As in **Fig 5a**, feedback techniques compensate for the voltage converter's output impedance. The LTC1044 in **Fig 6c** is a voltage doubler; the 1-μF capacitor pumps up the 100-μF capacitor. Q_1 and Q_2 are a bidirectional switch that can interrupt the pump-up action. An LM10 op-amp reference controls the switch that regulates the output. When the output voltage decays enough (**Fig 6d**, top trace), the LM10's reference amplifier swings high (middle trace), driving the op amp negative (bottom trace), and both transistors turn on. This allows the LTC1044 to pump charge to the 100-μF capacitor. For each charge cycle, the output takes a voltage step up. When the output steps high enough, the LM10 switches off and the cycle repeats.

Repetition is load dependent, with typical values of 1 to 400 Hz. The loop's gain-bandwidth sets response hysteresis to 40 mV. The feedback network fixes the 5V output within 0.025V for loads up to 2 mA (plotted in **Fig 6b**).

Transformer increases voltage gain

The circuit in **Fig 7a** is conceptually similar to the one in **Fig 6**, except that **Fig 7**'s circuit uses a transformer to get greater voltage gain. This produces a 5V output from a single 1.5V cell. Q_2, Q_3 and T_1 form a self-oscillating dc-dc converter, which is controlled by the Q_1 switch. As in **Fig 6c**, an LM10 closes the feedback loop around this battery step-up converter. With only 1.5V at the input, you must pay particular attention to switch-saturation losses. The germanium transistors specified have under 50-mV drop, less than silicon types. Germanium output diodes also contribute low forward-drop losses. The 0.004-μF capacitor sets hysteresis at 20 mV, preventing erratic loop dynamics. An RC damper in T_1's primary eliminates parasitic high frequency oscillation.

Fig 7b shows the operation of the circuit in **Fig 7a**;

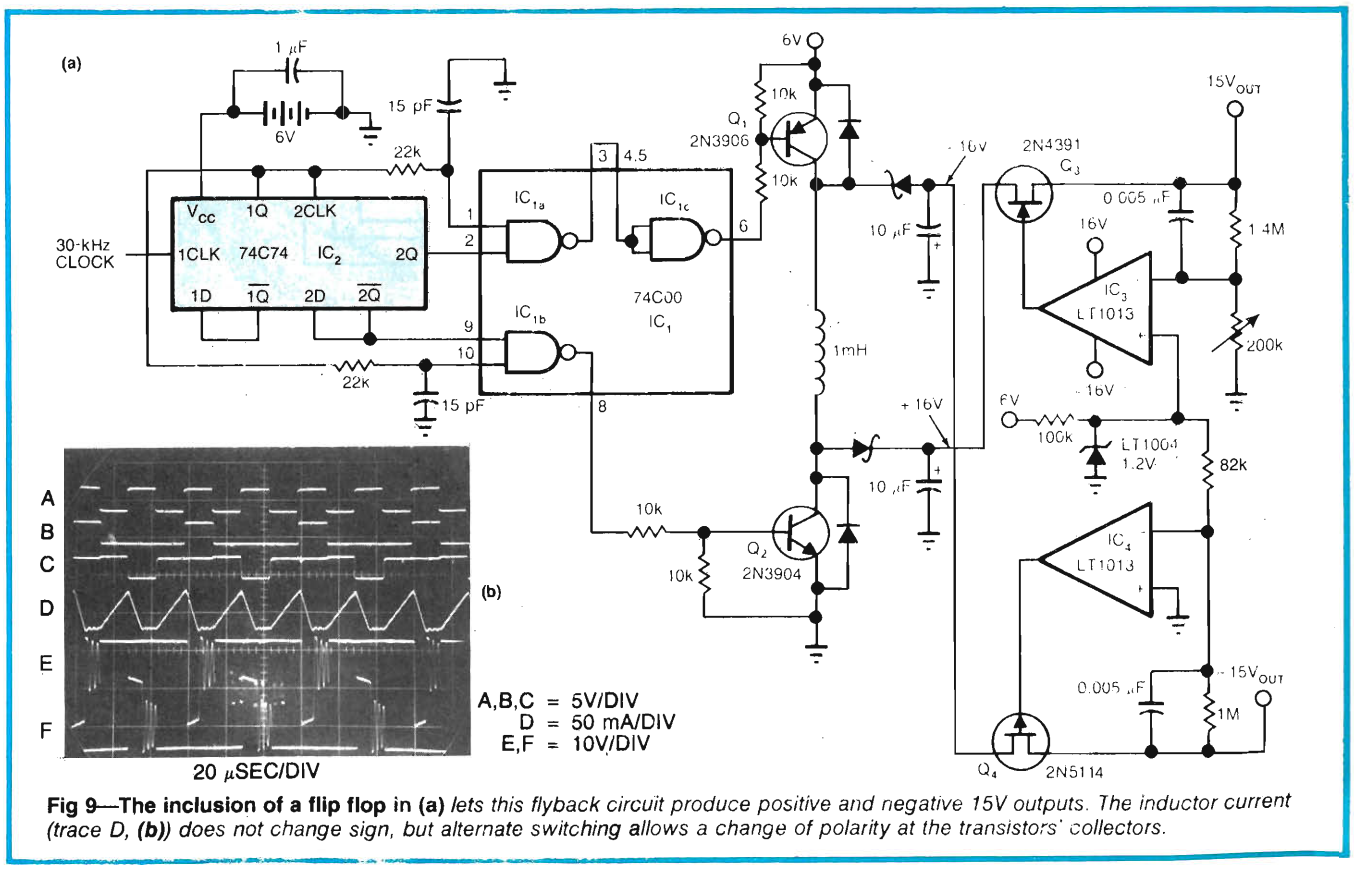


Fig 9—The inclusion of a flip flop in (a) *lets this flyback circuit produce positive and negative 15V outputs. The inductor current (trace D,* ***(b)****) does not change sign, but alternate switching allows a change of polarity at the transistors' collectors.*

Flyback circuit increases voltage gain

Q_1's collector (top trace) goes high when the circuit's output voltage (bottom trace) falls below the loop's set point. The second and third traces are the LM10's output and Q_2's collector, respectively. Note that the output's ramp steps up in a manner much like that of **Fig 6c**'s capacitively driven circuit. As with **Fig 6c**, loop oscillation frequency depends directly on the load, and is typically 1 to 250 Hz. This circuit will supply a 5V, 150-μA load (about 25 CMOS SSI ICs) for 3000 hrs from a single 1.5V D battery.

Fig 8a shows a 15V-output converter that delivers up to 50 mA from a 6V battery. Efficiency is 78%. Feedback controls the frequency of inductive events in this flyback converter. The inductor's output, rectified and filtered to dc, biases the feedback loop to establish a stable output.

If the converter's output is below the loop's set point, IC_2's inputs are unbalanced, and the current is fed through the 1-MΩ resistor at IC_1. This ramps the 1000-pF value positive (trace A, **Fig 8b**). When this

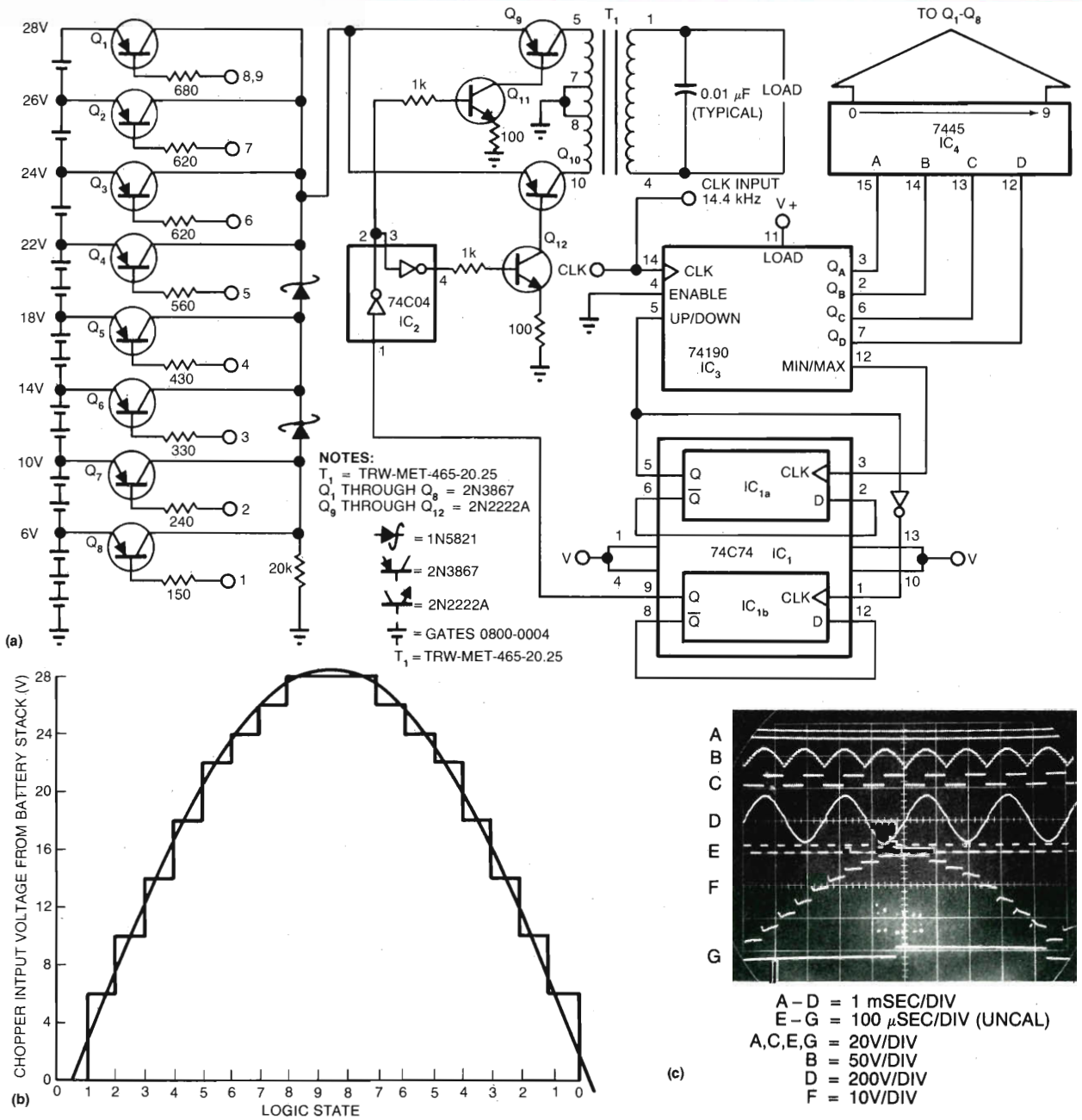


Fig 10—A 28V battery can drive 115 V ac with this design. *The circuit* ***(a)*** *sequentially switches segments of the battery stack into a fixed-gain, step-up voltage chopper. As a function of the sequencing logic's state, the voltage going into the chopper* ***(b)*** *closely fits a sine wave.*

Batteries drive 400-Hz ac load

ramp exceeds the 0.5V potential at IC_1's positive input, the amplifier switches high (trace B). Q_2 comes on, discharging the 1000-pF capacitor to ground. Simultaneously, regenerative feedback through the 210-pF capacitor causes a positive-going pulse at IC_1's positive input (trace C), sustaining IC_1's positive output. Q_1 comes on, allowing inductor (L_1) current to flow (trace D). When IC_1's conduction pulse decays, Q_1 turns off. Then, the inductor's flyback effect pulls Q_1's collector high (Trace E), and the energy in the inductor gets stored in the 100-μF capacitor.

The 100-μF capacitor's voltage, which is the circuit output, gets sampled by IC_2 to close a loop around the IC_1-Q_1 combination. This loop forces IC_1 to oscillate at whatever frequency maintains the 15V output. IC_1's fixed output-pulse width prevents L_1 from ever saturating and destroying Q_1. The 0.1-μF capacitor at IC_2 compensates the feedback loop, and the LT1004 serves as a reference. Regulation is within 0.05% over a wide range of output loads and temperature coefficient is typically 50 ppm/°C. The relatively high voltage/power output of this circuit suits mixed linear-digital systems.

Single inductor yields two voltages

Fig 9a shows a way to obtain positive and negative 15V outputs from a single inductor. The circuit alternately allows one end of the switched inductor to supply energy to one of the regulators. The resultant positive and negative peaks get rectified, stored and regulated to produce a bipolar output. The 30-kHz clock drives the 74C74 flip flop, producing a square wave at Q_1 (trace A, **Fig 9b**). This waveform gets fed to the 74C00 network. The RC networks between the chips prevent unwanted pulses caused by flip-flop delay. IC_{1b} and IC_{1c}'s outputs appear as traces B and C, respectively, and bias Q_1 and Q_2 on and off.

The logic alternately turns Q_1 and Q_2 off when the inductor flies back. Although the inductor's current (trace D, **Fig 9b**) always flows in the same direction, the alternating switching allows positive and negative flyback action. Trace E shows Q_1's collector, and trace F is Q_2's output. The ringing, which is due to incomplete damping, is common in low-power converters and isn't deleterious to circuit operation. The LT1013 dual op amp and the FETs form a dual, low-dropout 15V regulator with 30-mA output capability. These mirror-image circuits function like the one shown in **Fig 4c**.

Produce a 115V ac output from dc input

Not all battery converters must produce a dc output. Some battery-driven systems need high-voltage, sine-wave-driven devices like small motors, gyros and synchros. Deriving high-voltage sine waves from a battery supply is possible with linear techniques, but efficiency is poor. **Fig 10a** shows a circuit that obtains 78% efficiency by sequentially switching segments of a 28V battery stack into a fixed-gain, step-up voltage chopper. **Fig 10b** illustrates the voltage presented to the chopper as a function of the sequencing logic's state. The battery stack's segments provide the best sine-wave fit.

Fig 10c details waveforms of operation. Trace A is the 14.4-kHz clock, which feeds the logic network. The logic generates nine discrete states, which bias Q_1 through Q_8 On sequentially. These transistors sequentially place portions of the battery stack at the input of the Q_9, Q_{10}, and T_1 chopper. The 74C74 flip flop, IC_{1a}, directs the 74190 up-down counter to reverse directions each time it reaches zero, resulting in a repetitive, rectified sine wave at the chopper input (trace B). The diodes in the transistor's collector line prevent reverse breakdown. A flip flop in IC_{1b} (trace C) alternately biases Q_9 and Q_{10} On so that T_1 receives alternating drive. T_1's output approximates a sine wave (trace D) at the voltage step-up of the transformer's ratio.

In this case, the output is 115V ac, 400 Hz with a power capability of about 20W. The 0.01-μF capacitor shown in **Fig 10a** filters residual harmonics and may not be required for some loads. Traces E, F and G are increased-resolution representations of traces A, B and C. They clearly show the relationship between the clock and the chopper-input stepping. You can see the dissimilar amplitude steps, in accordance with the schema in **Fig 10b.** **EDN**

Author's biography

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and -instrumentation design. He has served in related capacities at National Semiconductor Corp, Arthur D Little Inc and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art and collecting antique scientific instruments.

Settling-time measurements demand precise test circuitry

Fast op amps and D/A converters make settling-time measurement a mandatory design task. Building a test setup that handles such devices, though, requires a fundamental understanding of the components as well as the test instruments.

Jim Williams, *Linear Technology Corp*

Amplifiers in servo, digital/analog-converter, and data-acquisition applications require good dynamic response —in particular quick settling to a final value after an input step. This settling-time spec plays a key role because it allows you to establish circuit timing margins with confidence and to know that output data is valid. To develop accurate settling-time figures for your high-speed-amplifier circuits, though, you need high-performance test circuitry, and designing such testers can prove challenging. A look at the characteristics of one circuit that allows you to determine precise high-resolution settling-time parameters illustrates the problems you must address.

Watch for hidden flaws

First, examine the problems you're likely to encounter when designing test circuits for this purpose. The network in **Fig 1** illustrates one method for measuring amplifier settling time (**Refs 1, 3,** and **5**). The resistors and amplifier form a bridge network, and the circuit uses a false-summing-node technique. Assuming ideal resistors, the amplifier output steps to $-V_{IN}$ when you apply an input pulse. While the signal slews, the diodes hold the scope probe's output constant to limit voltage excursions. When settling occurs, the scope probe's voltage would ideally equal zero, but because of divider attenuation, it equals one-half the settled voltage level.

This circuit theoretically allows you to observe small-amplitude settling voltages. In practice, though, several flaws prevent it from producing useful measurements. First, the circuit requires an input pulse with a top that's flat to within required measurement limits; you're generally interested in the time required for the amplifier's output voltage level to settle to within a

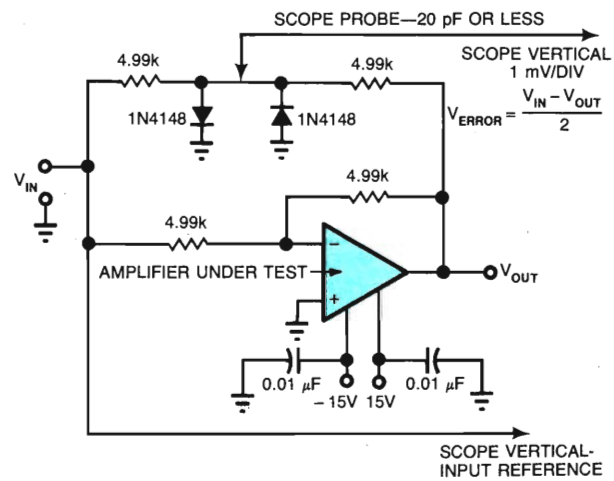


Fig 1—Using the false-summing-node technique *to measure amplifier settling time, this test circuit uses the resistors and the amplifier to form a bridge-type network. However, it performs poorly with most available scope probes.*

Scope aberrations from pulse generators can hide amp drift

10-mV band in response to a 10V step input. However, general-purpose pulse generators don't hold output amplitude and noise within these limits. Thus, probes can pick up pulse-generator output aberrations that are indistinguishable from amplifier output movement, and so the resulting measurements are unreliable.

Other problems arise from the scope connection. As probe capacitance rises, ac loading of the resistor junction influences observed settling waveforms. A probe with capacitance of 20 pF or less alleviates this problem, but its 10× attenuation sacrifices oscilloscope gain. Furthermore, most 1× probes aren't suitable because of excessive input capacitance.

An active 1× FET probe does work; clamp diodes at its probe point reduce voltage swing during amplifier slewing, thereby preventing excessive scope overdrive. Unfortunately, scope overdrive recovery characteristics vary widely and aren't usually specified. The diodes' 600-mV drop can represent an unacceptable overload for some scopes and bring displayed results in question. (See **box**, "Evaluating scope overload response.")

Fig 2 shows a practical settling-time test circuit that addresses these problems. Combined with an appropriate scope, it provides reliable settling-time measure-

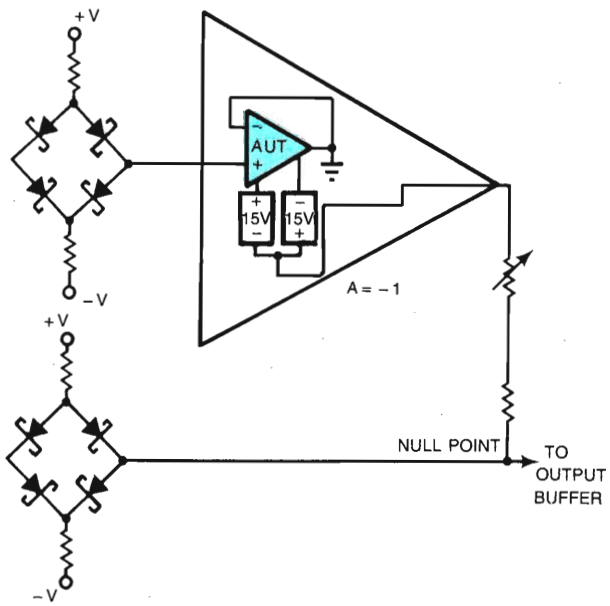


Fig 3—By using a battery for the amplifier under test *so that it floats from the main supply line, you can test both inverters and followers with the basic settling-time test circuit in* ***Fig 2.***

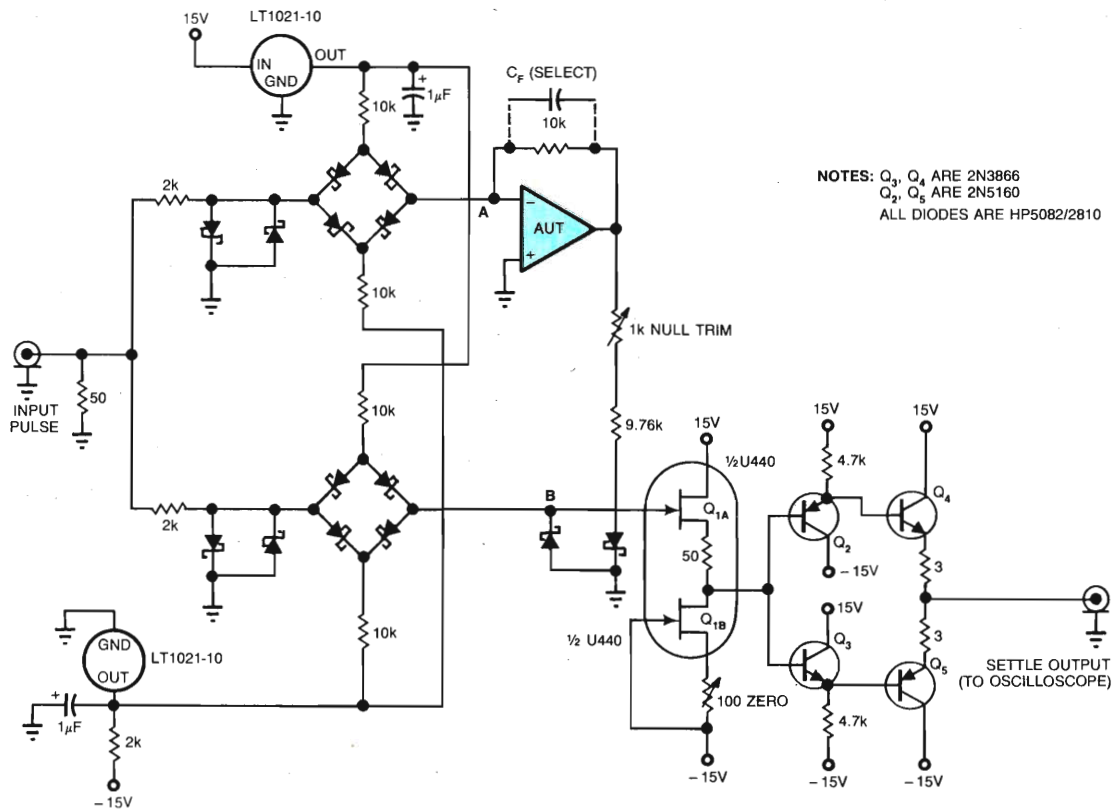


Fig 2—Reliable settling-time measurements *with accuracies in the 0.1 to 0.01% region are possible when you combine this test circuit with an appropriate scope. Input-pulse characteristics don't influence the measurement.*

ments with accuracies in the 0.1% to 0.01% region. The input pulse doesn't drive the amplifier; instead it switches a Schottky bridge through a clamp.

Two LT1021 10V references bias the bridge. Depending on input polarity, current flows through the appropriate 10-kΩ resistor to bias the amplifier's summing point. The bridge switches cleanly and quickly, producing a flat-topped current pulse that drives the amplifier under test (AUT). Note how input pulse characteristics no longer influence the measurement. A second clamp bridge supplies an opposite-polarity signal that's nulled against the amplifier's output at point B. Schottky clamp diodes limit the voltage excursion at point B to ±300 mV.

The **Fig 2** circuit's transistor configuration (Q_1 through Q_5) forms a low-input-capacitance, high-speed buffer that drives the scope. Q_{1A}'s 1- to 2-pF input capacitance presents light ac loading and thereby eliminates probe-related problems. Q_{1B} operates as a current

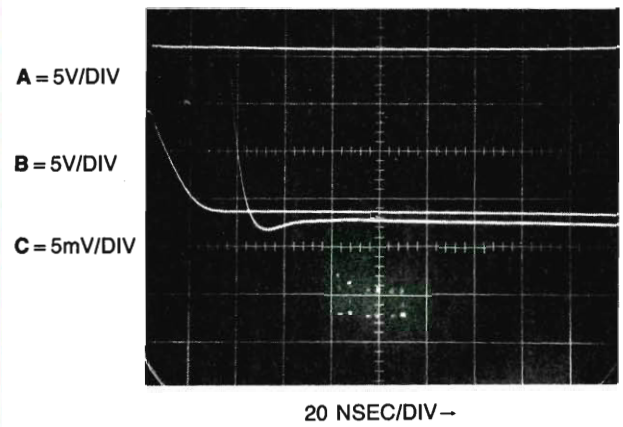


Fig 4—Gain confidence in your test circuit *by trying it out on a very fast UHF amplifier such as a Teledyne Philbrick 1435. That device is spec'd to settle in 70 nsec, and these test results confirm the device spec.*

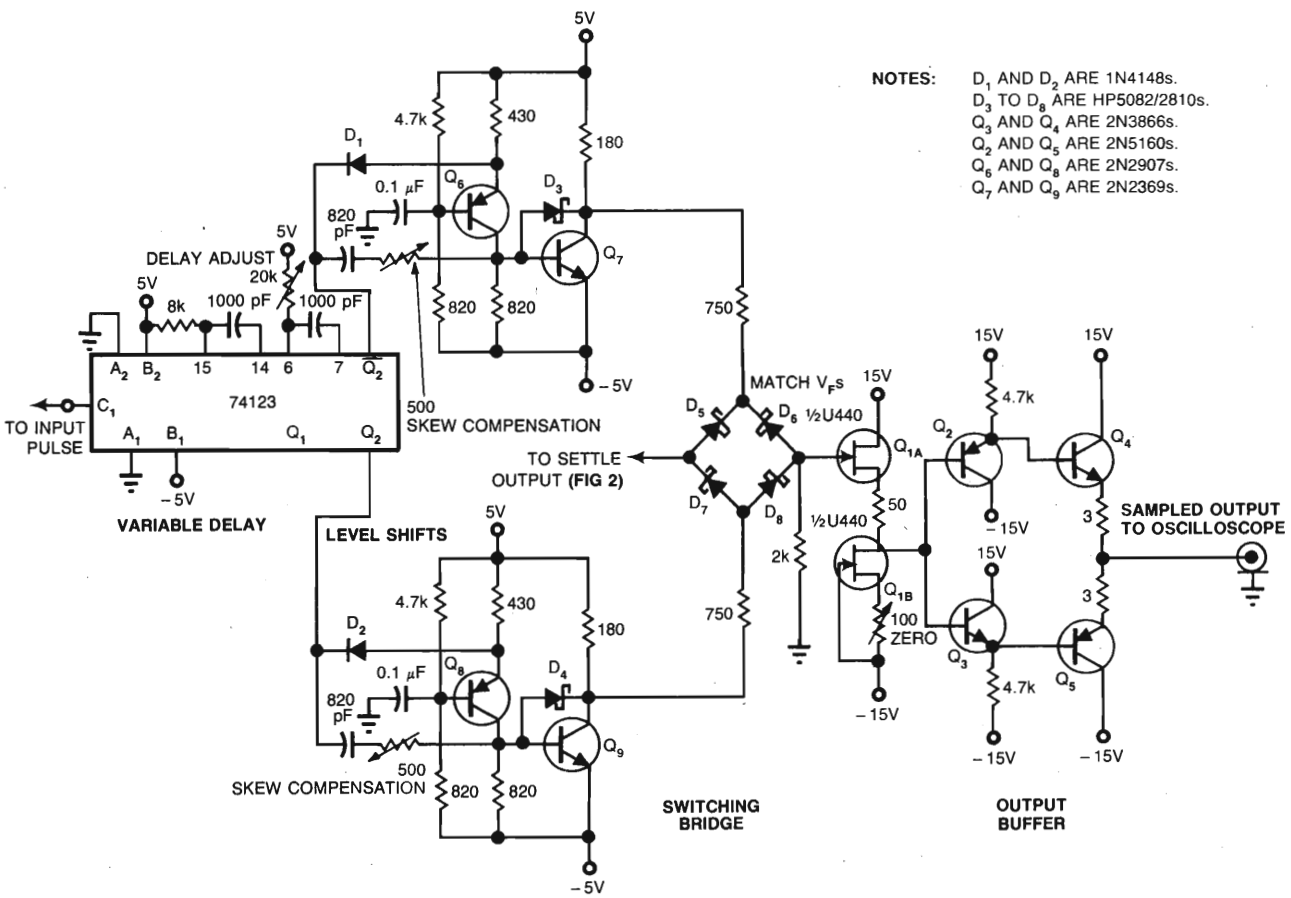


Fig 5—Improve Fig 2's performance *by connecting this network to the test circuit's output. The Schottky sampling bridge's inherent balance, combined with matched diodes and high-speed complementary bridge switching, yields a clean switched output. The circuit permits 10-µV measurements.*

Solder very-high-speed amps directly to the test setup

sink and compensates Q_{1A}'s V_{GS} drop. Transistors Q_2 through Q_5 form a complementary emitter follower that drives substantial cable capacitance without distortion.

When building the circuit, make sure the pc board's ground plane minimizes stray capacitance at points A and B. Because of this same effect, select a test-device socket with short leads. When dealing with high-speed amplifiers (with settling times less than 200 nsec), solder them directly to the board.

Used with a matched scope, this circuit allows you to observe amplifier settling to 1 mV for a 10V step (0.01%). Because this circuit works by nulling opposite-polarity sources, you might think that it can't test follower amplifiers. Not true. The AUT is battery-powered and floats relative to the circuit's power supply **(Fig 3).** The AUT output connects to circuit ground, the battery center tap becomes the output, and the Schottky bridge drives the amplifier's positive input. With this configuration, the circuit tests followers the way it does inverters. Note that the AUT's output appears inverted.

To calibrate the test circuit, ground point B and adjust the zero trim for 0V output. Next, temporarily tie the pulse input to +15V through a 680Ω resistor and adjust the null trim for 0V output. Now remove the resistor and the circuit is ready for use. When measuring settling times, remember to experiment with C_F to obtain best performance (see **box,** "Proper compensation is critical").

With such a high-precision circuit, you'll want to test it before putting it to work on devices with unknown characteristics. You can gain confidence in the circuit by testing a very fast UHF amp such as a Teledyne Philbrick 1435, which is specified to settle within a millivolt for a 10V step in 70 nsec. **Fig 4** shows the results of a trial run; trace A is the input pulse, B is the

Evaluating scope overload response

Settling-time measurements rely heavily on the oscilloscope used. In many cases, the scope must supply an accurate waveform after the display has been driven off the screen. How long must you wait after an overload before taking the display information seriously? The answer to this question is quite complex.

Many factors come into play: the degree of overload, its duty cycle, its magnitude in time and amplitude as well as other considerations. Scope response to overload varies from model to model, and you can also observe markedly different behavior in each instrument. For example, the recovery time for a given overload at 0.005V/div sensitivity can differ considerably from that at 0.1V/div. The recovery characteristic can also vary with waveform shape, dc content, and repetition rate. With so many variables, you obviously have to approach measurements involving scope overload with caution. Fortunately, a simple test, illustrated in the **figure,** indicates when overdrive deteriorates scope performance.

First, place the waveform to be expanded on the screen with vertical sensitivity set to eliminate all off-screen activity **(a).** Assume you want to expand the lower right portion and therefore increase vertical sensitivity by a factor of two. Doing so, however, drives the waveform off the screen **(b),** but the remaining display seems reasonable: Amplitude has doubled, and waveshape is consistent with the original display. A careful look reveals a dip in the waveform at about the third vertical division as well as some disturbances to the right of the dip. All in all, this expansion of the original waveform is believable.

Increasing gain even further, as in **c,** amplifies all the features of **b.** The basic wave shape appears more clearly, and the dip and small disturbances are also easier to see. However, no new waveform characteristics become visible. On the other hand, when you again increase vertical sensitivity by a factor of two, some unpleasant surprises appear **(d).**

This gain increase causes definite distortion. Although larger, the initial negative peak has a different shape—the bottom isn't as broad as in **c.** In addition, the positive peak's recovery has a slightly different shape, and a new rippling disturbance is visible in the center of the screen. Such changes indicate that the scope is having trouble, and an additional test confirms that overloading influences this waveform.

Without changing the vertical gain, use the vertical position knob to relocate the display at the bottom of the screen **(e).** Doing so shifts the scope's dc operating point, which under normal circumstances should have no effect on the displayed waveform. In this case, though, a marked shift in waveform amplitude and outline occurs. Repositioning the waveform to the top of the screen **(f)** produces a different type of waveform distortion. Thus, it's obvious that for this waveform you can't get accurate settling-time test results using a 0.1V/div gain setting.

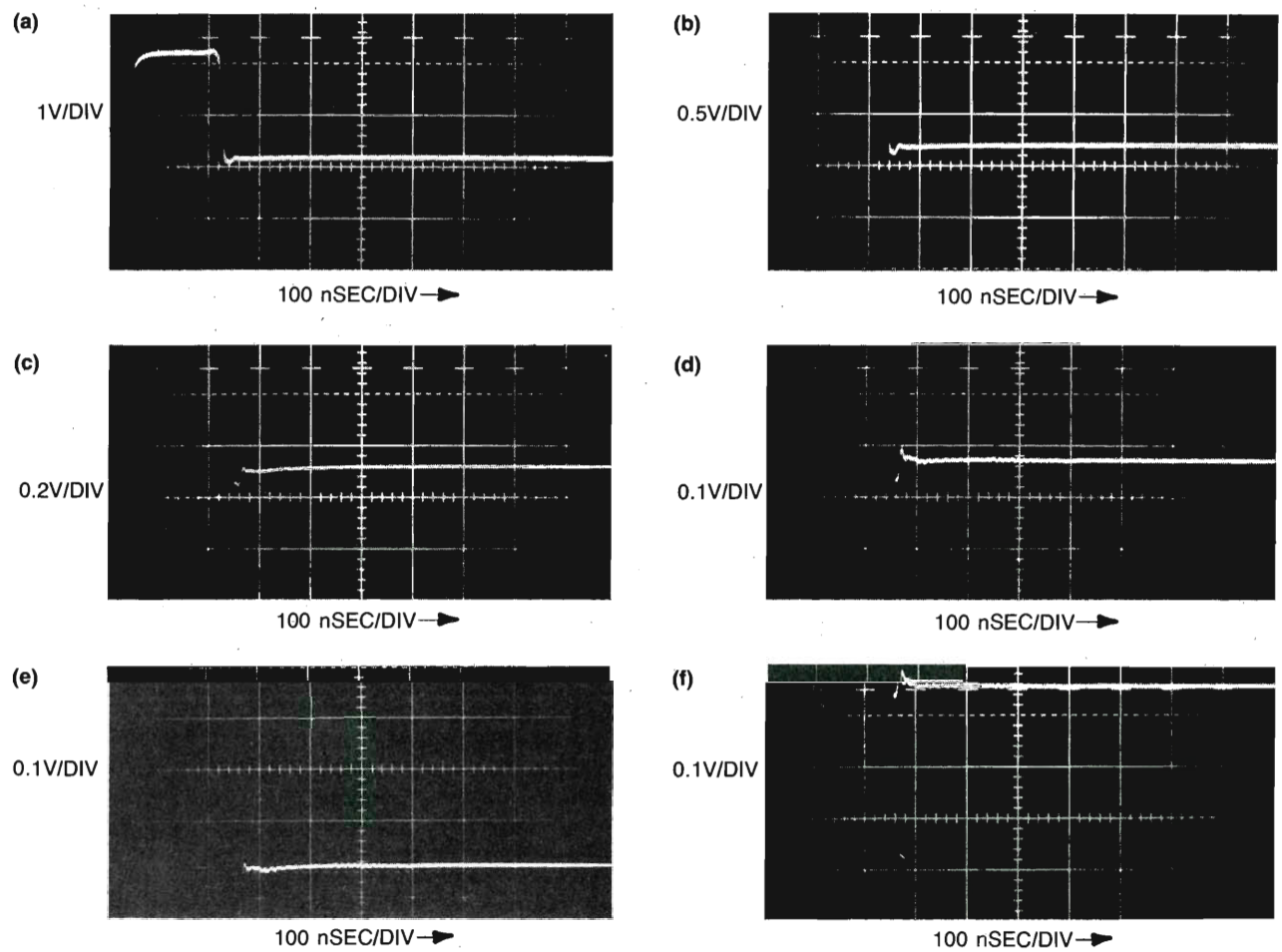
amp's output, and C is the settled signal. Settling occurs within 70 nsec. This indicates sound agreement between the test-circuit results and the AUT specs. Because most amps aren't nearly this fast, you can assume that the circuit provides reliable results.

Settling time requirements increase

In the past, designers rarely had to worry about measuring amplifier settling levels below 1 mV. This is not the case today: 16- and 18-bit D/A converters are common, and designers must deal with settling times to submillivolt levels. Furthermore, until recently you didn't have to worry about measuring amplifiers' settling times to within 50 μV because their thermal drift swamped such values. Today, however, monolithic amplifiers' offset specs make very high precision settling-time data an important parameter.

Obtaining higher precision measurements with **Fig 2**'s circuit requires some modifications. The 300-mV Schottky clamp potential at point B limits its resolution to 0.01%. Trying to improve resolution by increasing scope gain doesn't work because of severe overload problems. With the scope set to 50 μV/division, the Schottky boundary allows a 6000:1 overdrive, but no scope vertical amplifier can accommodate such levels. Scope overload recovery dominates the observed waveform, making all measurements meaningless.

One way around this problem is to clip the incoming waveform. By preventing the scope from seeing the waveform until settling is nearly complete, you avoid overload conditions. To clip the waveform, place a switch at the settling circuits' output and control it with an input-triggered variable delay. Don't use FET switches: Their gate-source capacitance allows gate-drive perturbations to corrupt the scope display and produce confusing readings. In the worst case, gate-



To detect whether overdrive *adversely affects scope performance, you can run a simple test in which you gradually increase scope sensitivity until waveform distortion appears.*

Null opposite polarity sources to handle followers as well

drive transients become large enough to induce overload and defeat the switch's purpose.

Fig 5 illustrates a switch implementation that eliminates these problems. Connected to **Fig 2**'s measurement network, this circuit allows you to observe settling to within 10 μV. The Schottky sampling bridge provides the switching action, and its inherent balance, combined with matched diodes and high-speed complementary bridge switching, yields a clean switched output. An output buffer stage identical to that in **Fig 2**'s circuit unloads the bridge and drives the scope.

The Q_1-Q_2 and Q_3-Q_4 level shifters supply the switching drive for the complementary bridge. Including an emitter-switched current source feeding a Baker-clamped common emitter output, each circuit converts the variable-delay one-shot's TTL output to ±5V levels. Feedforward capacitance to the output transistor increases speed—overall delays are roughly 3 nsec. These level shifters must switch simultaneously to minimize drive-induced disturbance in the bridge's output. The skew compensation trims allow you to make minor phasing adjustments in each level shifter and thereby compensate for skews in the 74123's outputs.

TYPICAL AMPLIFIER SETTLING-TIME FIGURES

AMPLIFIER	SETTLING TIME (μSEC)	REMARKS
LT1001	65	
LT1007	18	
LT1008	65	STANDARD COMPENSATION
LT1008	35	FEEDFORWARD COMPENSATION
LT1012	70	
LT1055	6	
LT1056	5	

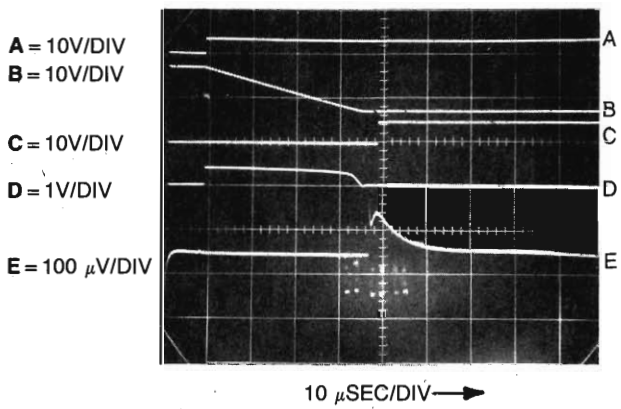


Fig 6—Measurements of an amplifier's settling time *using the* ***Fig 5*** *test circuit show the amplifier capabilities. A LT1001 op amp sees the input in* ***A*** *and produces the output in* ***B.*** *During its slewing, the one-shot fires* ***(C)*** *and turns off the bridge, whose input is in trace* ***D.*** *Trace* ***E*** *shows the circuit's final output at a vertical sensitivity of 100 μV/div.*

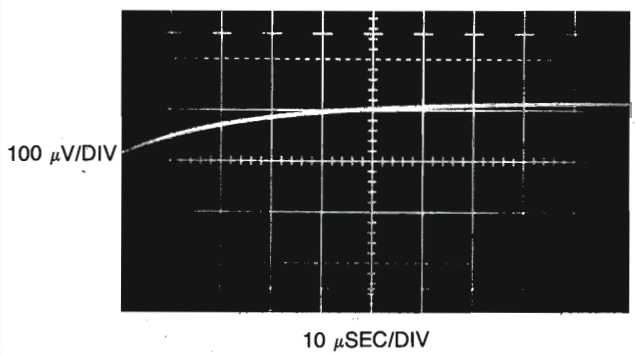


Fig 7—Thermal tails *such as this one, which extends for many milliseconds after settling apparently occurs, arise from die heating.*

To calibrate this circuit, ground the bridge input and pulse the 74123's C_1 input. Now set the scope to 100 mV/div and adjust the skew trims for minimum indication on the screen. Connect the bridge input back to the settling circuit's output and it's ready for use. Exercise extreme care when constructing this circuit. A ground plane is mandatory, and keep all bridge connections as short as possible. To minimize noise, route the bridge's output ground return away from high-current returns such as the 74123's ground pin.

Combined with the settling-time measurement network in **Fig 2,** this switch circuit provides performance adequate for today's amps: The **table** lists settling times measured at 50 μV/div (0.0005% of a 10V step) for a group of precision amplifiers, and **Fig 6** shows test results for one of these devices, the LT1001. Traces A and B show the input pulse and the AUT output, respectively. The 74123 one-shot fires during the AUT's slewing period (trace C represents the one-shot's Q output), turning off the bridge. (Trace D shows the bridge input.) The 74123 delay is set so the bridge switches when settling is nearly complete. Trace E, the circuit's final output, shows settling details at 100 μV/div. The narrow peaking at the waveform's leading edge arises from switching residue.

Watch for temperature problems

When making settling-time measurements, you must always consider temperature effects. Some poorly designed amplifiers exhibit substantial thermal tails after responding to an input step. Generated by die heating, this phenomenon can cause the output to wander outside desired limits long after the amplifier has apparently settled. After checking settling time at high speeds, it's always a good idea to slow the scope down

Proper compensation is critical

To realize the best settling-time performance from any amplifier, you must specify the feedback capacitor (C_F) carefully. This component rolls off amplifier gain at the frequency that provides the best dynamic response, and its optimum value depends on the feedback resistor's value and source characteristics.

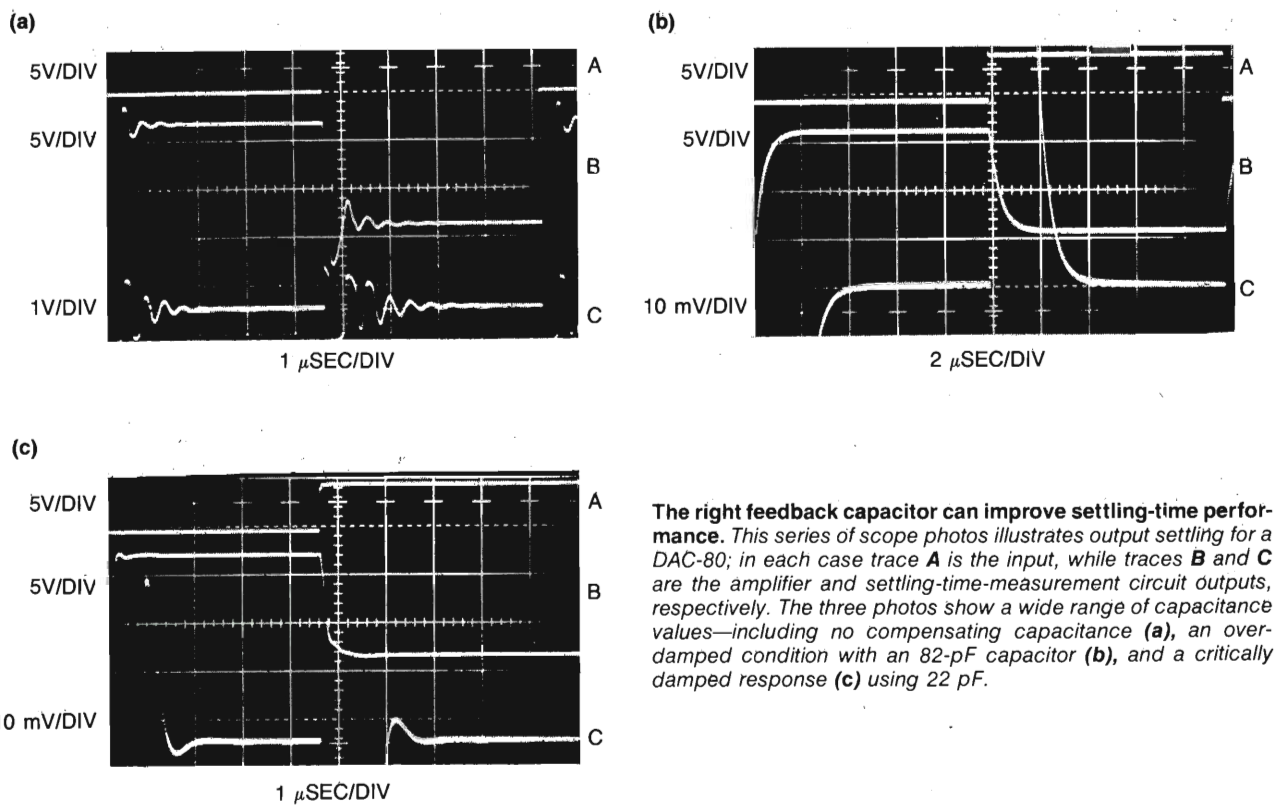
Unfortunately, one of the most common sources—a D/A converter—is also one of the most difficult to handle. In many cases, you must convert a D/A converter's current output to a voltage. You can easily do so with an op amp, but careful design techniques are paramount if you hope to obtain good dynamic performance.

A fast D/A converter can settle to 0.01% in 200 nsec. However, its output also includes a parasitic capacitance that makes the amplifier's job more difficult. Normally, the D/A converter's current output unloads directly into the amplifier's summing junction and thus effectively places a parasitic capacitance across the amplifier input. This capacitance introduces feedback phase shift at high frequencies, forcing the amplifier to hunt and ring about the final value before settling.

D/A converters have various output - capacitance values: CMOS devices have the highest output capacitance, which varies with the input code. Bipolar D/A converters typically have 20 to 30 pF of capacitance, but it's stable over all codes. Given their output capacitance characteristics, D/A converters provide an instructive example for illustrating the importance of amplifier compensation.

To study this effect, you can use the settling-time measurement circuit shown in **Fig 2** of the accompanying article, but replace the Schottky bridge that feeds the amplifier under test (AUT) with the D/A converter in question. Depending on the D/A converter input coding, you might have to use inverters on the input lines to maintain nulling action. The nearby scope photos show the response of a DAC-80 combined with an LT1023 op amp optimized for inverting applications. In all cases, trace A shows the input while B and C show the amplifier and settling outputs, respectively.

With no compensation capacitor **(a),** the amplifier rings badly before settling. An 82-pF feedback capacitor stops the ringing, and settling time drops to 4 μsec **(b).** This overdamped response indicates that C_F dominates the capacitance at the AUT's input, and stability is assured. If the response in **b** isn't fast enough, then reduce C_F. For instance, using a 22-pF compensation capacitor yields the critically damped response shown in **c.** The 2-μsec settling time shown is the best obtainable with this converter/amplifier combination.



The right feedback capacitor can improve settling-time performance. *This series of scope photos illustrates output settling for a DAC-80; in each case trace* ***A*** *is the input, while traces* ***B*** *and* ***C*** *are the amplifier and settling-time-measurement circuit outputs, respectively. The three photos show a wide range of capacitance values—including no compensating capacitance* ***(a),*** *an overdamped condition with an 82-pF capacitor* ***(b),*** *and a critically damped response* ***(c)*** *using 22 pF.*

and look for thermal tails; **Fig 7** shows such a thermal tail. To get a better view of the tail, in most cases you can accentuate its effect by loading the amplifier's output. **EDN**

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Author's biography

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in related capacities at National Semiconductor Corp, Arthur D Little Inc, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art, and collecting antique scientific instruments.

Circuits allow direct digitization of low-level transducer outputs

Designers like to digitize analog signals as far forward in the signal chain as possible, but many believe that dc preamps are mandatory. Part I of this 2-part series describes circuits that digitize low-level signals without preamplification.

Jim Williams, *Linear Technology Corp*

Almost all transducers produce low-level signals, and designers typically use signal-conditioning amplifiers to boost the output prior to further processing or transmission. However, many systems now transmit transducer outputs digitally to reduce noise and eliminate the inaccuracy problems associated with analog transmission over long cable runs. In fact, designers want to digitize signals as far forward in the signal chain as possible, and although you might believe that dc preamplification of transducer outputs is still mandatory, such is not the case: New components and design techniques allow you to digitize directly at the transducer.

This 2-part series details such circuit techniques, which you can use to digitize low-level transducer outputs and eliminate the traditional dc gain stage without sacrificing performance. The circuits produce serial frequency outputs that you can transmit over one wire with the characteristic noise immunity of digital systems. Part I discusses methods of handling the most common transducer quantities: temperature and force. Part II (scheduled for January 10, 1985) will discuss similar methods for handling light, humidity, level, and acceleration.

Obviating dc preamplification

Before moving on to these techniques, it's worthwhile to examine the reason why most designers feel dc preamplification is necessary. Classical A/D-conversion techniques emphasize high-level input ranges to keep LSB step sizes as large as possible and thus minimize offset and noise errors. For this reason, A/D LSB size is almost always greater than a millivolt, with 100- to 200-μV/LSB step sizes in some 10V FS devices.

Now consider the minimum A/D-converter step size required for direct digitization of the output of a typical strain-gauge transducer. The device's full-scale output is 30 mV, so a 10-bit A/D converter must have an LSB increment of only 30 μV. Performing a 10-bit conversion on a type-K thermocouple monitoring a 0 to 60°C environment proves even more stringent. The thermocouple generates 41.4 μV/°C over the 0 to 60°C range. The following equation determines the LSB increment:

$$\frac{41.4\ \mu V/^{\circ}C \times 60^{\circ}C}{1000} = 2.48\ \mu V/LSB.$$

These step sizes are far smaller than those found in commercially available A/D converters, leading some designers to conclude that it's impossible to digitize the step sizes without dc preamplification. But circuitry designed specifically for that task directly digitizes the outputs from these transducers (and others) to stable 10-bit resolution.

Start with an IC temperature sensor

The straightforward circuit shown in **Fig 1** converts an LM134 temperature sensor's current output to a corresponding output frequency. The sensor pulls a temperature-dependent current (0.33%/°C) from IC_1's positive input node. This point, biased from the LM329-driven resistor string, responds with a temperature-dependent voltage that varies the operating point of IC_1, which is configured as a self-resetting integrator. IC_1 integrates the LM329-referenced current into its summing point and produces a negative ramp. When the ramp amplitude becomes large enough, the transistors turn on, thereby resetting the feedback capacitor and forcing IC_1's output to zero. When the capacitor's reset current goes to zero, the transistors turn off, and

Designers like to digitize early in the signal chain

IC_1 again begins to integrate negatively.

This oscillation's frequency depends on IC_1's dc operating point, which varies with the LM134's temperature. The circuit's dc biasing values are such that a 0 to 100°C temperature excursion produces a 0- to 1-kHz output. In addition, a voltage of only 2V appears across the LM134, minimizing sensor errors related to power dissipation.

For interfacing purposes, the differentiator/transistor network at IC_1's output provides a TTL-compatible output. To calibrate this circuit, place the LM134 in a 0°C environment, and trim the 0°C adjustment for a 0-Hz output. Then put the sensor in a 100°C environment and set the 100°C adjustment to a 1-kHz output. Repeat this process until both points are fixed. When properly constructed and calibrated, this circuit achieves a stable 0.1°C resolution with 1°C accuracy.

If you prefer thermocouples to IC temperature sensors, consider the temperature/frequency converter shown in **Fig 2,** which uses the popular type K thermocouple. That sensor's extremely low output (41.4 μV/°C) and the requirement for cold-junction compensation make it one of the most difficult transducers to digitize directly. This approach uses the 50-nV/°C input offset drift of the LTC1052 chopper-stabilized amplifier (IC_1). Besides providing cold-junction compensation for the thermocouple over a 0 to 60°C range, the design achieves ±1°C accuracy with 0.1° resolution.

In this approach, the thermocouple biases IC_1's positive input. IC_1 then drives a crude V/F converter (IC_2) comprising several 74C04 inverters and associated circuitry. Each V/F output pulse causes the 100-pF capacitor to dispense a fixed charge into the 1-μF capacitor via the LTC1043 switch. The larger capacitor integrates the charge packets and produces a dc voltage at IC_1's negative input. That amp's output forces the V/F converter to run at a frequency that balances its inputs. This feedback action eliminates drift and nonlinearities in the V/F converter, and the output frequency is a function only of the dc conditions at the amp's inputs.

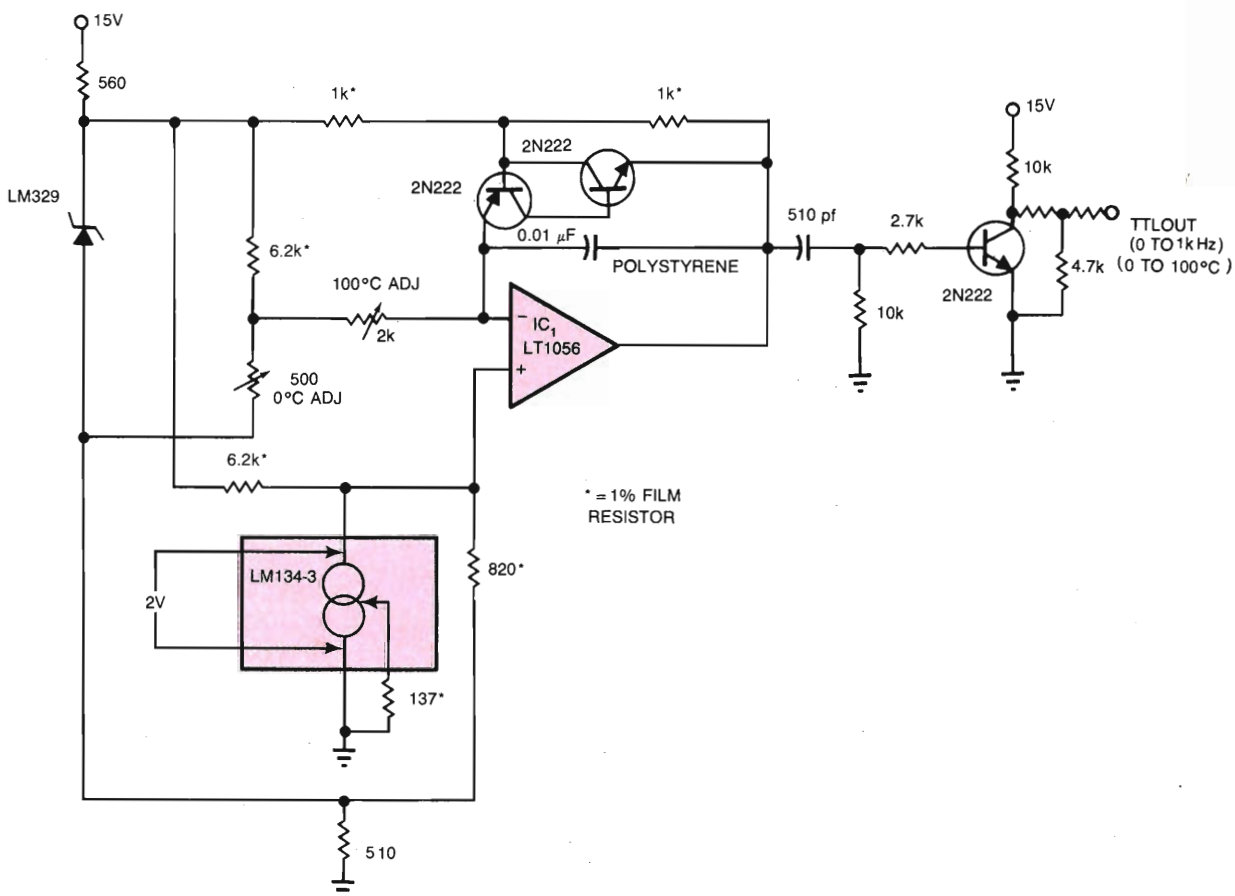
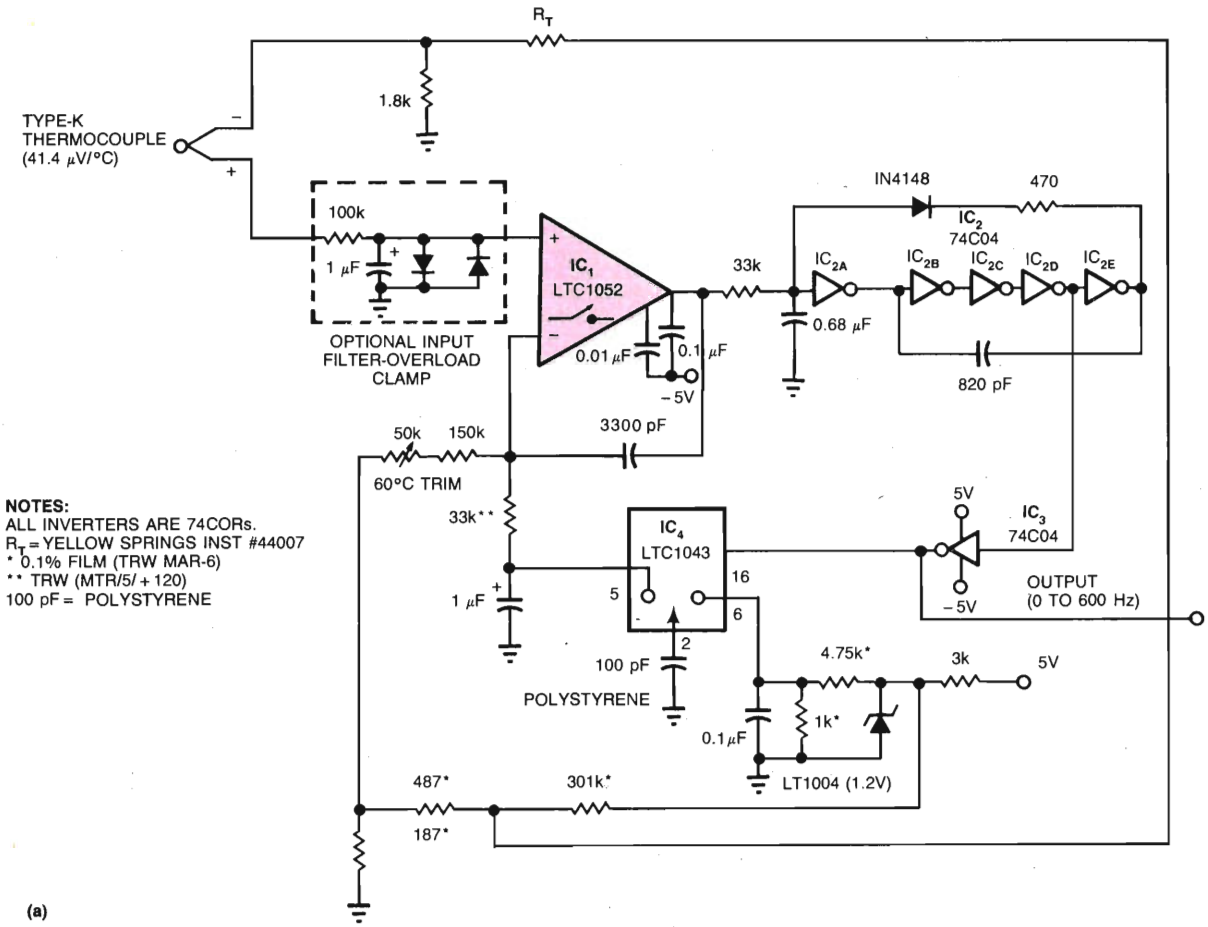
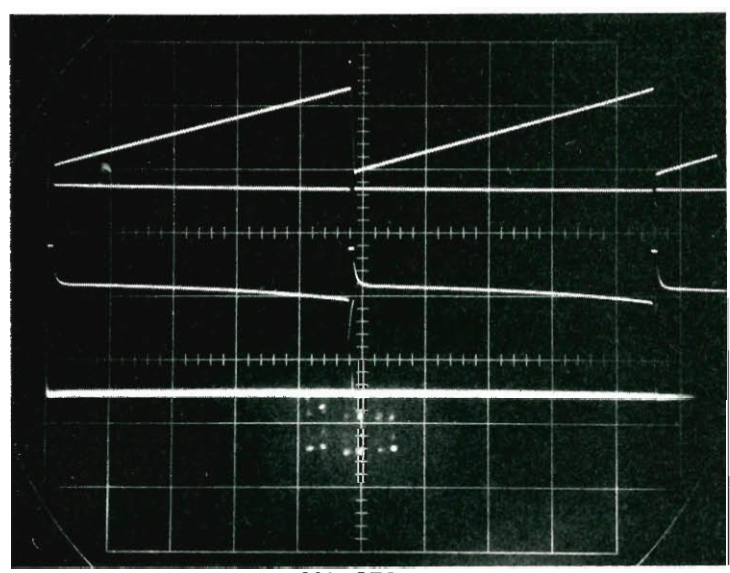


Fig 1—IC_1's dc operating point *determines oscillation frequency, causing the transistors to toggle and produce an output that corresponds to the sensor's temperature. This design directly digitizes the sensor's output and maintains 0.1°C resolution with 1.0°C accuracy.*



(a)



(b)

Fig 2—The low output levels and cold-junction compensation requirements *of K thermocouples render those devices' outputs tough to digitize directly. This circuit relies on IC_1's low input offset drift to accomplish that task. The thermistor and several resistors perform the cold-junction compensation and offsetting functions.*

Sensor outputs are much lower than typical A/D LSB size

To stabilize the feedback loop, the 3300-pF capacitor forms a dominant response pole for IC_1. Furthermore, the amp's low drift eliminates offset errors in the circuit, despite an LSB value of only 4.14 μV (per 0.1°C).

To effect cold-junction compensation for the K thermocouple, thermistor R_T and the 1.8-kΩ, 187Ω, 487Ω, and 301-kΩ resistors form a compensation network that's biased from the LT1004's 1.2V reference. In addition to cold-junction compensation, the network provides offsetting so that a 0°C sensor temperature yields a 0-Hz output.

Ramp frequency varies with temperature

Fig 2b details circuit operation. IC_1's output drives the 33-kΩ/0.68-μF combination, which produces a ramp (trace A) across the capacitor. When the ramp crosses inverter IC_{2A}'s threshold, the cascaded inverter chain switches to produce a low output at inverter IC_{2E} (trace B). This action causes the 0.68-μF capacitor to discharge through the diode, resetting the capacitor to 0V. To ensure a clean reset, the 820-pF unit sends positive ac feedback to IC_{2B}'s input (trace C). This ramp/reset sequence's frequency varies with IC_1's output, which varies with the temperature at the sensor.

The inverter not located in the V/F converter's chain (IC_3) controls the LTC1043 switch and thereby closes the loop around the amp. When IC_3's output is High, the switch connects pins 2 and 6, allowing the 100-pF capacitor to receive charge from the LT1004's 1.2V reference. When IC_3 goes Low, the switch connects pin 2 to pin 5, and the 100-pF capacitor completely discharges (trace D) into the 1-μF unit. Because the amount of charge the capacitor delivers is constant for each cycle (Q=CV), the voltage to which the 1-μF capacitor charges is a function of frequency and discharge-path resistance.

This voltage is summed with the LT1004-derived offsetting potential at IC_1's negative input, thus closing the amplifier loop. The −120-ppm/°C drift of the 100-pF, charge-dispensing polystyrene capacitor is compensated by the opposing temperature coefficient of the resistors in the 1-μF capacitor's discharge path. This selection achieves a typical circuit gain drift of 20 ppm/°C, allowing less than 1 LSB (0.1°C) output drift over a 0 to 70°C ambient operating range.

The thermocouple's characteristics, combined with IC_1's low offset and the components specified for the cold-junction/offsetting network, eliminate the need for zero trimming. You calibrate the circuit by placing the thermocouple in a 60°C environment and adjusting the 50-kΩ potentiometer for a 600-Hz output. Beyond 60°C, the cold-junction network departs from the thermocouple's response, and output error increases rapidly. And, although the digital output varies with thermocouple temperature over hundreds of degrees, you must still linearize the system with a monitoring processor.

Finally, note that this circuit directly converts any low-level, single-ended signal. By removing the offsetting/cold-junction network and tying the 50-kΩ potentiometer to ground, you can apply inputs to IC_1's positive terminal as well. The design then produces an output that's accurate to 10 bits with a full-scale range of only 1 mV (1 μV/LSB). Furthermore, IC_1's high-impedance input allows you to filter or clamp input signals without introducing error.

The circuits discussed thus far all use standard temperature transducers, but they have difficulty in handling such extreme conditions as wide temperature ranges. The circuit shown in **Fig 3** uses an unusual transducer that accommodates a wide input range; it measures temperature by exploiting the relationship between the temperature and the speed of sound in a medium. The equation representing this relationship is

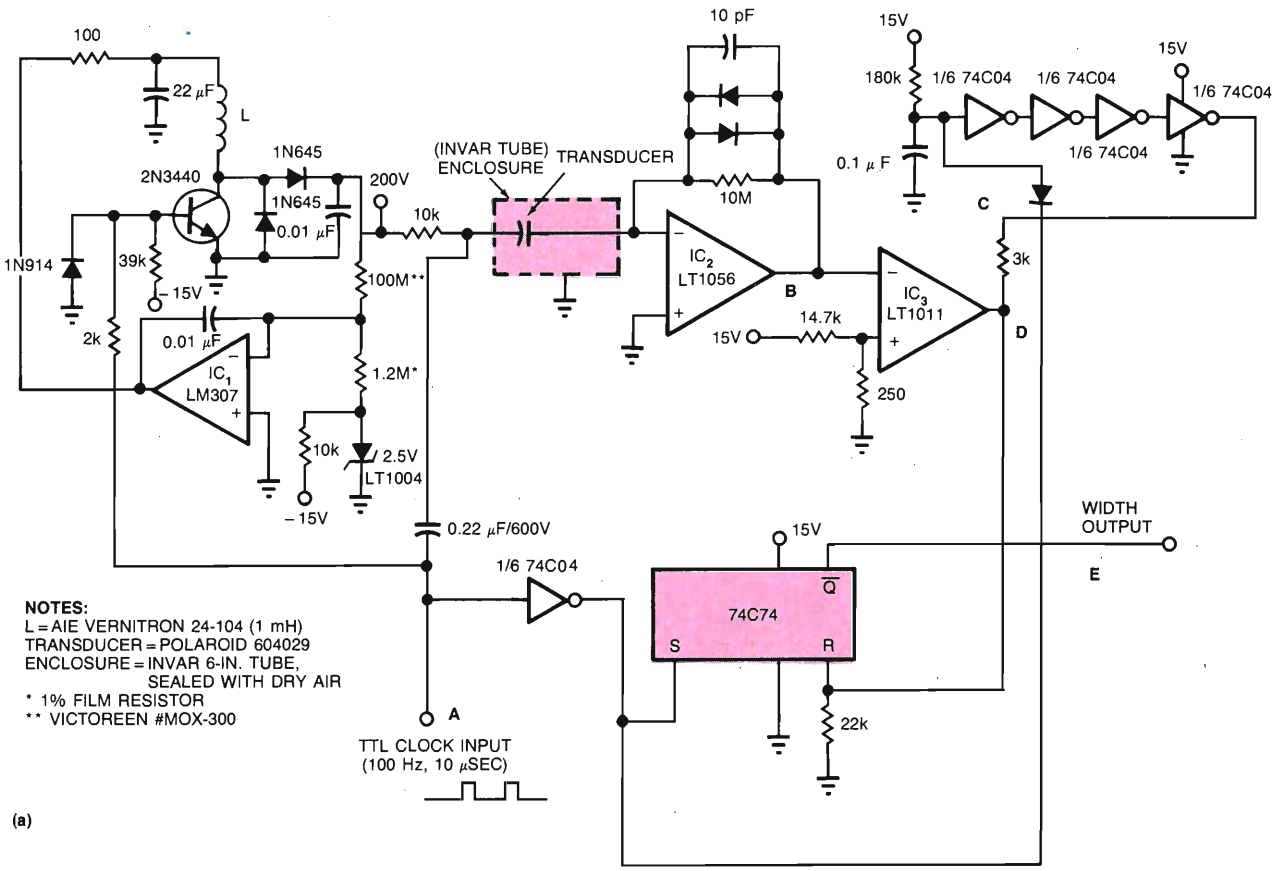
$$C = 331.5\sqrt{\frac{T}{273}}\ \text{M/SEC},$$

where C is the speed of sound and T is expressed in degrees Centigrade. Such acoustic thermometry finds uses, for example, in cryogenics and nuclear reactors. In addition, you can build acoustic temperature standards by operating the acoustic transducer in a sealed, known medium.

An acoustic thermometer's inherent time-domain operation suits direct digitization. In **Fig 3a**'s circuit, IC_1 and the inductor form a simple flyback, regulated 200V source that biases the acoustic transducer, which is a Polaroid ultrasonic element. You mount the transducer at one end of a sealed, 6-in.-long Invar tube; the Invar material minimizes mechanical tube deformation that occurs as a function of temperature. The medium inside the tube is dry air. In this configuration, you may think of the ultrasonic element as a capacitor, composed of an insulating disk with a conductive coating on each side.

The circuit operates in this fashion: Each time the TTL clock (trace A in **Fig 3b**) goes High, the transducer receives ac drive from the 0.22-μF capacitor. This drive causes the disk to move and emit ultrasonic energy. Simultaneously, the clock input sets the 74C74 flip flop's output (trace E) Low and pulls the 0.01-μF capacitor to ground. This discharge cuts off drive to the comparator IC_3's 3-kΩ output pullup resistor (trace C), forcing its output (trace D) to zero.

When the clock's output is positive, IC_2 saturates (trace B). When the clock pulse returns to zero, IC_1 amplifies in a linear manner. The ultrasonic transducer now acts like a capacitance microphone, with the 200V



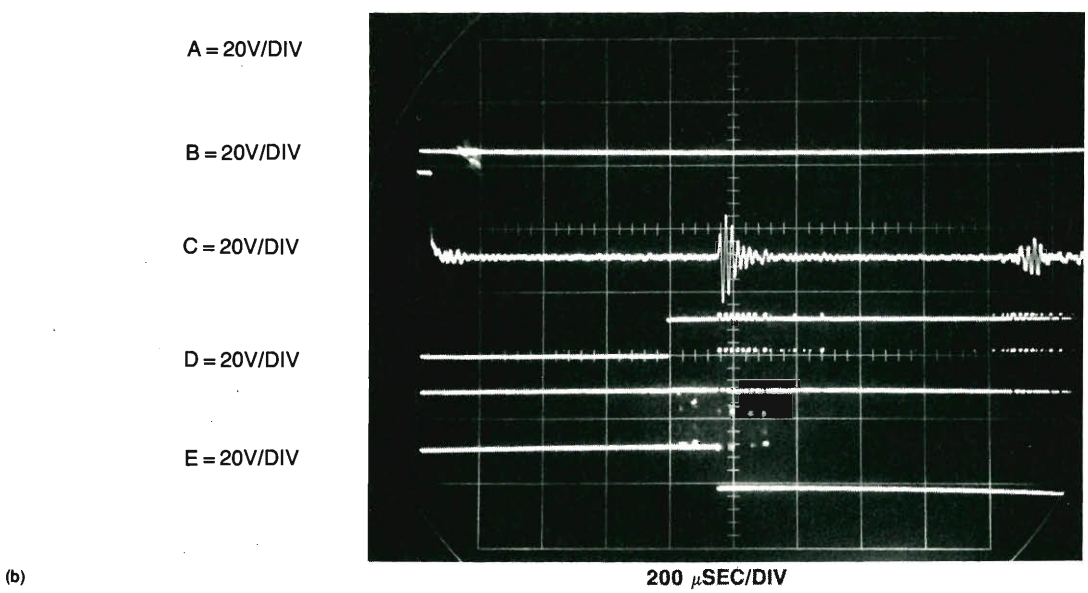


Fig 3—An ultrasonic sensor *measures temperature by exploiting the relationship between the speed of sound in a medium and temperature. The sensor uses an ultrasonic element as its active transducer element. The flip flop's output pulse width varies with temperature, and you can use digital circuitry to convert it to temperature information.*

supply providing bias voltage. Residual disk ringing now appears at IC_2's output, but it can't trigger IC_3, because the 0.01-μF capacitor hasn't charged high enough to allow the inverter chain's output to bias IC_3's output pullup resistor.

The emitted ultrasonic energy travels down the tube, bounces off the far end, and heads towards the transducer. Before the energy returns, though, the 0.01-μF capacitor's potential crosses the inverter's threshold, and the inverter chain applies 15V to IC_3's 3-kΩ resistor (trace C). Upon returning, the sonic energy mechanically displaces the transducer to force a capacitance shift. This shift causes a charge displacement into IC_2's summing point, and the amp's output responds with an amplified version of this signal (trace B). IC_3's output (trace D) now triggers and resets the flip flop, whose output pulse (trace E) represents the transit time down the tube. This time varies with temperature according to the earlier equation, and a processor can convert the pulse width into temperature information.

You can see the second return bounce, which is lower in amplitude, at the extreme right side of trace B. Also note the increased detected noise level after the first bounce returns; this noise is caused by sonic-energy dispersion inside the tube. The transducer picks up energy that's phase shifted from the desired signal and deflected from the tube walls. IC_3 responds to these unwanted signals, but the circuit's final pulse output is unaffected. In addition, the time-window gating supplied to IC_3's pullup resistor greatly reduces the likelihood of false triggering that may be caused by noise coming from outside the tube.

No strain to measure force

One final example deals with another common transducer variable: force. Strain-gauge transducers, which typically handle pressure or force, are often bridge-based sensors that produce full-scale outputs of 3 mV/V of bridge drive. **Fig 4** shows one way to digitize directly a strain-gauge bridge's output to 10-bit accuracy, although the bridge's differential output complicates the required converter input structure. With this resolution, you achieve a 25-μV LSB increment for a 7.5V bridge drive, which is considerably larger than that of the thermocouple examples but is still far below the requirements of conventional A/D converters.

IC_1 and the 2N2905 transistor drive the bridge. One of the bridge's outputs connects to IC_1's negative input, and that amp drives the transistor to bias the bridge at a voltage that brings its negative input to ground potential. Voltage drops from the diodes in the bridge's −5V return line allow the transistor to force the voltage on the bridge's positive end high enough to balance IC_1's inputs. This arrangement permits sensing of the bridge's other output in a single-ended, ground-referred fashion. Although a slight error exists because of IC_1's offset voltage, you eliminate it by referring the converter's input to IC_1's negative input rather than to ground.

The design's A/D converter, which uses a current-balancing technique, consists of IC_2, a flip flop, and some gates. Again, you rely on the chopper-stabilized LTC1052's 50-nV/°C input drift to implement the low-level input A/D function. To examine the circuit's operation, assume that the flip flop's Q output (trace B in **Fig 4c**) is Low and connects LTC1043 pins 11 and 12 to pins 7 and 13, respectively. The main current switch passes no current because a 3.3-MΩ resistor is placed across IC_2's inputs. The current-loading compensation switch also puts a 3.3-MΩ value across the 1-kΩ divider/resistor, reducing the voltage across it by 0.03%.

Under these conditions, the only current into IC_2's summing point comes from the bridge via the 470-kΩ resistor. This positive current forces IC_2's output (trace A) to integrate negatively. This ramp continues and finally passes the flip flop's switching threshold. At the next clock pulse (trace C), the flip flop changes state (trace B) and causes the LTC1043 to reverse switch positions. At this point, the 3.3-MΩ resistor controlled by the current-loading compensation switch disconnects from the 1-kΩ resistor, but the 3.3-MΩ value controlled by the main current switch replaces it. The 0.03% loading of the 3.3-MΩ resistor, combined with this switching scheme, eliminates sags or loading effects across the 1-kΩ resistor during switching. As a result, a quickly rising, precise current flows from IC_2's summing point.

This current, scaled to be greater than the bridge's maximum output, forces IC_2 to integrate positively. Switching occurs at the first clock pulse that appears after IC_2's output has crossed the flip flop's triggering threshold, and the entire cycle repeats. Because the reference current is fixed, the flip flop's duty cycle is a function only of the bridge's signal current into IC_2's summing point. The reference current comes from the bridge drive indirectly through the 22.3-kΩ/1-kΩ divider. Consequently, the A/D converter's reference current varies ratiometrically with the bridge output, eliminating errors caused by variations in bridge drive.

The flip flop's output gates the clock to produce output A (trace D). To eliminate spurious output pulses caused by flip-flop delay, the 10-kΩ resistor combines with the output gate's input capacitance to delay the clock signal slightly. To extract the circuit's data output (the ratio of output A to the clock frequency), you can use counters.

You must observe several facts when setting up and using this circuit. First, because the output is ex-

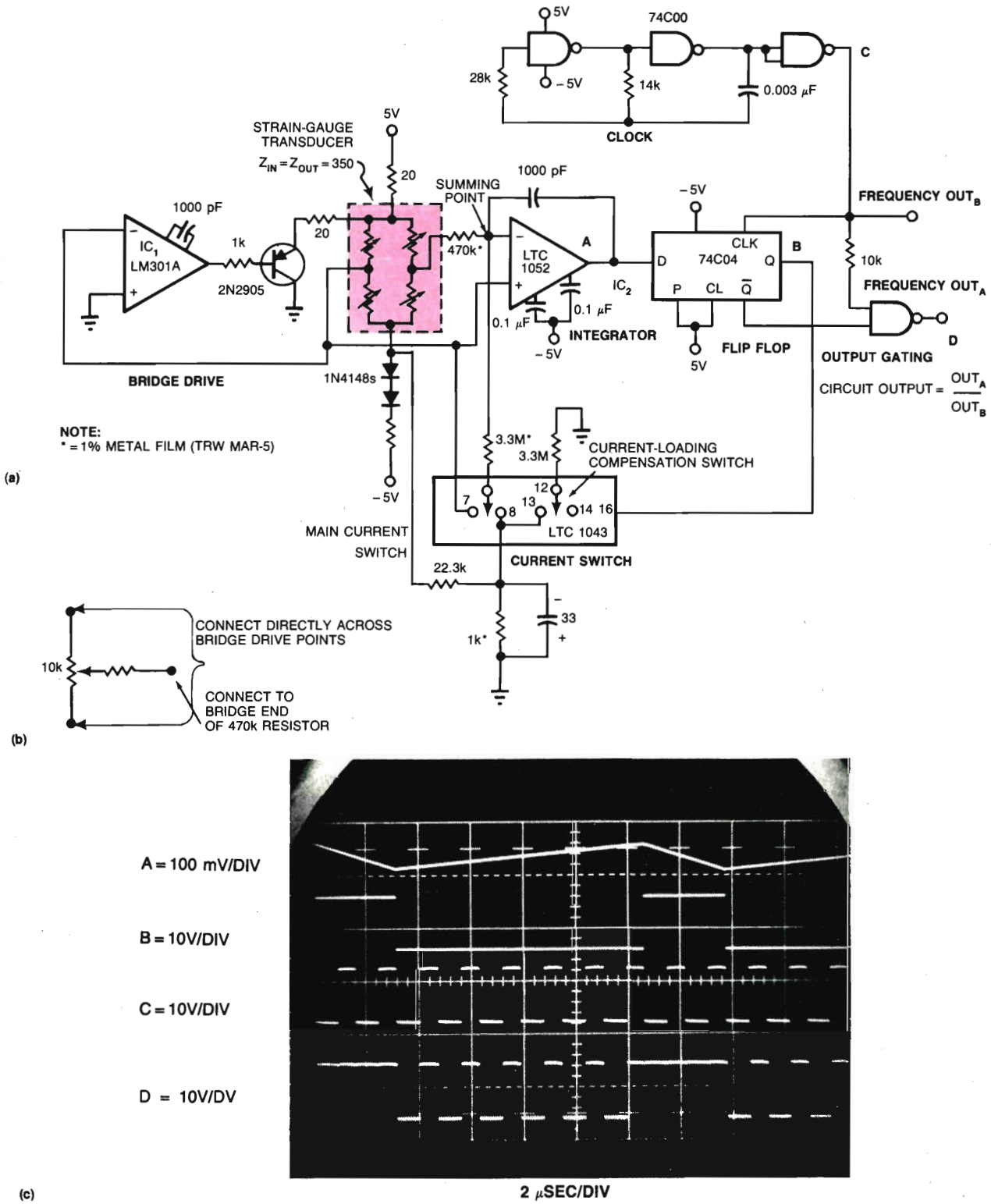


Fig 4—Although a strain-gauge bridge transducer's output *is larger than that of a thermocouple, it's still too small for most A/D converters. This direct-digitization circuit maintains 10-bit accuracy, and if your transducer requires it, you can accomplish transducer zero trimming with an optional network* **(b).**

pressed as a ratio, clock frequency stability is unimportant. Next, you select a 470-kΩ input resistor at IC_2 to produce less than 1-LSB loading error on the strain-gauge bridge, which receives only about 7.5V of drive because of the deliberate resistor and diode drops in its supply lines.

At a 3-mV output per volt of bridge drive, the full-scale signal is 22.5 mV, producing a current of 0.0225V/470 kΩ, or 48 nA. To maintain 10-bit accuracy, leakage and amplifier bias current into A_2's summing point must be less than 0.1% of this figure, or 48 pA. Although IC_2's bias current is much lower than this level, board leakage can cause trouble. Be careful during layout, and keep the board clean. The best way to do so is to use a Teflon standoff for all summing-point connections.

As another layout consideration, place the 470-kΩ and 3.3-MΩ resistors associated with IC_2's negative input as close as possible to the IC pin. Note also that the 3.3-MΩ current-summing resistor switches to IC_2's positive input when not sourcing the summing point. This seemingly unnecessary connection prevents small, stray 60-Hz and noise currents from coupling to IC_2's summing point when the current reference is off; not making this connection produces jitter in the LSB.

After laying out the circuit, you'll want to trim it. You can accomplish gain trimming by varying the 22.3-kΩ resistor. If your strain gauge requires zero trimming, use the optional network shown in **Fig 4b.** When properly trimmed, the circuit typically maintains 10-bit outputs within 1-LSB accuracy over the 0 to 70°C range. This small error arises primarily from the tracking errors of the starred resistors. **EDN**

Author's biography

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and -instrumentation design. He has served in related capacities at National Semiconductor Corp, Arthur D Little Inc, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. Jim is a former student of psychology at Wayne State University, and he enjoys tennis, art, and collecting antique scientific instruments.

Digitize transducer outputs directly at the source

Designers are searching for ways to digitize transducer outputs at the transducer itself. In Part 1 of this series, we described some circuit-design techniques that did the job for pressure and force transducers. Other physical properties—humidity, light, level, and acceleration—are subject to such design innovations as well.

Jim Williams, *Linear Technology Corp*

Digitizing transducer outputs far up in the signal chain is highly desirable—but tricky. Part 1 of this 2-part series demonstrated that it's possible to digitize directly at the transducer, without resorting to dc preamplification. It then described circuits that digitize the outputs of such common transducers as those that measure temperature and force. This second installment examines methods of digitizing outputs of transducers that detect light, humidity, surface levels, and acceleration.

Because of their extremely wide dynamic range, photodiodes generate outputs that are particularly difficult to digitize. High-quality devices furnish linear current outputs over a 100-dB range, and directly digitizing these outputs while maintaining that dynamic range would require 17-bit A/D converters as well as current/voltage input amplifiers. To mitigate the effects of this restriction, one common alternative approach calls for the compression of the diode's output with a logarithmic current/voltage input amplifier. This approach allows you to use a lower-resolution A/D converter, saving you the cost of a 17-bit A/D converter. However, nonlinear outputs aren't convenient to work with, and log amps respond slowly and can degrade performance in some photometric measurements.

The circuit shown in **Fig 1a** provides another alternative. It directly converts a photodiode's current output to a frequency output that has a 100-dB dynamic range. An optical input of 20 nW to 2 mW produces a linear, calibrated output of 20 Hz to 2 MHz. The circuit responds quickly to input steps, yet it costs little to implement.

Modified I/F converter does the trick

In operation, the photodiode's output current feeds a modified high-frequency version of a Pease charge-pump I/F converter. The output current biases amplifier IC_1's negative input, causing the amp's output (**Fig 1b,** trace A) to ramp down. When IC_1's output crosses zero, comparator IC_2's output (trace B) goes low. (The comparator's high-frequency response is aided by the 200-pF/1.8-kΩ network at the positive input.) The LT1009 diode and its associated diode bridge limit IC_2's output to −3.7V. When IC_2's output goes low, it also provides ac positive feedback to its positive input (trace D). Additional ac positive feedback comes from transistor Q_3's collector (trace C).

During this interval, the 47- and 5-pF capacitors pull charge from IC_1's summing point (trace E). This action causes IC_1's output to switch rapidly in a positive

Aimed at light-sensing applications, an I/F circuit converts a photodiode's output current to a frequency signal with a 100-dB dynamic range.

direction, and this event in turn switches IC_2 after the positive feedback around it has decayed. Now the LT1009 and its associated diode bridge limit IC_2's output to +3.7V. As the capacitor pair receives charge, IC_1's summing junction recovers, and the entire cycle repeats at a frequency linearly related to photodiode output current.

While D_1 and D_2 compensate the bridge diodes, transistor Q_1 compensates transistor Q_2. These two transistors, connected as diodes (Q_2 operates as a steering diode), provide lower leakage current than standard components. Comparator IC_3 provides protection against circuit latchup—a precaution made necessary by the circuit's ac-coupled feedback loop. If latchup occurs, IC_1's output saturates low, causing IC_3's emitter-follower-connected output to go high. This change forces IC_1's output positive and initiates normal circuit operation.

The LT1021-10 reference biases the photodiode to obtain optimum optical response. To trim this circuit, place the photodiode in a *completely* dark environment. Trim the dark-current adjust control so that the circuit oscillates at the lowest possible frequency—typically 1 to 2 Hz. Next, apply or electrically simulate a 2-mW optical input and trim the 5-pF adjust control for a 2-MHz output. If the adjustment falls outside the trimmer's range, alter the 47-pF capacitor's value. Once calibrated, this circuit maintains 1% accuracy over the photodiode's 100-dB range, and photodiode characteristics—and not the circuit—limit accuracy. **Fig 1c** shows the circuit's dynamic response to a fast light pulse (trace A); note that the frequency output settles within 1 μsec on both edges.

Humidity transducers pose problems

One the most difficult physical properties to detect electronically is relative humidity. The circuit shown in **Fig 2a** incorporates a recently introduced humidity transducer that transmits readings of relative humidity (RH) as a linear function of capacitance shift. The transducer features a nominal ±1.7-pF/%RH shift; a 500-pF value corresponds to RH=76%, and the transducer doesn't require temperature compensation. When conditioning its signals, however, note that the average voltage across it must be 0V; no net voltage may be applied to it.

The circuit converts the RH transducer's capacitive shifts directly into a calibrated frequency output. The LTC1043 switched-capacitor IC has an internal clock, and because it runs free at 150 kHz, it switches, via pin 2 (**Fig 2b,** trace A), between the LT1004 negative reference and IC_1's summing junction. (The 1-μF/22-MΩ combination ensures that no dc signal component is applied to the transducer.) Two states are therefore possible: When pin 2 connects to pin 6, the transducer receives a negative charge; when pin 2 connects to pin 5, the transducer's charge goes into IC_1's summing point.

IC_1's input (trace B, just faintly visible) shows transducer current, while trace C is IC_1's output. Functioning as an integrator, IC_1 ramps up in steps as successive packets of charge appear at its summing point. Concurrently with this action, a second set of switches (pins 7, 11, 8, 13, 12, and 14) synchronously transfers a fixed charge of opposite polarity into IC_1's summing junction. The amount of this fixed charge cancels the sensor offset (for instance, 0% RH doesn't extrapolate to 0-pF sensor capacitance). Consequently, the slope of the stepped ramp at IC_1's output varies with the sensor's value minus its offset term.

IC_1's output continues to ramp up until it equals the voltage at comparator IC_2's negative input and triggers IC_2's output high (trace D). AC-positive feedback holds IC_2's output high long enough for the 2N4393 FET to discharge IC_1's feedback capacitor. Then IC_1's output drops to zero, and the entire cycle repeats. The frequency of repetition is a function of the RH transducer's capacitance.

Low dependency on temperature

The LTC1004 reference provides an input voltage for IC_2, while the LTC1043's pins 3, 18, and 15 and the 330-pF capacitor form a simple charge pump that biases IC_3's summing point. IC_3's output assumes the value required to keep its summing point at zero. The 0.22-pF capacitor across IC_3 integrates that amp's response to dc, and the feedback resistors establish its operating point. Because IC_3's output voltage determines ramp height, these feedback resistors set the circuit's gain slope. The time and magnitude expansions in traces A_{EXP}, B_{EXP}, and C_{EXP} detail the effects of the transducer's charge dumping on IC_1's output ramp.

Temperature dependency in this circuit is low because the −120-ppm drifts of the 330-pF and 0.01-μF polystyrene capacitors (both gain terms) cancel ratiometrically. Further ratiometric error cancellation occurs because the transducer's charge source and IC_3's output voltage both come from the LT1004 reference. The only uncompensated term in the circuit, the 470-pF capacitor that supplies the offsetting charge, has a

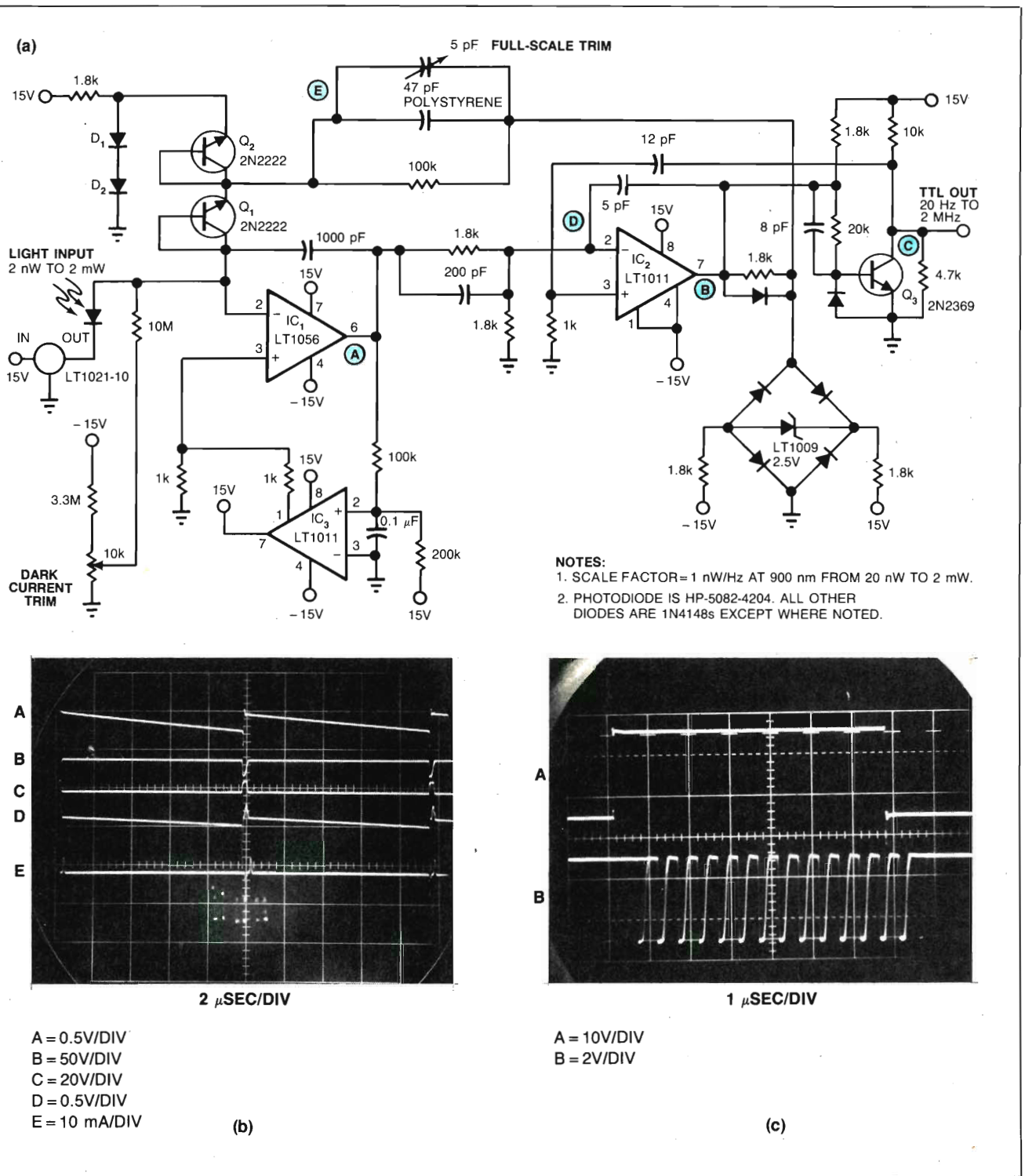


Fig 1—This circuit (a) directly converts the current output *of a photodiode into an output frequency with 100 dB of dynamic range. Once calibrated, the circuit—a modified Pease charge-pump I/F converter—maintains 1% accuracy over the full range. Its frequency output settles within 1 μsec on both edges* ***(c).***

A variable-capacitance transducer forms the basis of a circuit that generates an output frequency proportional to relative humidity.

−120-ppm/°C drift that's well below the transducer's 2% accuracy specification. Circuit temperature independence is thus assured.

To calibrate this circuit, place the transducer in a 5% RH environment and adjust the 5% trim for a 50-Hz output. Next, place the transducer in a 90% RH environment and adjust the 90% trim for a 900-Hz output. By repeating this procedure until both points are fixed, you'll achieve relative-humidity accuracy of 2% over the 5 to 90% RH range. If RH standards aren't available, you can approximately calibrate the circuit by using fixed capacitors in place of the sensor. Ideal values are 5% RH=379.3 pF and 90% RH=523.8 pF. You should note that these values assume an ideal sensor, and that an actual device's values can deviate by 10%.

Another common physical property that lends itself to direct digitization is surface level. You'll find transducers that measure the angle of deviation from an ideal level in road-construction applications, machine tools, inertial-navigation systems, and other systems requiring a gravity reference.

A small tube, containing a partially conductive fluid and leaving a bubble that changes location with respect to level, forms an elegant, simple level transducer (**Fig 3a**). Electrodes are inserted in each end of the tube, and a common electrode penetrates the center. If the tube is level with respect to gravity, the bubble sits in the center, and respective resistance values between

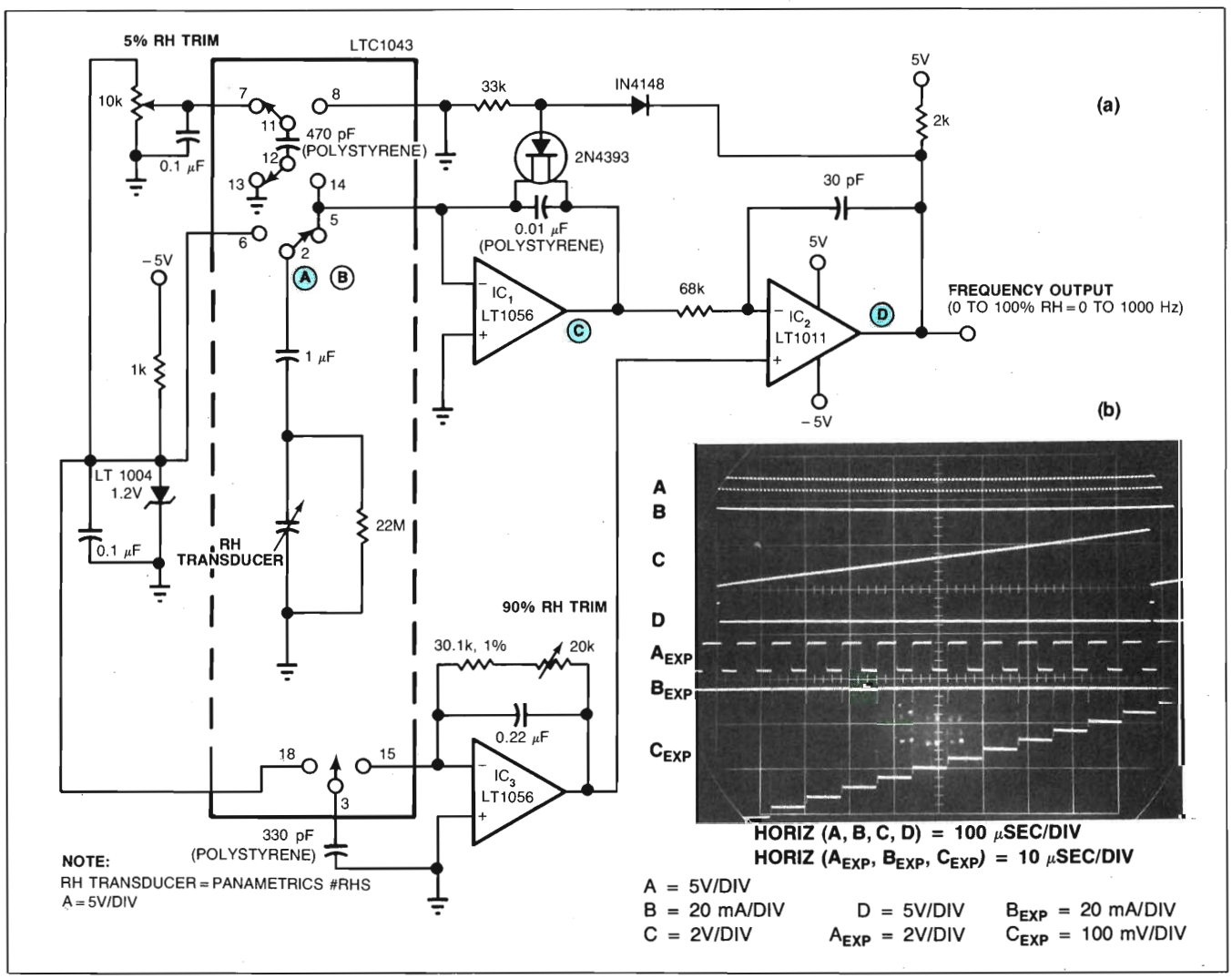


Fig 2—Tracking relative humidity as a function of linear capacitance shift, *the transducer in this circuit* ***(a)*** *requires no temperature compensation. Be sure to keep the average voltage across the device at 0V.*

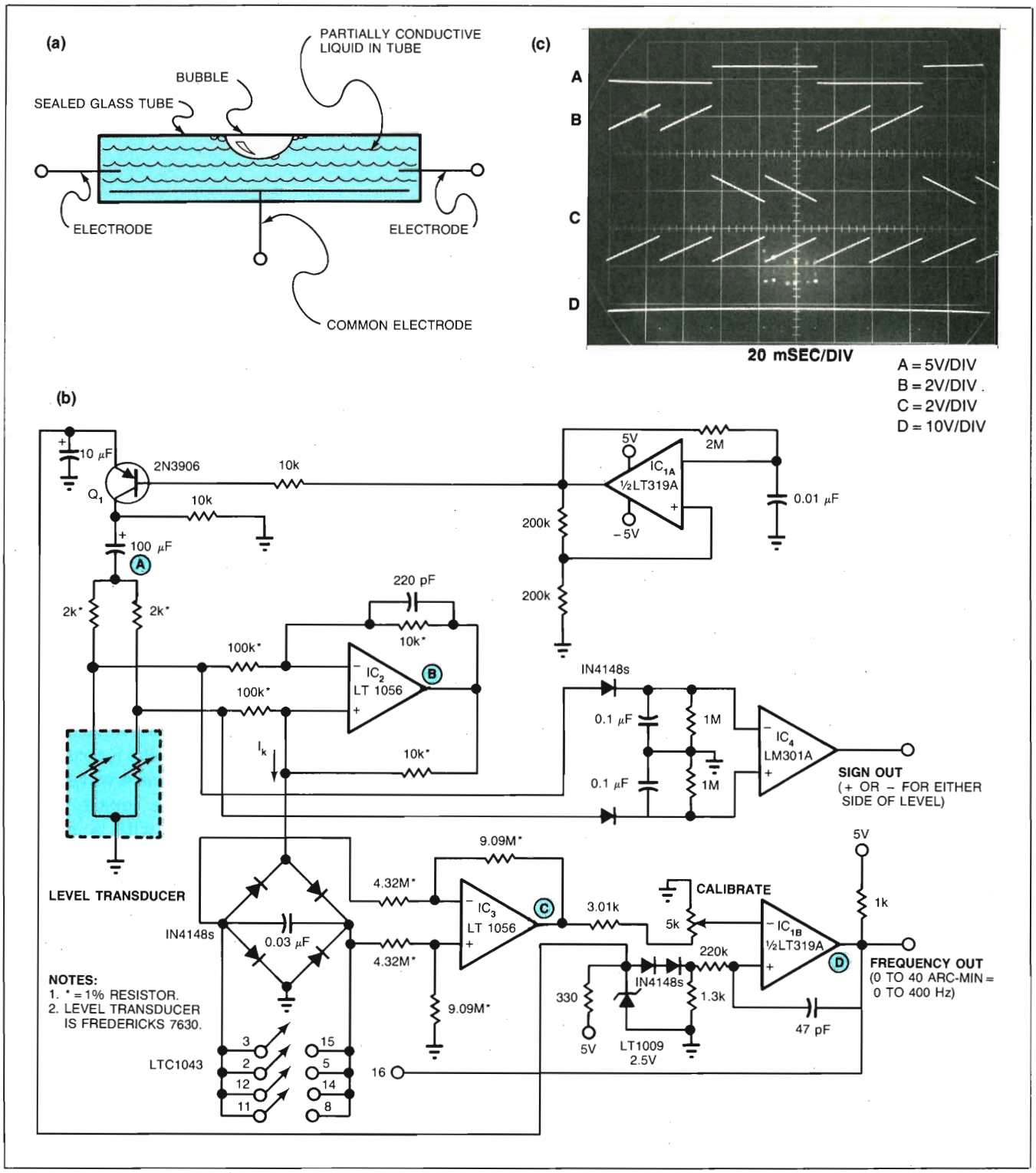


Fig 3—A simple level transducer (a) *contains partially conductive fluid and determines level according to the position of the bubble, which alters resistance values between the respective end electrodes and the common electrode. The transducer's attached circuitry* ***(b)*** *produces a calibrated frequency output corresponding to surface level.*

the common electrode and the two end electrodes are identical. As the tube shifts away from level, however, these resistance values change proportionally. By controlling tube shape, suppliers can produce units with linear output that you can incorporate into a bridge circuit.

To avoid damaging the tube's conductive liquid, you must excite it with an ac waveform. The transducer circuit then must generate this excitation as well as extract angle information and determine polarity (ie, determine in which direction the level has shifted). **Fig 3b** shows a circuit that directly produces a calibrated frequency output corresponding to level. A sign bit, also supplied at the output, gives polarity information.

The level transducer consists of two 2-kΩ resistors in a bridge that takes ac excitation from IC_{1A} (which is

An elegant level transducer employing a curved tube and conductive liquid measures a surface's angle of deviation from the horizontal.

configured as a multivibrator) in the following manner: IC_{1A} biases Q_1, which switches the LT1009's 2.5V potential through the 100-μF capacitor to provide the ac drive. Then IC_2, operating as a Howland current pump, converts the bridge's differential-output ac signal into a current. This current, whose polarity reverses as the bridge's drive polarity switches, is rectified by the diode bridge. As a consequence, the 0.03-μF capacitor receives unipolar charge. IC_3, running at a differential gain of 2, senses the voltage across the capacitor and presents its single-ended output to IC_{1B}.

When the voltage across the 0.03-μF capacitor becomes high enough, IC_{1B}'s output goes high and turns on the paralleled sections of the LTC1043 switch to discharge the capacitor. A 47-pF capacitor provides enough ac feedback to IC_{1B}'s positive input to allow a complete zero reset for the 0.03-μF capacitor.

Offset translates level to frequency

When the ac feedback ceases, IC_{1B}'s output goes low and the switch goes off. The 0.03-μF unit again receives constant current charging, and the entire cycle repeats. The magnitude of the constant current delivered to the bridge/capacitor configuration determines this oscillation's frequency; that magnitude depends on the transducer bridge's offset, which is related to level.

Fig 3c shows circuit waveforms. Trace A represents the bridge's ac drive, and trace B is IC_2's output. Note that when bridge drive changes polarity, IC_2's output rapidly switches polarity to maintain a constant current into the bridge/capacitor configuration. IC_3's output (trace C) is a unipolar, ground-referred ramp, and trace D shows IC_{1B}'s output pulse, which is the circuit's output.

The diodes at IC_{1B}'s positive input provide temperature compensation for the sensor's positive temperature coefficient, allowing IC_{1B}'s trip voltage to track bridge output over temperature ratiometrically. The sign output comes from IC_4, which operates without feedback and compares the rectified and filtered bridge-output signals with respect to ground.

To calibrate this circuit, place the level transducer at a 40-arc-min angle and adjust the 5-kΩ trimmer at IC_{1B} for a 400-Hz output. The transducer limits circuit accuracy to roughly 2.5%.

Accelerometers exploit ceramics

The final example concerns direct digitization of the outputs of piezoelectric accelerometers, which rely on the properties of ceramic materials to produce charge when mechanically excited. In such transducers, a mass is coupled with a ceramic element, which dispenses a charge when the mass experiences acceleration. The transducer's sensitivity and frequency response vary according to the device's mechanical design and the ceramic used.

The best way to condition a piezoelectric output is to unload it through a coaxial cable directly into the virtual ground of an op amp's summing point. This method ensures that there will be no voltage difference in the coaxial cable between its center conductor and its shield, and it thereby eliminates cable capacitance as a parasitic term—an important consideration in any charge-output transducer. Because the accelerometer produces ac outputs, a direct digitization of its output must include a sign bit as well as amplitude data.

Square-wave source is instructive

The circuit shown in **Fig 4a** accomplishes a complete direct A/D conversion of the piezoelectric accelerometer's output, and it will work with other devices in the same class. To understand the circuit, it's instructive to replace the accelerometer with a square-wave source coming through a resistor. When the square wave is positive, IC_1's integrator responds with a negative ramp output (**Fig 4b,** trace A). IC_2, also detecting the square wave's polarity, goes high, but the LT1009 and its associated diode bridge (trace B) limit the signal to +3.7V.

These two signals converge at IC_3's negative input, where IC_1's ramp output combines with the bridge's output. For stability, the series diodes provide temperature compensation for the bridge diodes. When IC_1's output goes negative to a specified point, IC_3's output (trace C) goes high. The two comparators control output gating: When IC_2's output is low and IC_3's is high, Q_1's gate (trace D) receives turn-on bias.

When Q_1 comes on, it discharges IC_1's feedback capacitor and resets IC_1's output to zero. Local ac-positive feedback at IC_3 ensures adequate time for a complete zero reset of IC_1's feedback capacitor. The 100-pF capacitor at IC_3's input aids high-frequency response. When the ac feedback decays, Q_1 goes off, IC_1 again ramps down, and the cycle repeats as long as the input square wave is positive. The frequency of oscillation is directly proportional to the current flowing into IC_1's summing point.

When the input square wave goes negative, IC_1 abruptly ramps up. Simultaneously, the output of IC_2's input-polarity detector goes negative and forces the

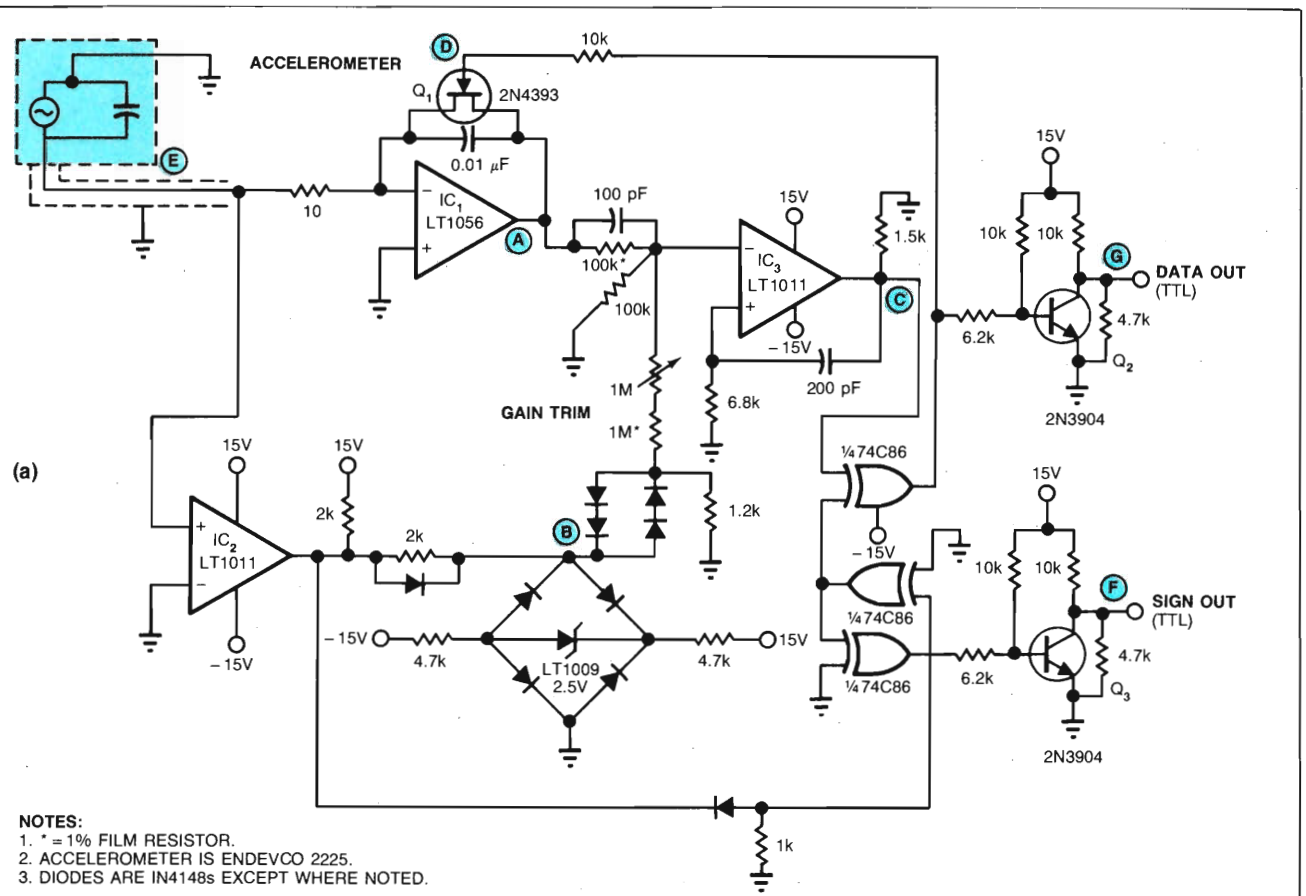


Fig 4—By replacing the accelerometer in this circuit (a) *with a square-wave source, you can more easily understand its operation. Direct digitization of a signal proportional to acceleration results when you return the piezoelectric accelerometer to the circuit. The waveforms in* **c** *show circuit response when you apply acceleration to the transducer.*

A piezoelectric accelerometer's ceramic elements release charge when excited.

LT1009 and its diode bridge's output negative. IC_3's output now switches when IC_1's output exceeds a positive limit. The output gating, directed by IC_2's polarity signal, inverts IC_3's output to supply proper drive to Q_1's gate. Q_1 turns on and resets the circuit. Consequently, the loop maintains oscillation, but with all signs reversed. The Q_2 and Q_3 level shifters supply TTL data outputs for sign and magnitude.

Insert accelerometer for digitization

The circuit described constitutes an I/F converter that responds to ac signals. If you now replace the square-wave source with a piezoelectric accelerometer, direct digitization results. **Fig 4c** shows circuit response when you apply an acceleration (trace E) to the transducer; in this case the response is a damped sinusoid. The sign bit (trace F) tracks acceleration polarity, while the frequency output supplies amplitude data.

Note the drop in output frequency as the input waveform damps. A monitoring process, sampling the sign and frequency waveforms faster than twice the highest frequency of acceleration, can extract the desired acceleration waveform data. To trim the circuit, apply a known amplitude acceleration and adjust the 1-MΩ gain trim at IC_3. As an alternative, you can electrically simulate the accelerometer using scale factors provided in accelerometer data sheets. **EDN**

Author's biography

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA) specializes in the design of analog circuits and instruments. He has served in related capacities at National Semiconductor Corp, Arthur D Little Inc, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. Jim is a former student of psychology at Wayne State University, and he enjoys tennis, art, and collecting antique scientific instruments.

Chopper-stabilized monolithic op amp suits diverse uses

Chopper stabilization produces op amps with lower time and temperature drifts than are possible with differential types. One such device improves upon previous specs. This article, first of a 2-part series, offers guidelines for optimizing such high-performance op amps. Part 2 will describe several applications for the new IC.

Jim Williams, *Linear Technology Corp*

For low dc offset and minimal time and temperature drifts, chopper-stabilized amplifiers have no rival. Nonetheless, a new monolithic chopper-stabilized op amp, Model LTC1052, improves upon previous monolithics in several areas. To use it most effectively, however, you must understand and combat various error sources.

The chopper amplifier's low drift, high gain, and high input impedance make it attractive in many demanding applications. These advantages, however, make the device proportionally more prone to external error sources than classic differential amplifiers. You can identify such error contributors, though, and minimize their detrimental effects in high-performance circuits.

Cool down thermal EMFs

To derive maximum benefit from the LTC1052's very low drift, you must pay considerable attention to dc parasitics—particularly thermal EMF. Any connection of dissimilar metals produces a potential that varies with the junction's temperature (the Seebeck effect). Thermocouples, for example, exploit this phenomenon to produce useful information. In low-drift amplifier circuits, thermal EMF is usually the primary error source.

Connectors, switches, relay contacts, sockets, wire, and even solder are candidates for thermal-EMF generation. Connectors and sockets can, of course, form

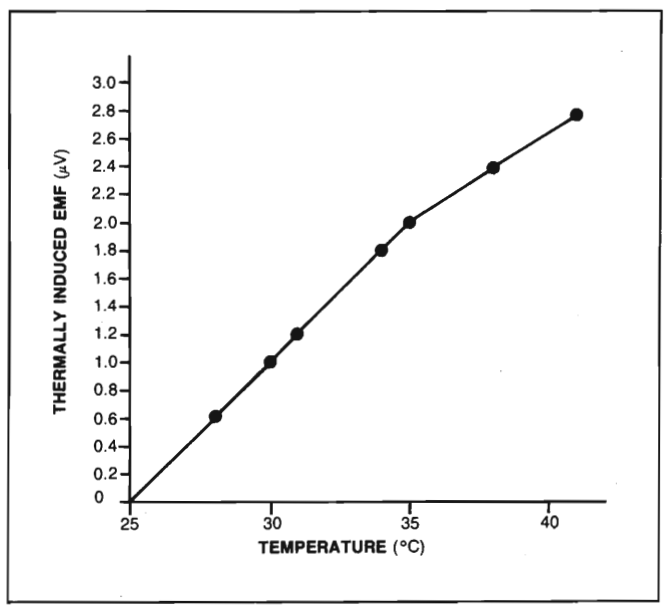


***Fig 1—Wire from two different manufacturers** can form a junction that generates thermal EMF. This empirically derived curve shows that a temperature rise of only 16°C above ambient causes a 2.8-μV thermally generated EMF in such a junction.*

Providing much lower offsets and drifts than classic differential op amps do, chopper-stabilized amplifiers use a carrier-modulation technique.

thermal junctions. In addition, junctions of wire from different manufacturers can easily generate 200 nV/°C —four times the LTC1052's drift specification. **Fig 1** shows a plot for such a wire junction. Solder, too, can become an error source at low levels by creating a junction with copper or Kovar wires or with pc-board traces (**Fig 2**).

You can minimize thermal-EMF-induced errors if you pay careful attention to circuit-board layout. In general, limiting the number of junctions in the amplifier's input-signal path is good practice. Avoid connectors, sockets, switches, and other potential error sources as much as possible. Of course, you can't always avoid them. In these instances, attempt to balance the number and type of junctions in the amplifier's inputs to achieve differential cancellation.

Deliberately create errors

Balancing junctions in an amplifier's inputs—in effect, deliberately creating errors—is a practice borrowed from standards-lab procedures. The practice can be quite effective in reducing thermal-EMF-originated errors. **Fig 3** shows a simple example in which a nominally unnecessary resistor is included to promote such thermal balancing. For such remote signal sources as transducers, connectors might be unavoidable. In these cases, choose a connector that's specified for relatively low thermal-EMF activity, and use a balanced approach in routing signals through the connector, along the circuit board, and to the amplifier.

If some imbalance is unavoidable, introduce a counterbalancing junction. In all cases, place the junctions in proximity to one another to keep them at the same temperature. Avoid drafts and temperature gradients that could introduce thermal imbalance. **Fig 4** shows the LTC1052 set up in a test circuit to measure the amplifier's temperature stability. The lead lengths of the resistors connected to the amplifier's inputs are identical.

The thermal capacity at each input is also balanced

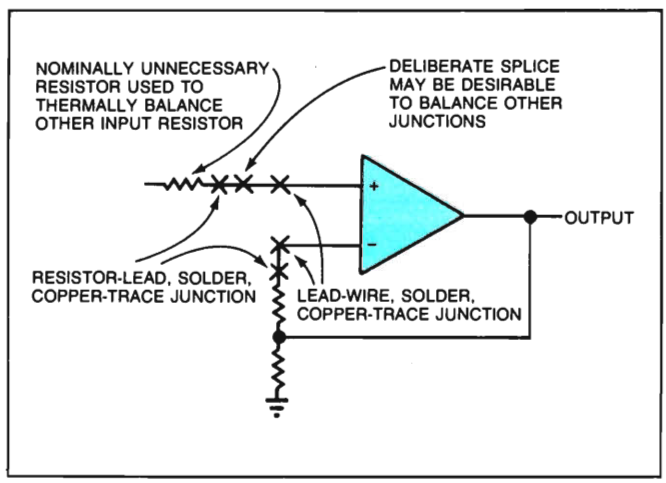


Fig 3—Fight fire with fire. *In some cases, you might need to introduce temperature-dependent voltage sources to compensate for unavoidable thermal-EMF sources. In this circuit, the nominally unnecessary resistor serves to match the temperature-varying impedances at the amplifier's inputs.*

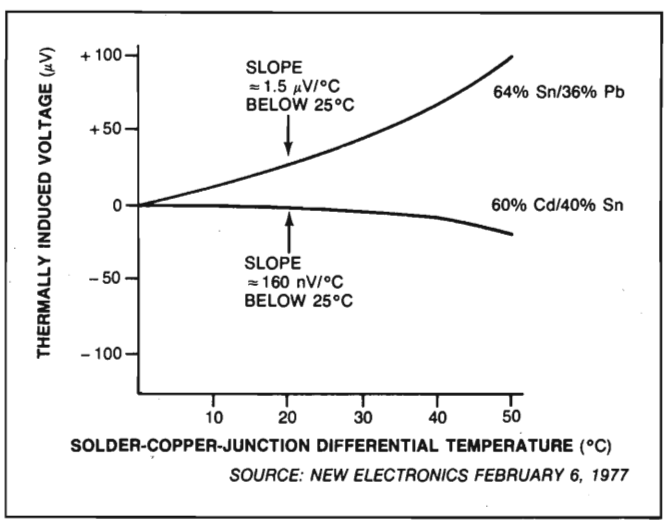


Fig 2—The junction of solder with other metals *can be a significant cause of thermally generated EMF. These curves show the voltages generated by joining two different solders with copper conductors.*

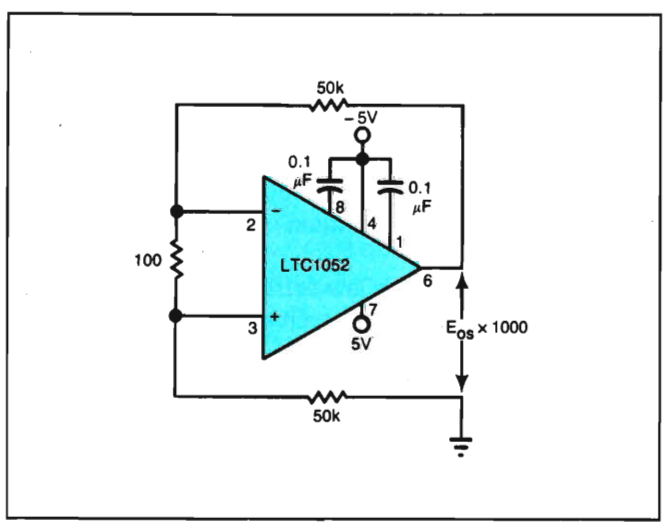


Fig 4—You can measure an amplifier's *offset-voltage stability with this simple test circuit. It's important to match the impedances at the amplifier's two input terminals.*

because of the symmetrical connection of the resistors and their identical size. Thus, thermal-EMF-induced shifts are equal in phase and amplitude and cancellation results. But slight air currents can still affect even this arrangement. For example, **Fig 5** shows a strip chart **(a)** of output noise generated by a test circuit **(b)** uncovered (upper trace) in supposedly still air and by one covered by a small styrofoam cup (lower trace). This data illustrates why it is often prudent to enclose the LTC1052 and its associated components in some form of thermal baffle.

Power-transformer fields cause errors

Thermal EMFs are the most likely, but not the only, potential low-level error source. Electrostatic and electromagnetic shielding could prove necessary to protect against power-transformer-field errors. Power-transformer fields are notorious sources of errors that are often mistakenly attributed to an amplifier's dc drift and noise. A circuit requiring that a transformer be mounted near the amplifier to effect high-quality grounding is particularly likely to suffer disturbances resulting from the transformer's magnetic field, which, impinging on a pc-board trace, could easily generate microvolts across that conductor. The amplifier cannot distinguish between this spurious signal and the desired input.

Attempts to eliminate the problem by rolling off amplifier gain with a feedback capacitor might work, but often the filtered version of the undesired pickup masquerades as an unstable dc component in the output. The most direct approach is to use shielded transformers, but careful layout could be equally effective and less costly. An RF choke connected across an oscilloscope probe can determine the presence and relative intensity of transformer fields, thereby aiding in layout experimentation.

Work around stray leakage currents

Another source of parasitic error is stray leakage current. The LTC1052's 30-pA bias current allows operation from very high source impedances. In such

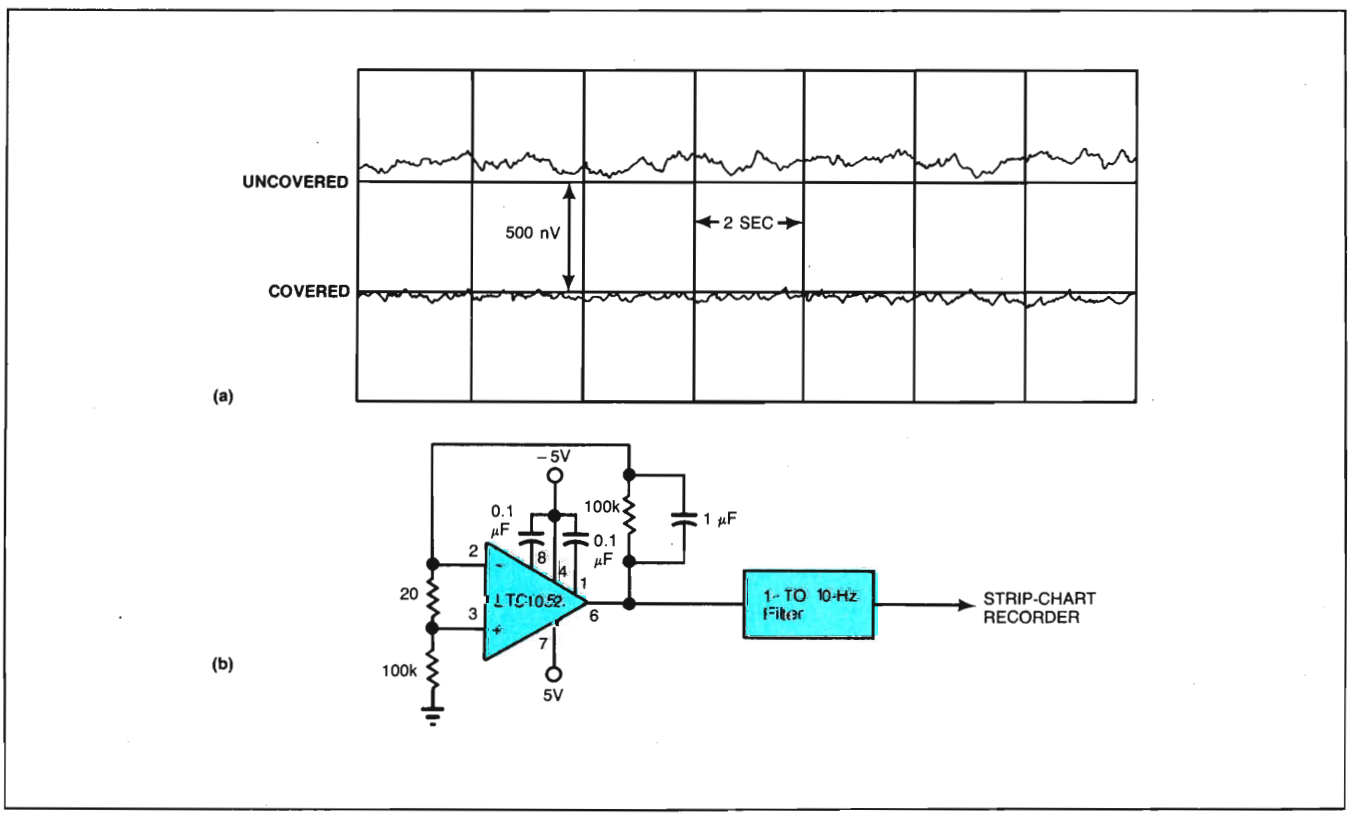


Fig 5—Still air is not so still, *as seen in this strip-chart recording* ***(a),*** *which characterizes a test circuit* ***(b).*** *The upper trace shows offset variations of about 200 nV p-p in an uncovered amplifier; the drift drops significantly if you shield the amplifier from the nearly imperceptible air currents that are always present.*

Choppers, chopper stabilization, and the LTC1052

The dc characteristics of op amps have improved significantly. Some of the carefully executed designs currently available provide submicrovolt offset temperature drift, low bias currents, and open-loop gains exceeding 10^6. Considerable design and processing advances were needed to achieve these specs. Yet in spite of this fact, amplifiers with even better dc specs were available in 1963 (Philbrick Research Model SP656).

The Philbrick amplifiers were large (about 3×2×1.5 in.) and expensive ($195) by modern standards, and they used relatively primitive components, but their dc performance anticipated today's best monolithic amplifiers. Their secret was the use of chopper-stabilization techniques instead of the more common differential dc-stage approach.

The chopper-stabilization approach (**Fig A**), developed by E A Goldberg in 1948, uses the amplifier's input to amplitude-modulate an ac carrier. This carrier, amplified and synchronously demodulated back to dc, supplies the amplifier's output. Because the dc input is translated to—and amplified as—an ac signal, the amplifier's dc parameters have no effect on overall drift.

This modulation and demodulation process is the reason why chopper-stabilized amplifiers are able to achieve significantly lower time and temperature drifts than classic differential types. In addition, the ac processing of the signal aids low-frequency amplifier-noise performance and eliminates the need for many of the careful design and layout procedures necessary in a classic differential approach.

The most significant tradeoff is increased complexity. The chopping circuitry and sampled-data operation of these amplifiers requires close attention for good results. In addition, the ac dynamics of chopper-stabilized amplifiers are complex if you need bandwidths greater than the chopping carrier frequency.

Referring to **Fig A,** the ac amplifier's input switches alternate between the signal input and the feedback divider network. The amplitude of the ac amplifier's output represents the difference between the feedback signal and the input. This output is converted back to dc by a phase-sensitive demodulator composed of a second switch, driven synchronously with the input switch.

The output-integrator stage smoothes the switch's output to dc and presents the final output. Drifts in the output integrator are of little consequence, as this stage is preceded by the ac gain stage. The dc drifts in the ac stage are also inconsequential, because the coupling capacitors isolate the drifts from the rest of the amplifier.

Overall dc gain, the product of the gain of the ac stage and the dc gain of the integrator, is very high. Although the approach in **Fig A** easily limits drifts to 100 nV/°C and yields open-loop gains of 10^8, the method is not without drawbacks. For instance, the amplifier has a single-ended, noninverting input and can't accept differential signals without the aid of additional front-end circuitry.

Moreover, the carrier-based approach constitutes a sampled-data system; thus, overall amplifier bandwidth is limited to a small fraction of the carrier frequency. The carrier frequency, in turn, is restricted by ac-amplifier gain and phase limitations and errors induced by switch re-

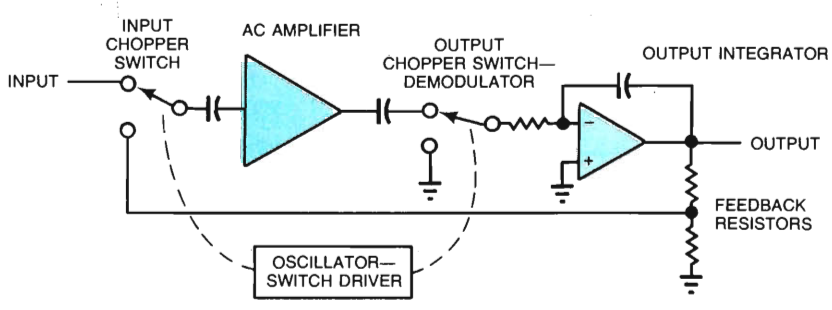


Fig A—This basic chopper-stabilization configuration *involves modulating an ac carrier by the input voltage. The output stage demodulates (rectifies) this carrier; the integrator stage smoothes the resulting dc voltage.*

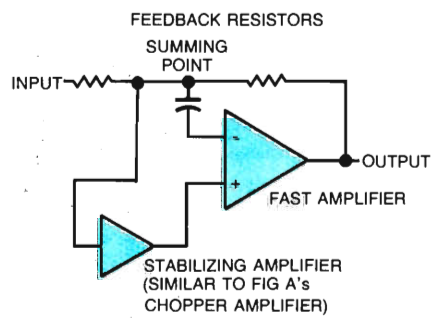


Fig B—Enhancing the speed of Fig A's basic chopper circuit, *this configuration uses a parallel-path approach. The chopper block forces the fast amplifier's summing point to zero and amplifies low-frequency signals; fast signals drive the fast amplifier directly. For best results, the two amplifiers' high- and low-frequency rolloffs should coincide.*

sponse time. Maintaining good dc performance involves keeping the effects of these considerations small by setting carrier frequencies in the low kilohertz range.

Solving the bandwidth problem

The classic chopper-stabilized amplifier solves the chopper amplifier's low-bandwidth problem. It uses a parallel-path approach (**Fig B**) to provide greater bandwidth while maintaining good dc characteristics. The stabilizing amplifier, a chopper type, biases the fast amplifier's positive terminal to force the summing point to zero.

Fast signals drive the ac amplifier directly, while the stabilizing amplifier handles the slow signals. To achieve smooth overall gain-frequency characteristics, the fast amplifier's low-frequency cutoff must coincide with the stabilizing amplifier's high-frequency rolloff.

With proper design, the chopper-stabilized approach yields bandwidths of several megahertz and provides the low drift characteristic of a chopper amplifier. Unfortunately, because the stabilizing amplifier controls the fast amplifier's positive terminal, the classic chopper-stabilized approach is restricted to inverting operation only.

A new approach

The LTC1052 (**Fig C**) adopts a different approach—one that permits full differential-input operation and good bandwidth while retaining extremely low drift. The IC relies on an autozeroing technique. During the device's autozero cycle, the inputs short together, and a feedback path closes around the input stage to null the offset. Switch S_2 and capacitor C_{EXTA} act as a sample/hold block to store the nulling voltage during the sampling cycle.

In the sampling cycle, the now almost-ideal amplifier serves to amplify the differential input voltage. Switch S_2 connects the amplifier input voltage to C_{EXTB} and the output gain stage. C_{EXTB} and S_2 act as a sample/hold circuit to store the amplified input signal during the autozero cycle. By switching between these two states—at a frequency much higher than that of the signal—a continuous output results.

During the autozero cycle, the inputs are not only shorted together, they're connected to the negative input. This action forces nulling with the common-mode voltage present. The same argument applies to power-supply variations; it explains the LTC1052's creditable CMRR and PSRR specs.

The complete amplifier contains stabilizing elements, a feed-forward loop for high-frequency signals, and antialiasing circuitry, but the IC owes its superior dc performance entirely to the simple loop described here.

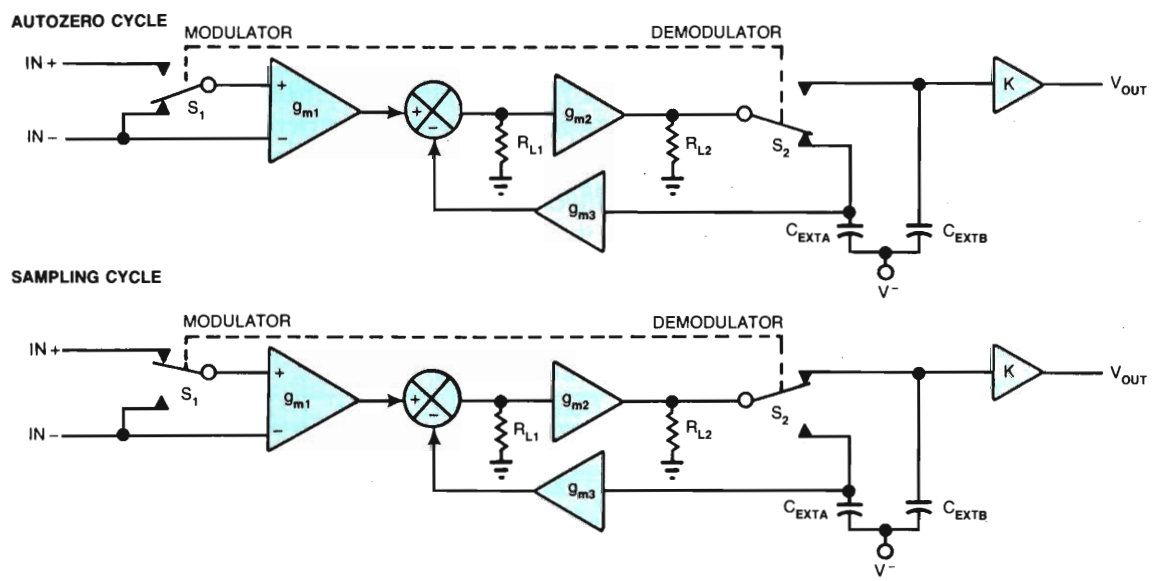


Fig C—Using autozeroing and sample/hold techniques, *the LTC1052 chopper-stabilized op amp offers full differential-input mode and specs extremely low offset drift and noise. During the autozero cycle, the inputs short together and feedback nulls the amplifier's offset. In the sampling cycle, the now offset-free amplifier amplifies the differential input voltage.*

To take maximum advantage of a chopper amplifier's low drift specs, you must consider various environmentally contributed, error-inducing sources.

cases, you'll want to prevent stray leakage currents from reaching the inputs. The simplest way to do this is to connect the amplifier's inputs directly to the signal source via a Teflon standoff. Because the amplifier's inputs never contact the pc board, stray leakage currents don't affect them.

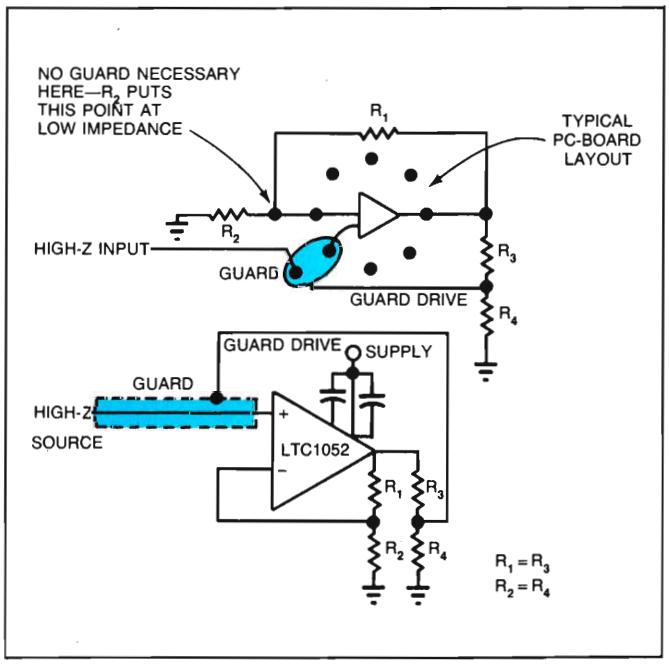


Fig 6—Use guarding to eliminate leakage-current effects. *The technique involves encircling sensitive inputs with a conductor driven by a potential equal to that of the inputs.*

Although the standoff approach is effective, its implementation might not be acceptable in production. Guarding is another technique to minimize pc-board leakage effects. The guard is a pc-board trace that encircles the amplifier's input. You must drive this trace (**Fig 6**) at a potential equal to that of the input, thereby preventing leakage to the amplifier's input terminal.

Carrier-induced problems

The final form of parasitic error is one peculiar to all carrier-based amplifiers. If the amplifier is operating in a circuit that contains clocking or oscillation with substantial harmonic content at or near the carrier frequency (eg, from another LTC1052), erratic operation might result. This is particularly true if inductors or transformers radiate magnetic fields related to the clocking or oscillation frequency. The undesired interaction between the amplifier's chopping sequence and the externally generated ac signals could cause mixing or beat frequencies, resulting in errors in the output.

Synchronizing the LTC1052's internal oscillator with external-circuit clocking eliminates the preceding problem. The 14-pin version of the IC offers one pin that lets you synchronize the internal clock with an external signal.

Input signals containing substantial ac content can also cause the problem if the ac signal has strong spectral components related to the chopping frequency. For applications in which such ac components exist, it

TABLE 1—LOW-NOISE, LOW-DRIFT OPERATIONAL AMPLIFIERS

MODEL	LTC1052 CHOPPER STABILIZED	ICL7652 CHOPPER STABILIZED	HA2904/5 CHOPPER STABILIZED	AD547 FET	LM-11 LOW-I BIPOLAR	LT1012 LOW-I BIPOLAR
INPUT OFFSET AT 25°C	5 μV	5 μV	50 μV	250 μV	300 μV	35 μV
INPUT OFFSET DRIFT	0.05 μV/°C	0.05 μV/°C	0.4 μV/°C	1 μV/°C	3 μV/°C	1.5 μV/°C
OPEN-LOOP GAIN	120 dB	120 dB	5 × 10⁸	2.5 × 10⁵	2.5 × 10⁵	3 × 10⁵
BIAS CURRENT AT 25°C	30 pA	30 pA	150 pA	25 pA	50 pA	100 pA
COMMON-MODE REJECTION RATIO	120 dB	110 dB	120 dB	88 dB	110 dB	114 dB
POWER-SUPPLY REJECTION RATIO	120 dB	110 dB	120 dB	100 dB	100 dB	114 dB
COMMON-MODE INPUT RANGE	V_{CC} – 2V V_{EE} + 0V	V_{CC} – 1.5V V_{EE} + 0.7V	10V WITH 15V SUPPLY	V_{CC} – 2V V_{EE} + 3V	V_{CC} – 0.5V V_{EE} + 1.5V	V_{CC} – 1.5V V_{EE} + 1.5V
SLEW RATE	3V/μSEC	0.5V/μSEC	2.5V/μSEC	3V/μSEC	0.3V/μSEC	0.1V/μSEC
GAIN-BANDWIDTH PRODUCT	1 MHz	0.45 MHz	3 MHz	1 MHz	0.8 MHz	0.8 MHz

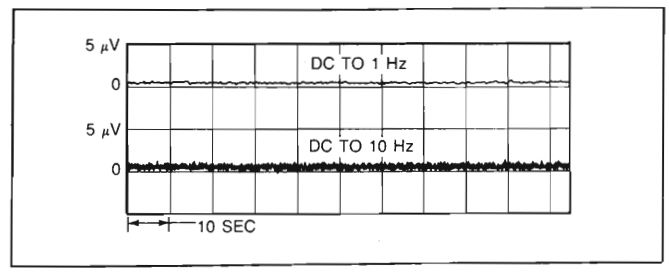


Fig 7—Showing what a chopper-stabilized op amp can do, *this strip-chart recording gives the LTC1052's input-noise voltages with 1- and 10-Hz bandwidths.*

might be necessary to drive the LTC1052 from an external clock source at a frequency that has no harmonic relationship with the input signal. For example, a 372-Hz clock frequency will prevent 60-Hz input components from affecting amplifier operation.

A look at the amplifier's specs

As mentioned, the LTC1052 improves upon the specifications of other available monolithic chopper-stabilized op amps. **Table 1** gives the IC's specs, along with those of other chopper-stabilized monolithics and, for purposes of comparison, those of an FET-input amplifier and two bias-current-compensated bipolar types. Note that the LTC1052's slew rate and bandwidth are much higher than those of its closest counterpart (the ICL7652), and offset and drift are much lower than the HA2904/5's.

Finally, noise is of particular concern in monolithic chopper-stabilized-amplifier designs. The **Fig 7** strip chart shows the LTC1052's noise performance at two measurement bandwidths. Also, the amplifier's input common-mode range includes the negative supply level, thereby making single-supply operation practical. **EDN**

Author's biography

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in related capacities at National Semiconductor Corp, Arthur D Little Inc, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art, and collecting antique scientific instruments.

Chopper amplifier improves operation of diverse circuits

A chopper-stabilized operational amplifier's low dc offset and time and temperature drift suit it to low-level dc-signal-processing applications. The first article in this 2-part series outlined the precautions you must take to obtain maximum benefit from the op amp's low drift and offset voltage. In this installment, you'll see how to make optimum use of the op amp's intrinsic stability in circuits ranging from a simple remote thermometer to an exceptional V/F converter.

Jim Williams, *Linear Technology Corp*

The LTC1052 op amp, like all chopper-stabilized, monolithic amplifiers, whose characteristics include low drift, high gain, and high input impedance, suits many demanding applications. Although this new device provides dc performance superior to that of previous monolithics, you must combat various error sources to use it most effectively. (See *EDN*, February 21, 1985, pg 305.) Once you are aware of the problems involved in using such a device and know how to solve them, you can consider ways to apply the amplifier in a variety of circuit designs.

The most obvious applications involve low-level dc signals; the op amp's low drift makes it superior to other amplifiers for such applications. On a more sophisticated level, you can exploit the LTC1052's low offset errors to extend the dynamic range of a circuit. Some of the following circuit descriptions demonstrate these points; others cover the use of the op amp to stabilize and enhance the performance of data converters, buffers, comparators, and other functional blocks. One of these circuits exploits the LTC1052's dynamic operating range to provide a V/F converter with 1-Hz to 30-MHz output for 0 to 5V input. Another circuit, the first described, uses two of the op amps in a variable voltage reference.

Standards-grade variable reference

In the **Fig 1** variable voltage reference (suitable for use in a standards laboratory), a pair of LTC1052s combine with high-grade saturated cells and other components to produce an extremely accurate, stable reference source. You can use the circuit to calibrate 6½-digit digital voltmeters, ultra-high-resolution data converters, and other apparatus requiring high-order traceability to primary standards.

The SCO106 saturated cells provide a reference voltage that IC_1 buffers and amplifies to precisely 10V. IC_1's output drives a 7-place Kelvin-Varley divider whose accuracy is 1 ppm. IC_2's low bias current and

A chopper amplifier's low offset and drift provide performance improvements in a variety of circuit applications.

high common-mode rejection let it unload the divider without introducing significant errors. To calibrate the circuit, adjust IC_1's output for exactly 10V by selecting the feedback resistor and trimming the 20-MΩ potentiometer.

You should measure IC_1's output with equipment that has high-order traceability to primary National Bureau of Standards specifications. Once calibrated, this circuit will provide 0.0014% worst-case accuracy over one year's time and ±5°C excursions. Note that the amplifiers contribute only about 1.3 ppm (0.00013%) of the total error.

Precision instrumentation amplifier

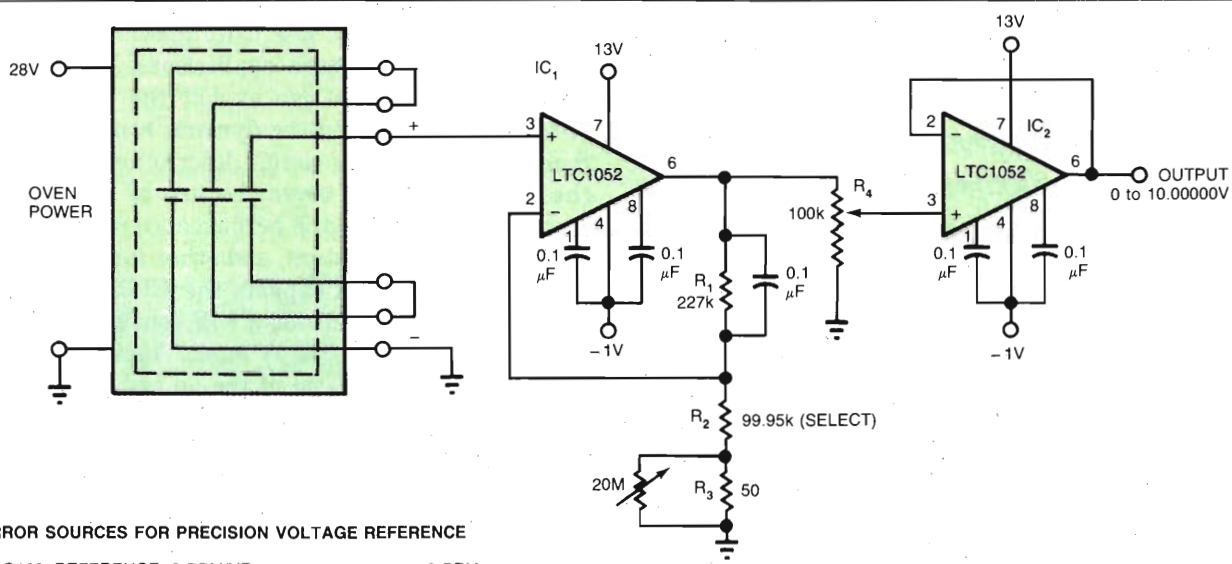
Another application for the LTC1052 is in an ultra-high-precision instrumentation amplifier (**Fig 2**). This circuit offers greater accuracy and lower drift than any commercially available IC—hybrid or module. In addition, it operates from one 5V power supply. Using a flying-capacitor technique, the LTC1043 switched-capacitor instrumentation building block provides a conversion from differential to single-ended input.

C_1 alternately samples the differential input signal and charges ground-referred C_2 with the sampled information. The LTC1052 measures the voltage across C_2 and provides the circuit's output. The amplifier's feedback-resistor ratio sets the gain. The LTC's output stage can normally swing within 15 mV of ground. If you need an output that can reach 0V, you can use the circuit shown within the broken lines; the configuration uses the remaining LTC1043 section to generate a small negative voltage by inverting a diode drop.

This negative potential drives the 10-kΩ pull-down resistor to force the LTC1052's output into class-A operation for voltages near zero. It is important to observe that the circuit's switched-capacitor front end forms a sampled-data filter that allows common-mode rejection to remain high—even with increasing frequency. The 4.7-nF capacitor sets the front end's switching frequency at a few hundred hertz.

Isolation amplifier

You can't always use an instrumentation amplifier to condition differential signals. In factory and process-



ERROR SOURCES FOR PRECISION VOLTAGE REFERENCE

SCO106 REFERENCE: 2 PPM/YR	2 PPM
IC_1: 0.05 μV/°C × 3(GAIN) × 5°C = 0.75 μV	0.075 PPM
IC_2: 0.05 μV/°C × 1(GAIN) × 5°C = 0.25 μV	0.025 PPM
IC_1 AND IC_2: TIME DRIFT/YR = 2 μV	0.02 PPM
VDR-307 DIVIDER: 0.5 PPM/°C × 5°C + 1 PPM/YR	3.5 PPM
RESISTORS: 0.1 PPM/°C (RATIO) × 5°C + 2 PPM/YR	7 PPM
IC_2 CMRR ERROR: 1 PPM	1 PPM
IC_2 LOADING ERROR: 0.2 PPM	0.2 PPM
	13.82 PPM

NOTES:
SATURATED CELL IS JULIE RESEARCH LABS MODEL SCO-106.
R_1 AND R_2 ARE JULIE RESEARCH LABS TYPE NB-1.
R_3 IS TRW TYPE MAR-6.
R_4 IS JULIE RESEARCH LABS KELVIN-VARLEY DIVIDER MODEL VDR-307.
USE SINGLE-POINT GROUNDING.

Fig 1—Meeting standards-lab specifications, *this reference source provides ±0.0014% worst-case accuracy for a full year after calibration. The LTC1052 chopper amplifiers contribute only about one-tenth of the total error. The circuit provides an ideal calibration standard for voltmeters, converters, and other exacting apparatus.*

control environments, for example, severe ground-line and common-mode voltages often mandate the use of an isolation amplifier. This device's inputs have galvanic isolation from the output and power connections. Because of this, the amplifier can ignore the effects of ground loops and operate at common-mode input voltages that are many times higher than the power-supply voltage.

Implementing a precise, low-drift isolation amplifier isn't easy, and commercial units are expensive. **Fig 3** shows a circuit with 0.03% transfer accuracy and the 50-nV/°C input drift of the LTC1052. As configured here, the circuit provides a gain of 1000; it can operate with common-mode input levels as high as 250V. The circuit works by modulating the output of a signal-conditioning amplifier's output amplitude through a transformer.

A synchronous demodulator/filter reconstructs the isolation amplifier's original output and provides the circuit's output. A separate oscillator and transformer provide the amplifier with power and thus preserve galvanic isolation between the circuit's input and output ports. Three 74C04 gates and their associated components form an oscillator that provides complementary drive to Q_5 and Q_6. These devices energize T_1, which in turn generates floating power on the input side of the **Fig 3** circuit.

The oscillator simultaneously provides a slightly delayed, complementary drive to the Q_1 and Q_2 FET switches by means of the 330Ω-100-pF network and the additional inverters. Rectified and filtered, the floating power produced by T_1 drives the LTC1052 (IC_1) via the zener drops of the transistors. The ±15V floating power is accessible, so you can use it to power transducers or other loads.

You can prevent interaction between the transformer's chopping carrier and IC_1's internal oscillator by synchronizing the amplifier with the carrier. Use the two decade counters for this operation. Q_3 and Q_4, driven by opposing-phase carrier signals derived from T_1, chop IC_1's output into T_2. T_2's other winding receives this modulated signal information. Because Q_1 and Q_2 switch synchronously with Q_3 and Q_4, they demodulate the amplitude and phase-polarity information in the carrier.

The 330Ω-100-pF network compensates for the slight skew in switch-drive signals on opposing sides of T_2 and, in this way, minimizes gain error. IC_2, which also provides the circuit's output, filters T_2's output (pin 2). Slight switching errors in the modulator/demodulator

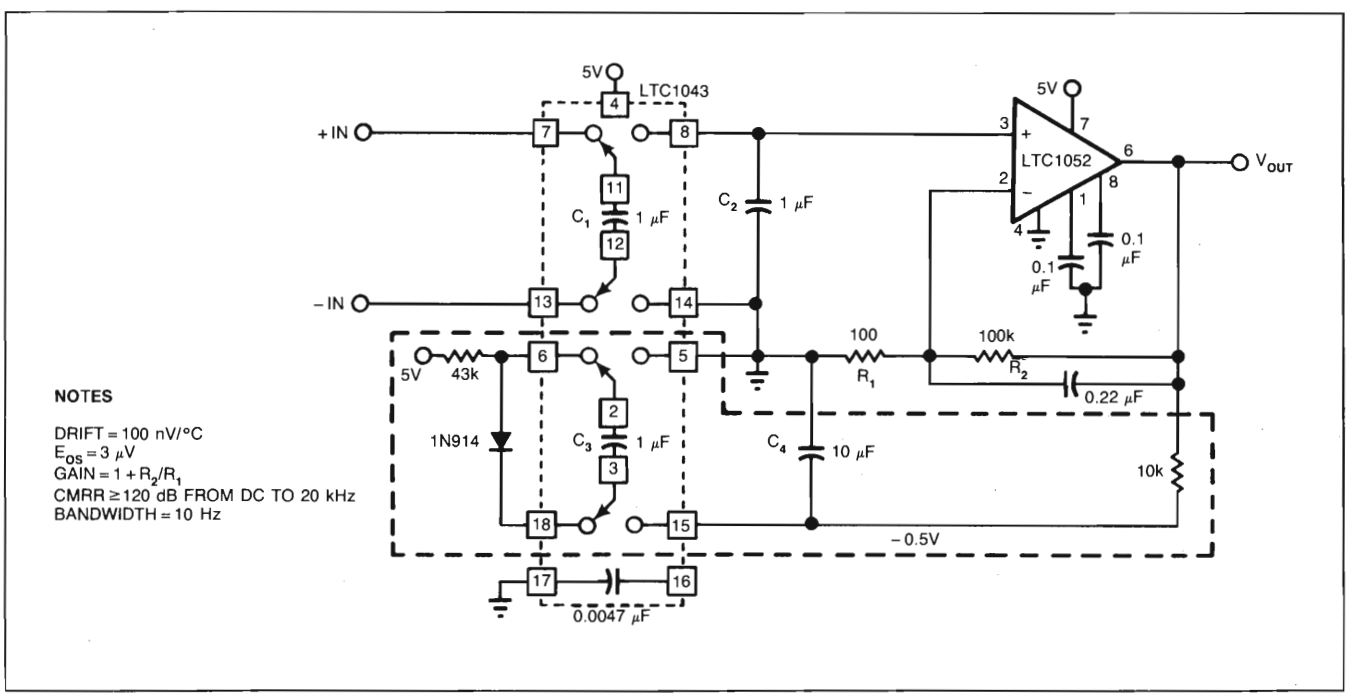


Fig 2—Extreme accuracy and minimal drift *are the hallmarks of this instrumentation-amplifier circuit. The configuration outperforms any available IC—hybrid or module. The method used involves a flying-capacitor technique that provides conversion from differential to single-ended input.*

Laboratory-grade voltage reference uses saturated cells and chopper amplifiers to configure a circuit accurate enough to serve as a lab calibration standard.

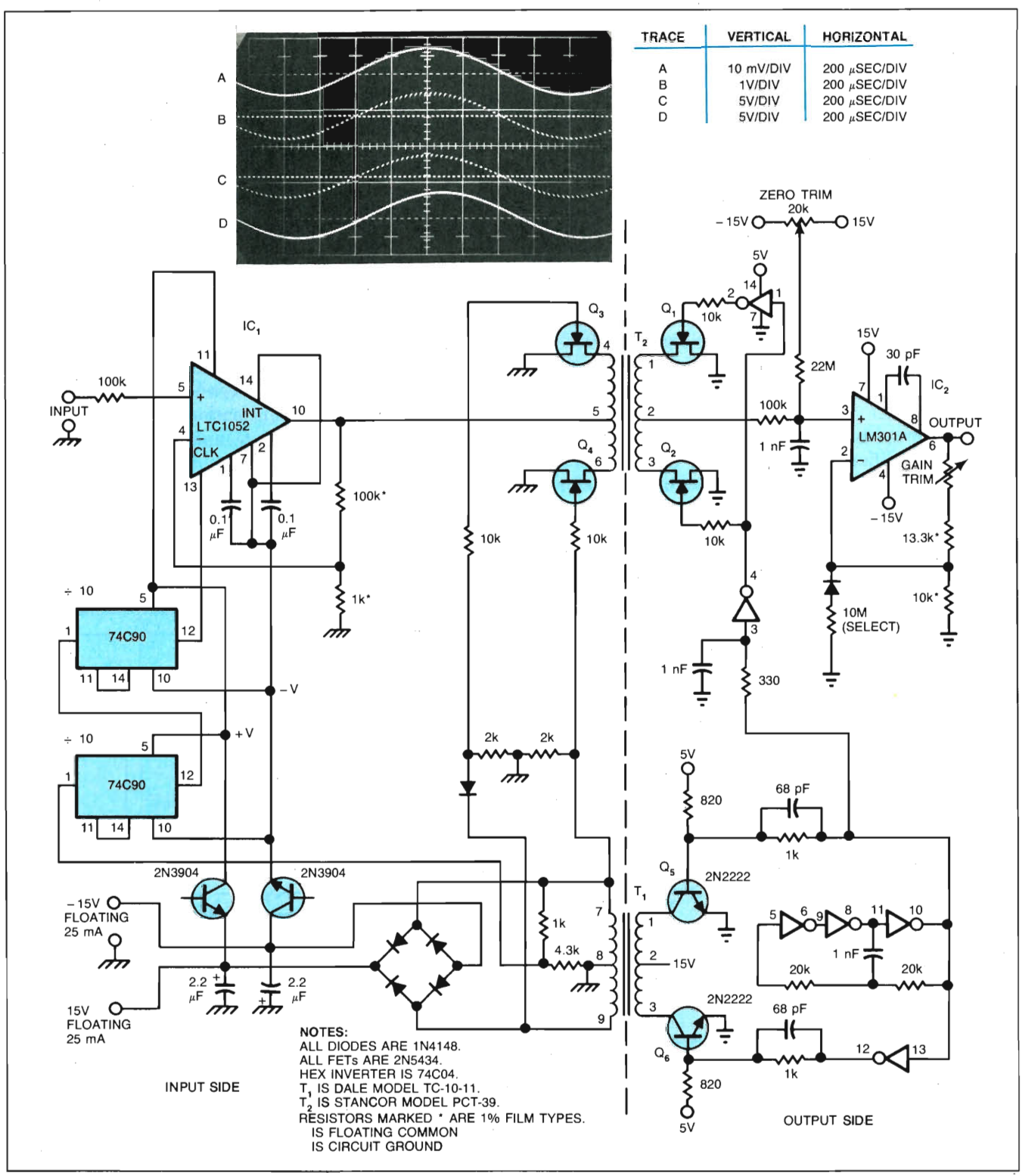


Fig 3—Suitable for industrial environments, *this isolation amplifier accepts common-mode input levels as high as 250V. The circuit operates by modulating the output of a signal-conditioning amplifier. It then demodulates and filters this amplitude-modulated signal.*

result in very small gain differences between positive and negative outputs at pin 2 of T_2. By providing a small gain reduction for negative outputs, the diode-resistor network in IC_2's output compensates for these differences.

The scope photo in **Fig 3** shows the response of the isolation amplifier to a sine-wave input. For this test, you tie the floating common level and circuit grounds together. Trace A is the input to IC_1. Trace B, taken at pin 4 of T_2, shows IC_1's amplified output being modulated into the transformer. Trace C, obtained at pin 1 of T_2, depicts the received modulated waveform as it is sychronously demodulated. The filtered and final output of IC_2 appears in trace D.

The 25-kHz carrier limits this circuit's full-power bandwidth to about 500 Hz, a level adequate for process-control and transducer applications. The transformers discussed here have a 250V breakdown specification; you can, however, achieve higher levels by using transformers with higher ratings. As shown in the **Fig 3** schematic, circuit gain is 1000, and this allows amplification of a ±5-mV signal (riding on 250V of common mode) to a ±5V output signal. Gain accuracy is 0.03%, and drift is 50 ppm/°C typ. The LTC1052's 50-nV/°C specification sets the input-referred drift.

To trim the circuit, tie IC_1's input to floating common, and adjust the zero-trim potentiometer for 0V output. Next, connect IC_1's input to a +5-mV source, and adjust the gain-trim potentiometer for exactly +5V output. Finally, connect IC_1's input to a −5-mV source, and select the resistor (shown as 10 MΩ) in IC_2's feedback path for a −5V output reading. Repeat the procedure until all three points are fixed.

Aside from its use in isolation amplifiers to handle the severe ground-line and common-mode voltages found in factory and process-control environments, the LTC1052 can be used in a circuit that meets a frequent need in automatic semiconductor-testing and -probing equip-

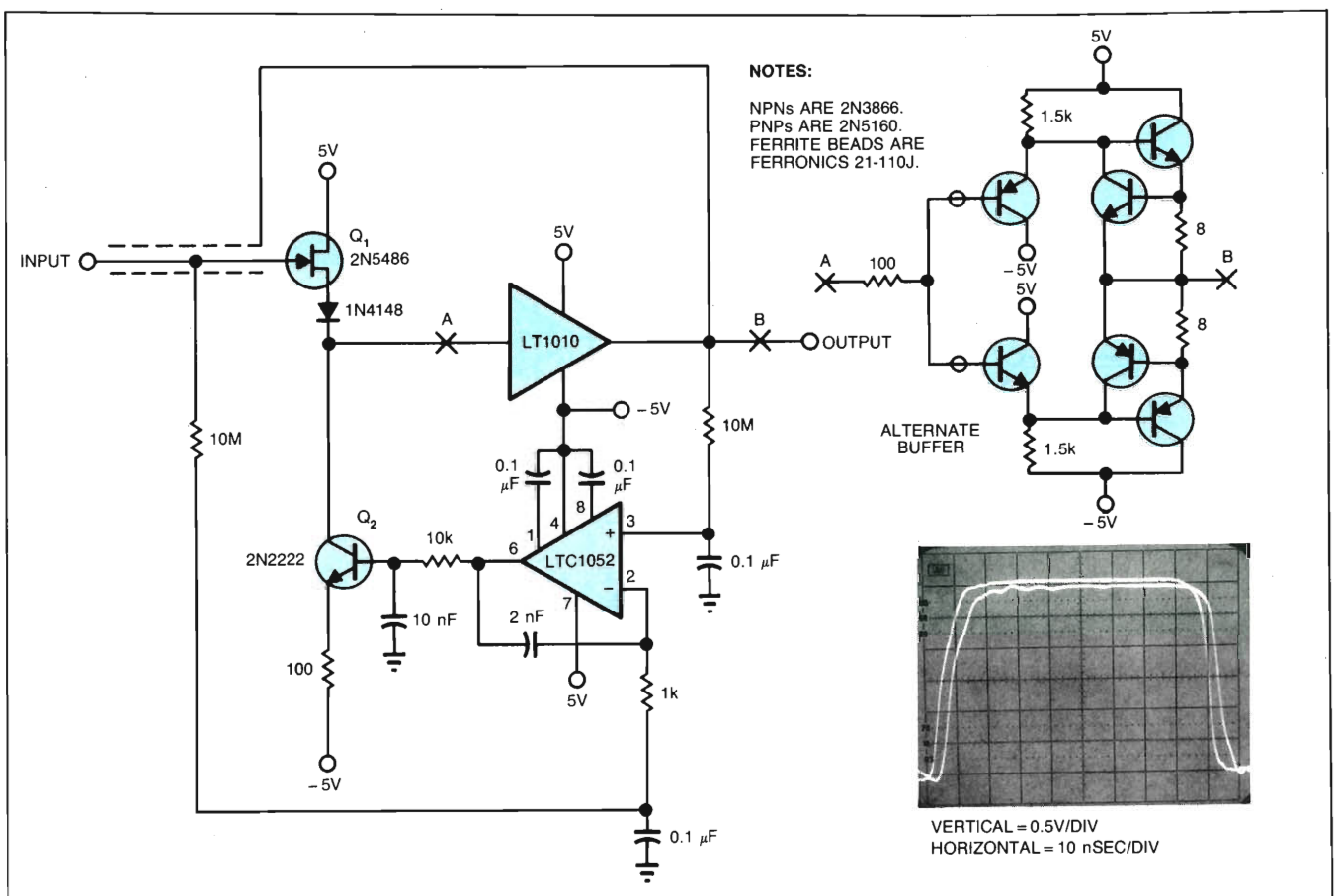
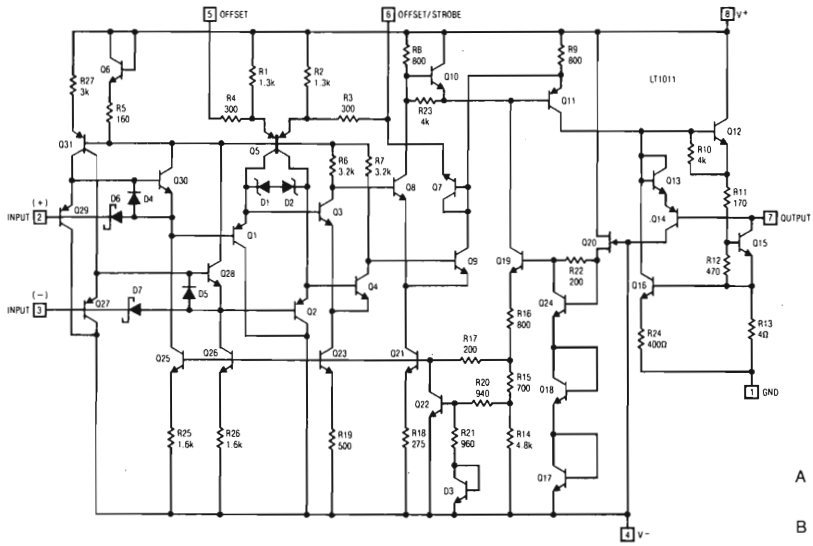


Fig 4—Low capacitive loading and low cost *are featured in this unity-gain, FET-probe buffer. The circuit features extremely fast rise time and low (4-nsec) delay; its gain is about 0.95.*

Instrumentation amplifier beats specs of commercially available units and works from one 5V supply.



TRACE	VERTICAL	HORIZONTAL
A	2V/DIV	50 μSEC/DIV
B	20V/DIV	50 μSEC/DIV
C	10V/DIV	50 μSEC/DIV
D	20V/DIV	50 μSEC/DIV

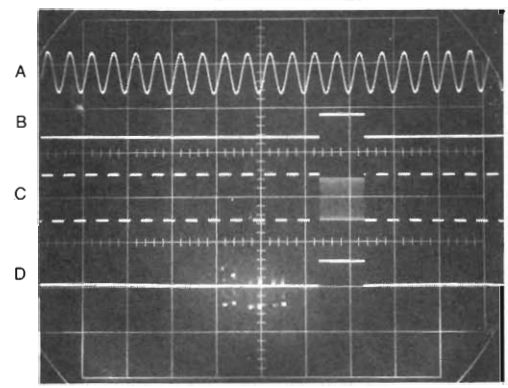


Fig 5—Offering an easy way to overcome comparator compromises, *this circuit uses a chopper amplifier to stabilize the comparator's offset voltage and drift. The method entails no sacrifice in speed or differential-input capability. The circuit periodically short circuits the comparator's inputs and nulls its offset. The result is a high-speed comparator configuration with <5-μV offset.*

ment: the demand for a highly accurate, unity-gain buffer-amplifier with low input capacitance. Such an amplifier is useful for other circuit chores as well (including the accurate monitoring of a point without introducing any significant ac or dc loading). **Fig 4** illustrates one such circuit.

In this circuit, Q_1 and Q_2 constitute a simple, high-speed input buffer. Q_1 functions as a source follower, and the Q_2 current-source load sets the drain-source channel current. The LT1010 buffer provides output-drive capability for cables or for whatever load exists. Because there's no dc feedback, you'd naturally expect this open-loop configuration to exhibit considerable drift. However, the LTC1052 has a feedback function to stabilize the circuit.

To ensure low drift in this situation, the op amp compares the filtered circuit-output signal to a similarly filtered version of the input signal. The amplified difference between these signals serves to set Q_2's bias and hence Q_1's channel current. This action forces Q_1's V_{GS} to whatever voltage level is necessary to make the circuit's input and output potentials equal.

The diode in Q_1's source line prevents the gate from becoming forward biased; the 2000-pF capacitor at IC_1 provides stable loop compensation. The RC network at IC_1's output prohibits this point from experiencing high-speed edges coupled through Q_2's collector-base junction. The output of IC_2 also feeds back to the shield around Q_1's gate lead and, as a consequence, effectively bootstraps the circuit's input capacitance to <1 pF.

The LT1010's 15-MHz bandwidth and 100V/μsec slew rate, combined with the amplifier's 150-mA output, are sufficient for most circuits. In extremely high-speed applications, the alternate, discrete-component buffer shown in the schematic can be useful. Although its output current handles only 75 mA max, the GHz-range transistors used provide exceptionally wide bandwidth, fast slewing, and minimal delay.

The scope photo in **Fig 4** shows the response of the LTC1052-stabilized, buffer-circuit/discrete-stage combination. The response is clean and quick, and delay is <4 nsec. Remember that the rise time is limited by the pulse generator and not by the circuit itself. For either stage, the LTC1052 sets the offset at 3 μV; stage gain is

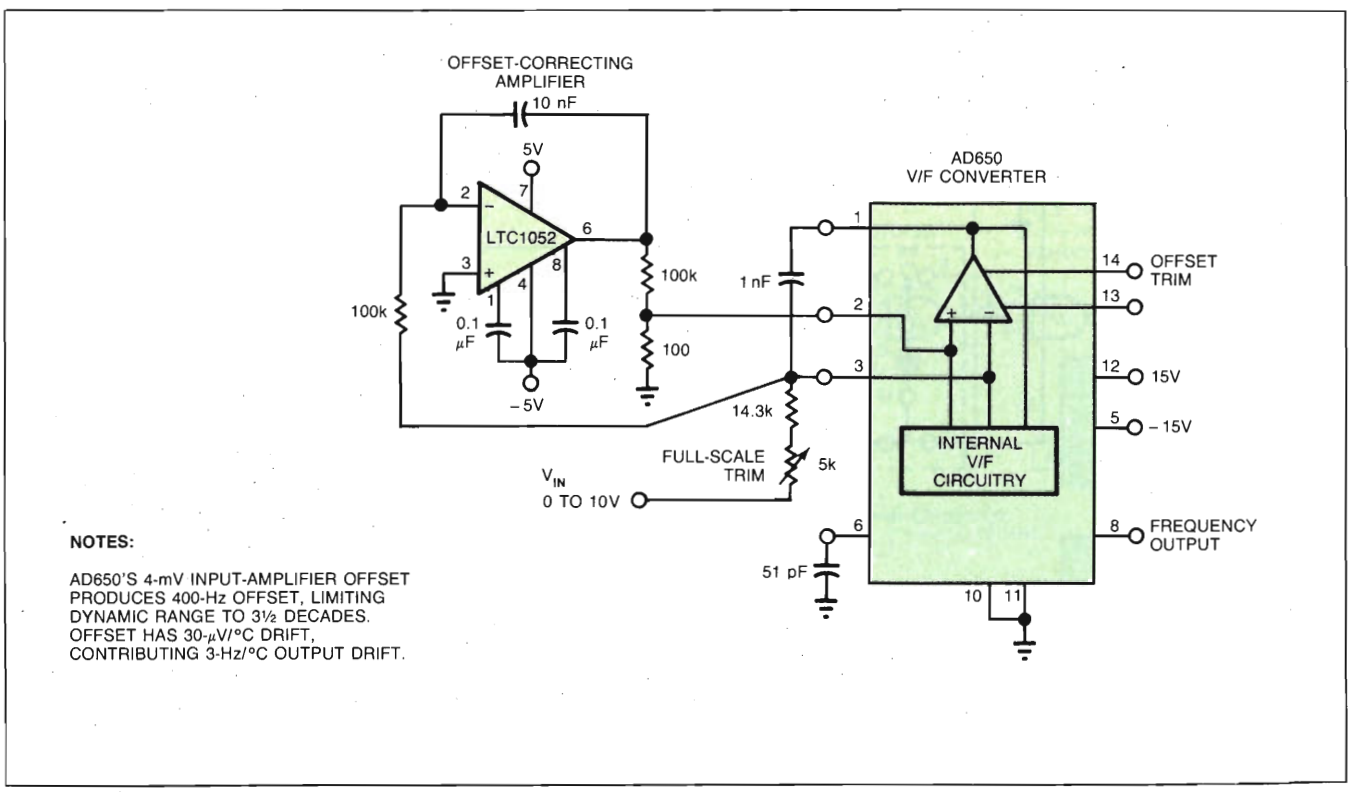


Fig 6—You can double the dynamic range *of a popular V/F-converter IC by using this stabilization circuit. The configuration eliminates the need for an offset trim; moreover, it reduces temperature drift to negligible levels. This method increases the converter's dynamic range from 3½ to 6 decades.*

Industrial-application isolation amplifier withstands high common-mode input signals and provides high accuracy and low offset.

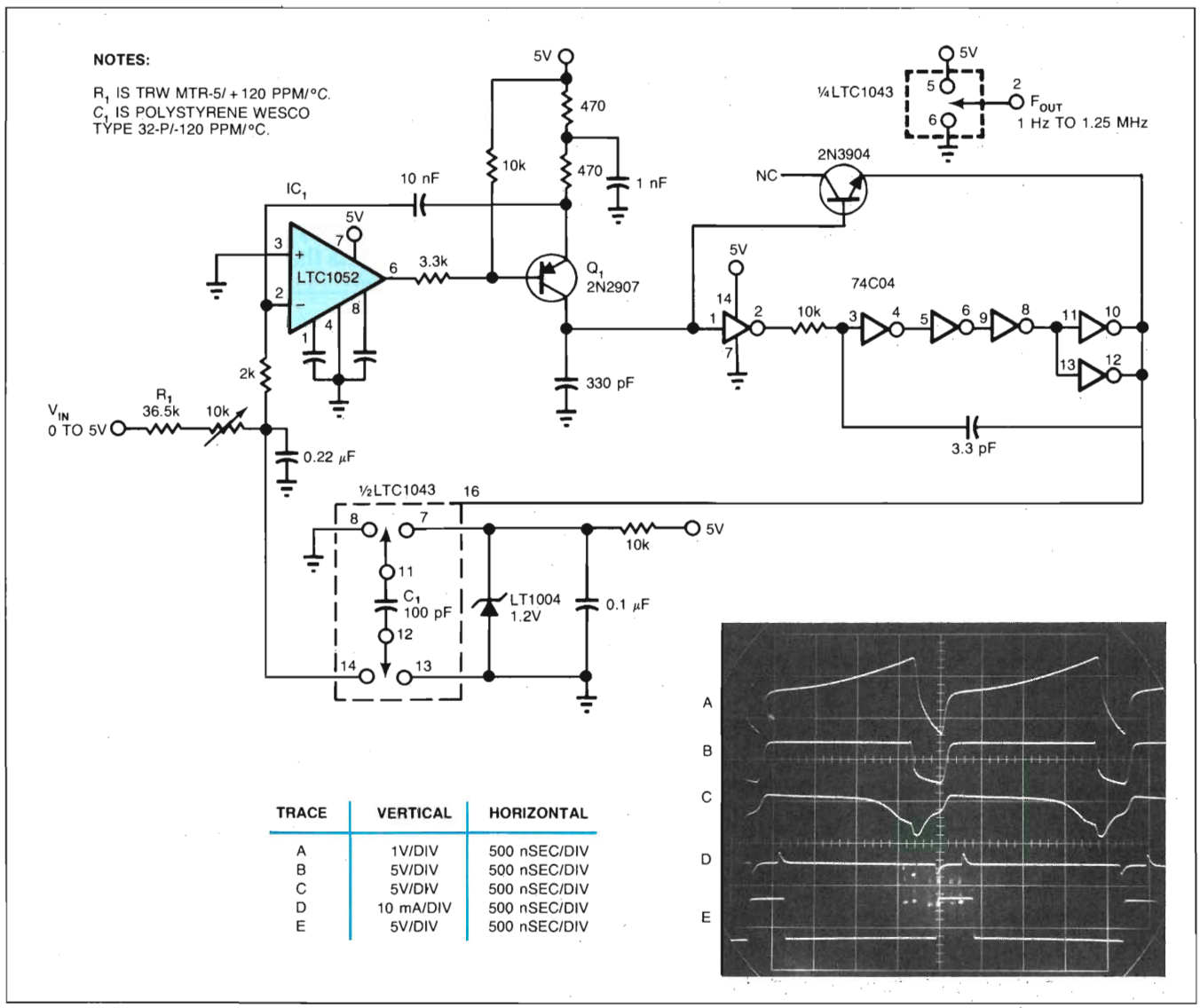
approximately 0.95. At a much lower price, this circuit performs the same function as commercial FET probes that cost about $1000.

Chopper-stabilized comparator

You can also use the LTC1052 in a reasonably fast comparator that exhibits low input-offset drift. Such a device is useful in high-resolution A/D converters, crossing detectors, or wherever you need a high-speed comparison that is both stable and precise. The problem is that it's difficult to achieve reasonable comparator speed and low input drift in a traditional design; hence monolithic-comparator designs must necessarily entail tradeoffs between drift and speed.

Fig 5 shows how to use the LTC1052 to eliminate offset and drift in a comparator without any sacrifice in speed or differential-input capability. Remember that this circuit is useful only in situations where some free time is available for the system's nulling action. The circuit functions by periodically short-circuiting the comparator's inputs together and then forcing the comparator into its linear region via its offset pins.

The circuit stores the balancing voltage required at the comparator's offset pins. When the comparator's



TRACE	VERTICAL	HORIZONTAL
A	1V/DIV	500 nSEC/DIV
B	5V/DIV	500 nSEC/DIV
C	5V/DIV	500 nSEC/DIV
D	10 mA/DIV	500 nSEC/DIV
E	5V/DIV	500 nSEC/DIV

Fig 7—Offering improvements over Fig 6's circuit, *this V/F converter covers a 1-Hz-to-1.25-MHz range. What's more, it features high linearity and low drift. Its low (330-pF) integrating capacitor demands low-leakage pc-board mounting techniques.*

inputs return to their normal states, the stored voltage remains at the offset pins; in this way, the stored voltage nullifies the device's offset. Updating (in periods of seconds) ensures continuous correction stability. In this circuit, IC_2 is the stabilizing amplifier for IC_1. A dpdt switch section provided by the LTC1043 controls IC_1's inputs.

When pin 16 of the LTC1043 is high, pins 12 and 11 connect to pins 13 and 7, respectively. Pin 3 (IC_1's output) connects to pin 18. Under these conditions, IC_2 is connected in the feedback loop between IC_1's output and its offset terminal (pin 5). This feedback forces IC_1 into its linear region; IC_1's output oscillates between the rail voltages.

IC_2, connected as a low-frequency integrator, filters this oscillatory voltage, compares its equivalent dc value to ground (the device's noninverting-input potential), and drives IC_1's offsets to zero. When pin 16 of the LTC1043 goes low, all switch states reverse; IC_1's inputs are then free to compare the signals present at pins 14 and 8 of the LTC1043.

During the comparison interval, IC_2's output remains fixed at the voltage stored in its feedback capacitor. IC_2's low bias current allows long durations between

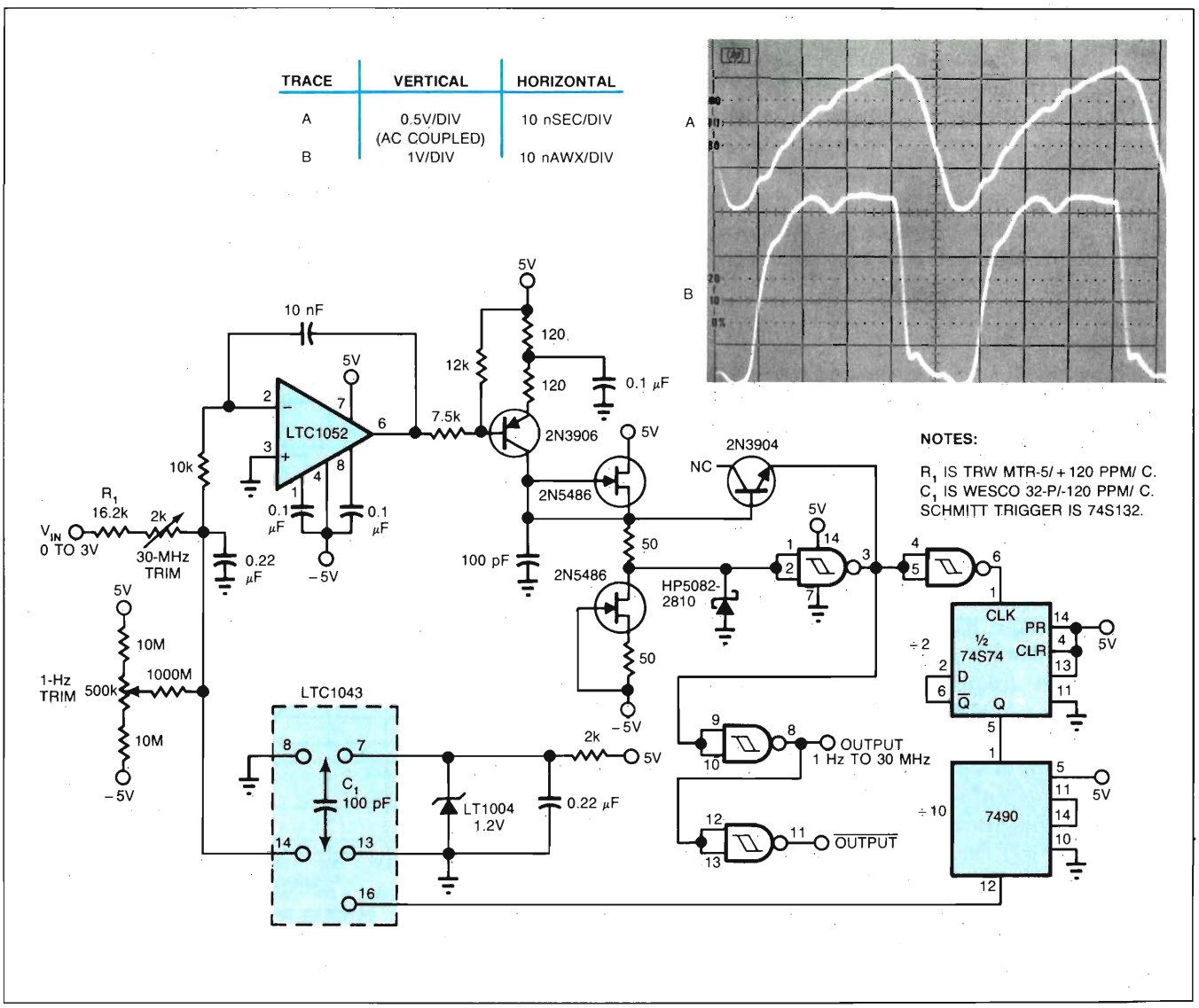


Fig 8—The widest range V/F converter yet, *this circuit offers 150-dB dynamic range—output frequency spans 7½ decades. The circuit specs 0.08% linearity as well as low jitter and noise over the entire range.*

A chopper op amp combined with high-speed ICs provides a fast, low-capacitance probe and a fast-switching, low-drift comparator.

correction cycles—indeed, periods of seconds are practical. At the same time, the current maintains the comparator's effective offset well within 5 μV with negligible temperature drift.

The **Fig 5** photo shows the circuit's response to a sine wave (trace A) applied to IC_1's positive input at pin 14 of the LTC1043. IC_1's negative input, pin 8 of the LTC1043, connects to ground. When the zero-command control line is low (trace B), IC_1's output (trace C) responds in the normal fashion. During this period, the status output (trace D) is low, a confirmation that IC_1 is in fact operating in its normal mode.

When the zero command occurs (trace B, just to the right of the screen's center), it forces IC_1 into its linear region, where it oscillates. During this time, IC_2 updates the correction voltage stored in its feedback capacitor. When the zero-command pulse falls, normal comparator action resumes. The circuit's true operating mode is reflected in its status output because the circuit's timing includes the 50-nsec delay of the LTC1043 switch. For this reason, you should use the status output—and not the zero-command line—to monitor the circuit's operating state.

High-stability V/F converter

Amplifiers and comparators are not the only elements that can benefit from the LTC1052's chopper stabilization: **Fig 6** shows a way to stabilize the offset of a data converter; the method doubles its dynamic operating range, eliminates the need for an offset trim, and reduces the converter's zero drift to negligible levels. In this circuit, the LTC1052 corrects for offset deficiencies in an AD650 V/F converter.

Although specified for 1-MHz full-scale operation, this V/F-converter IC's 4-mV input offset limits its untrimmed dynamic operating range to only 3½ decades of output frequency. Under normal operating conditions, the AD650's positive input connects to ground; the resistor string shown drives the negative input. To obtain more than 3½ decades of operation, you must effect an offset trim at pins 13 and 14. Even after trimming, however, the input amplifier's 30-μV/°C drift contributes a 3-Hz/°C zero-point error.

The LTC1052 corrects these problems by measuring the offset voltage at the AD650's negative input, comparing this input to ground, and then driving the positive input (normally grounded in the manufacturer's recommended circuit configuration) with the appropriate stabilizing correction voltage. The LTC1052's integrating configuration has high gain at low frequency and dc and thus preserves the AD650's fast dynamic response while eliminating the converter's offset errors.

Without causing overdrive during start-up and transients, the scaling of the divider network in the LTC1052's output allows enough correction range to zero the AD650's offsets. With this scheme, the circuit requires no zero trim to achieve full 6-decade operation. To calibrate the circuit, apply exactly 10V to the input, and trim the output for precisely 1 MHz.

Another stabilized V/F converter appears in **Fig 7,** but this converter's parameters represent substantial improvements over those of the previous circuit: This

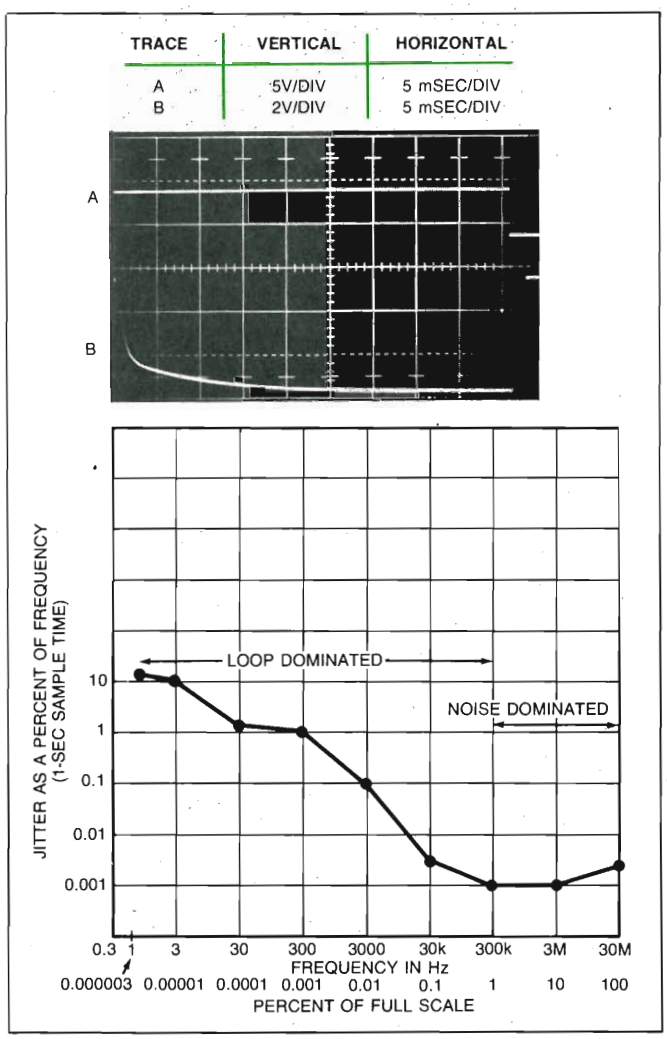


Fig 9—A closed-loop approach *yields low output jitter in* ***Fig 8****'s circuit, as this curve illustrates. For low frequencies, the feedback loop is the major jitter-producing factor; at high frequencies, the current-source and Schmitt-trigger noise predominates. The feedback loop slows step response, as the scope photo shows.*

circuit offers a range of 1 Hz to 1.25 MHz, 0.05% linearity, and a temperature coefficient of 20 ppm/°C typ. What's more, the **Fig 7** circuit is less expensive. The tradeoffs include a slower step response and a higher component count.

The circuit uses a charge-feedback scheme that allows the LTC1052 to close a loop around the entire V/F converter as opposed to simply controlling offset. This approach augments linearity and stability but adds the loop's settling time to the V/F converter's overall step-response time. The **Fig 7** photo shows the circuit's various waveforms.

A positive input voltage causes IC_1's output to become negative and, consequently, biases the Q_1 current source. Q_1's collector injects current into the 330-pF capacitor; an increase in this element's voltage (trace A) results. Biased from the ±5V supplies, the CMOS inverter, which has low input current, changes state

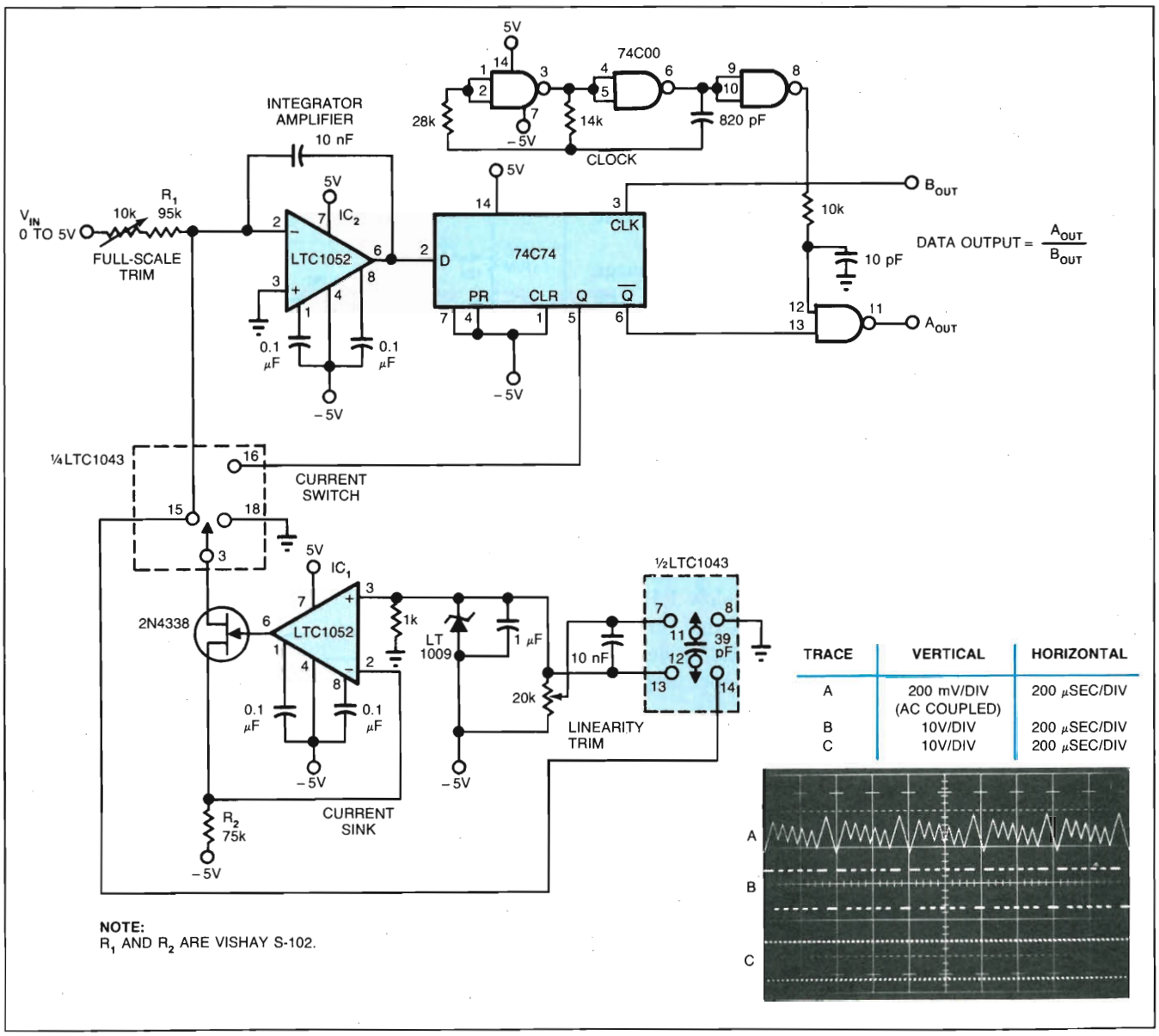


Fig 10—Offering 16-plus bits of resolution, *this A/D converter provides resolution to 100,000 counts (vs a normal 16-bit converter's 65,536 counts). The circuit uses a current-balancing technique and allows a mid-scale linearity trim that overcomes a parasitic error induced by charge pumping.*

Chopper-amplifier techniques stabilize offset of V/F and A/D converters, provide enhanced resolution, and eliminate the need for trimming.

when the ramp crosses 0V. This action causes all the inverters to switch.

The two parallel inverters at the end of the chain switch low (trace B) and simultaneously supply positive feedback to the 10-kΩ-3.3-pF junction as well as force the 330-pF capacitor to a lower voltage. They execute the latter action by removing current from this capacitor (trace D) via the diode-connected 2N3904. During the ramping interval, the LTC1043's switching pins 11 and 12 connect to pins 7 and 13 and so charge the 100-pF capacitor to the LT1004's reference voltage.

When the output inverters go low, they switch the LTC1043's control pin 16; at that point, the switch places the charged 100-pF capacitor across pins 8 and 14. Thus, each time the inverters switch, a fixed quantity of charge is dispensed into the X junction according to the equation Q=CV. The LTC1043's switching action is such that this charge is of opposite polarity to that of the noninverting input current.

The 0.22-μF capacitor integrates the discrete charge dumps to a dc level. The IC_1 servo controls the Q_1-inverter oscillator to run at whatever frequency is needed to force the servo's negative input to 0V. In this manner, IC_1's closed-loop control compensates for the oscillator's drift and nonlinear response. The circuit's frequency output (trace E) comes from pin 2 in the other LTC1043 section.

Several factors contribute to this circuit's performance: In spite of the small 330-pF integrating capacitor, the low input current of the CMOS inverter, combined with the low leakage of the 2N3904's base-emitter diode, allows operation to well below 1 Hz. In the lower frequency ranges, currents at this junction are small; therefore, pc-board leakage can lower the effective resistance at this point and hence degrade low-frequency operation.

To remedy the leakage effects, you can use a clean board, but the best approach is to mount the capacitor, Q_1's collector terminal, the inverter input, and the transistor's base terminal all on a Teflon standoff using connections that are as short as possible. The resistor and capacitor specified in **Fig 7,** both gain-determining components, have opposing temperature coefficients, and these characteristics aid gain-drift performance.

The LTC1052's low offset eliminates the need for a zero trim while preserving the circuit's >120-dB dynamic operating range. To trim the circuit, apply exactly 5V to the input, and adjust the 1.25-MHz trim for precisely 1.25-MHz output.

Although the performance of the previous circuit is impressive, that circuit still doesn't tax the LTC1052's dynamic operating range. **Fig 8** shows a substantially modified version of the circuit in **Fig 7.** It offers a 1-Hz to 30-MHz output (ie, a 150-dB dynamic range), for 0 to 5V input. These figures represent by far the widest dynamic range and highest operating frequency of any V/F converter described in published literature.

This V/F converter exploits the extremely wide signal-processing range of the LTC1052. The circuit maintains 0.08% linearity over its 7⅓-decade range and exhibits full-scale drift of approximately 20 ppm/°C. Zero-point drift is 0.3 Hz/°C, a figure that's directly related to the LTC1052's 50-nV/°C offset-drift spec.

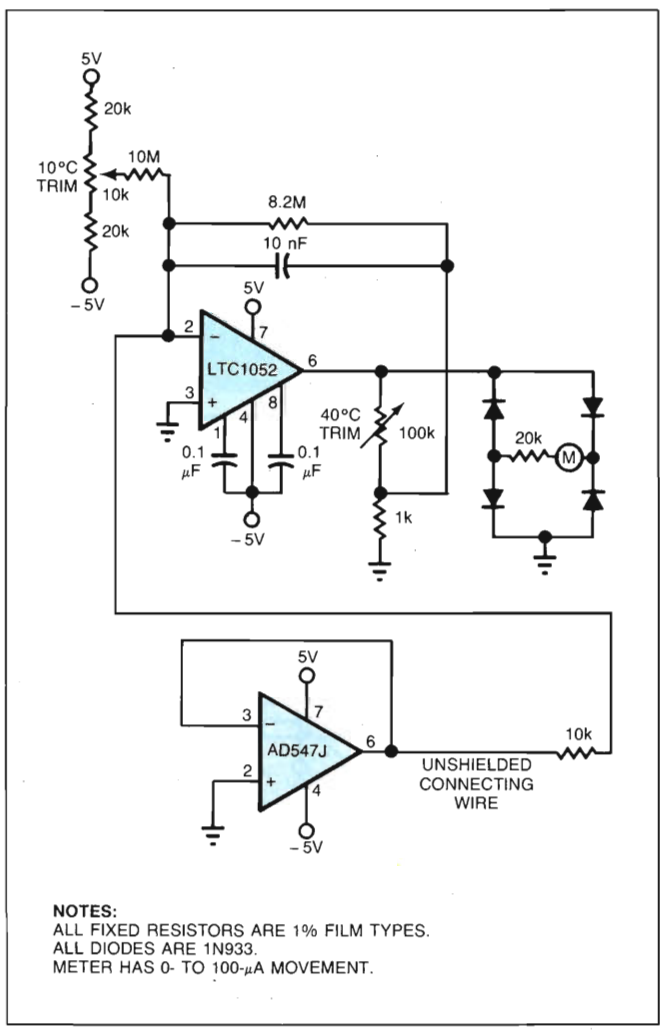


Fig 11—Taking advantage of an op amp's offset-voltage drift, *this circuit allows direct transmission of temperature data over an unshielded wire. The diode bridge at the output permits the use of op amps with either positive or negative offset drifts. The circuit has a 2-point calibration procedure.*

Current- and voltage-enhancement techniques provide increased output without attendant offset and drift compromises.

To attain the additional bandwidth, a fast JFET buffer driving a Schottky-TTL Schmitt trigger replaces the CMOS inverters in the **Fig 7** circuit. The Schottky diode prevents negative voltage levels at the Schmitt trigger's input. The diode-connected 2N3904 resets the low-value (100-pF) capacitor. This circuit avoids the positive feedback of **Fig 7**'s circuit and its attendant recovery time constant.

The Schmitt trigger's input-voltage hysteresis defines the limits of the oscillator's excursions. The 30-MHz full-scale output is much faster than the LTC1043 can accept; therefore, the digital divider stages reduce the feedback signal's frequency by a factor of 20. The remaining Schmitt-trigger sections provide complementary outputs. To avoid undesirable parasitic effects, you should use good high-frequency wiring techniques to construct the current-source-buffer and Schmitt-trigger sections .

The **Fig 8** photo gives the key waveforms when the circuit is idling at 20 MHz. Trace A is the Schmitt-trigger input (you can see that it follows a ramp function between two voltage limits), while trace B is the trigger's output. The closed-loop approach results in very low output jitter and noise over the 150-dB operating range. **Fig 9** plots this jitter as a function of output frequency. The jitter does not exceed 0.01% above 20 kHz, a frequency that's only about 0.05% of full scale.

Even at 1 ppm of full scale (30 Hz), the jitter is still about 1% and finally rises to 10% at 1 Hz (0.000003% of full scale). As the converter's operating frequency decreases toward the LTC1052's feedback-loop rolloff, the loop begins to dominate the jitter characteristic. In the high-frequency ranges, the loop poles are not a factor; instead, noise from the current source and Schmitt-trigger switching transitions predominate.

As in the wide-range V/F converter circuit (**Fig 7**), the feedback loop slows step response. The **Fig 9** photo illustrates this point: A full-scale input step requires almost 50 msec to settle. To trim **Fig 8**'s circuit, ground the input, and adjust the 1-Hz trim potentiometer until oscillation starts. Next, apply exactly 5V to the input, and set the 30-MHz trim potentiometer precisely for a 30-MHz output. Iterate this procedure until both points are fixed.

V/F converters are not the only types of data converters that can benefit from the LTC1052's performance. The circuit in **Fig 10** is a 16-bit A/D converter that provides 100,000 counts. *(Ed Note: A 16-bit integrating A/D converter always has a resolution of 65,536 counts.)* The converter, made up of two LTC1052s, a flip-flop, some gates, and a current sink, uses a current-balancing technique.

Once again, the chopper-stabilized LTC1052's 50-nV/°C input drift eliminates offset errors. The **Fig 10** photo shows the converter's waveforms. Assume the flip-flop's Q output (trace B) is low and therefore connects the LTC1043's pins 3 and 18. The current sink's output thus goes to ground. Under these conditions, the only current to IC_2's summing point comes from the input via the 95-kΩ resistor.

The positive input current forces IC_2's output (trace A) to integrate in a negative direction. The negative ramp continues and finally passes the 74C74 flip-flop's switching threshold. At the next clock pulse (trace C), the flip-flop changes state (trace B), and this event in turn causes the LTC1043's switch positions to reverse. Pin 3 connects to pin 15 to allow the current sink to bias IC_2's summing point.

This action results in a quickly rising, precise current flow out of IC_2's summing point. This current, scaled to

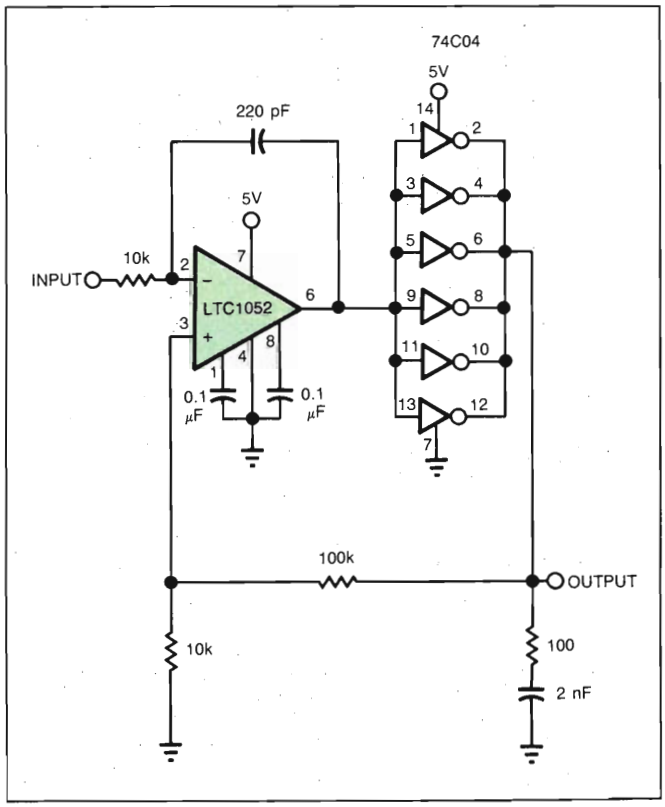


Fig 12—Using digital circuits for an analog function, *this configuration uses CMOS inverters to increase an amplifier's output-current capability. Contrary to their nature, the inverters operate in the linear region.*

Paralleled CMOS inverters provide an output-current capability as high as 20 mA.

be greater than the maximum input-derived current, forces IC_2's output ramp to reverse and integrate in the positive direction. At the first clock pulse after IC_2's output crosses the flip-flop's triggering threshold, switching occurs, and the entire cycle repeats itself.

Because the reference current is fixed, the flip-flop's duty cycle is solely a function of the input-signal current into IC_2's summing point. By gating the clock, the flip-flop's output produces the A_{OUT} frequency output. The 10-kΩ/10-pF network delays the clock signal slightly and, in so doing, eliminates spurious output pulses arising from flip-flop delay. Using counters, you can extract the circuit's data output (ie, the ratio of output A to the clock frequency).

Because the output is expressed as a ratio, frequency stability of the clock is unimportant. Minor parasitic charge pumping at the current switch introduces an error term that varies with operating frequency of the loop. This pumping effect, unless compensated, causes a small nonlinearity in the A/D converter's transfer function. To solve this problem, the remaining LTC1043 sections provide compensation by inverting the reference and returning a very small charge to the current sink's output each time the circuit switches.

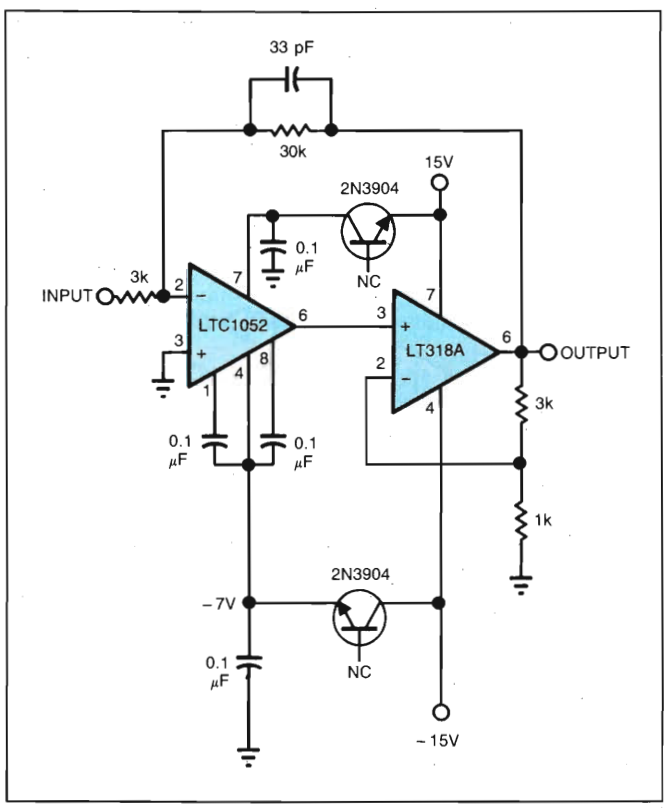


Fig 13—To enhance output current, *this circuit exploits the low offset and drift of the LTC1052 and the high output-current capability of the LT318A. Transistors, used as zener diodes, drop the ±15V supplies to levels that are acceptable to the LTC1052.*

The linearity trim scales the delivered charge to cancel the parasitic term. To calibrate the circuit, apply exactly 5V, and adjust the full-scale-trim potentiometer for 100,000 counts at the output. Next, set the input to 1.25V, and adjust the linearity-trim potentiometer for 25,000 counts. Iterate the procedure until both points are fixed. The converter's accuracy is ±1 count; its temperature coefficient is 15 ppm/°C typ. You can obtain a better temperature coefficient by using a more stable reference than the one discussed here.

Another application that exploits the LTC1052's low offset drift is a remote thermometer. Although many remote-thermometer circuits exist, few allow the direct transmission of the temperature transducer's output over an unshielded wire. The high output impedance of most transducers renders their outputs sensitive to noise on the line, which therefore requires shielding. The circuit in **Fig 11** offers one solution to this problem: Here, the low output impedance of a closed-loop op amp provides ideal line-noise immunity, while the op amp's offset-voltage drift assumes the temperature sensor's role.

Using the op amp in this way entails no external components and offers the advantage of a hermetically sealed package. The use of the AD547J op amp is arbitrary; any good amplifier with finite drift suffices for the application. The LTC1052 simply amplifies the op amp's offset drift to drive the meter. Because of the diode-bridge connection, you can use op amps with either positive or negative temperature-sensor drifts.

In the example shown, the circuit is configured for a 10 to 40°C output, although it can easily accommodate other ranges. To calibrate the circuit, place the op-amp sensor into a 10°C environment, and trim the 10°C-trim potentiometer for an appropriate meter indication. Next, perform a comparable operation at 40°C. Iterate the procedure until both points are fixed. Once calibrated, the circuit provides accuracy that's within ±2°C typ—even in high-noise environments.

In other circuit applications, you might need more output current or a wider voltage swing than the LTC1052 can provide. The IC's CMOS output stage can't provide the levels of current attainable in bipolar op amps. Furthermore, you might need to run the device from ±15V supplies in addition to requiring the increased current and voltage outputs. The circuit in

Fig 12 uses a package of paralleled CMOS inverters to provide an output-current capability as high as 20 mA.

The inversion in the loop demands that the feedback connect to the op amp's noninverting input. The RC damper at the output prevents oscillation in the parallel-inverter stage, which operates in its linear region. The local capacitive feedback around the amplifier provides loop compensation.

The circuit in **Fig 13** illustrates one way to run the LTC1052 from ±15V supplies and, at the same time, obtain the increased current- and voltage-output capabilities of the LT318A amplifier. The transistors operate as zener diodes by dropping the supplies to approximately ±7V at the LTC1052. The LT318A serves as an output stage with a voltage gain of four.

The output range is the same as that of the LT318A, ±13V into 2 kΩ typ with a short-circuit current of 20 mA. The circuit is dynamically stable at any gain in either the inverting or noninverting configuration. Be careful, however, not to exceed the LTC1052's input common-mode range: −7 to +5V with the ±15V power supplies used in this example. **EDN**

Author's biography

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and -instrumentation design. He has served in related capacities at National Semiconductor Corp, Arthur D Little Inc, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. Jim is a former student of psychology at Wayne State University, and he enjoys tennis, art, and collecting antique scientific instruments.

Design linear circuits for 5V operation

Although you often have to include linear circuit functions in predominantly digital systems, you no longer need to power the linear circuits from separate supplies. New components and design techniques let you power linear circuitry from the 5V logic rail.

Jim Williams, *Linear Technology Corp*

When you incorporate linear circuit functions in your digital system, you can avoid adding an extra supply just to power them. Instead, you can use analog components that furnish high performance when connected to the system's 5V logic supply.

Consider, for example, the LT1014 quad (or the LT1013 dual) op amps, which can operate from 5V supplies but whose specs compare favorably with those of the best ±15V op amps, and the LT1017/1018 Series dual comparators, which combine low power and high dc precision with speeds adequate for most applications. The common-mode range of these devices includes ground, which makes it easy to operate them from a single supply. (The nearby **table** summarizes the devices' specs.) In addition, the op amp's outputs can swing very close to the ground rail.

You can use such components to design signal-conditioning circuitry that operates from a 5V supply. **Fig 1** illustrates a scheme that provides complete, linearized signal conditioning for a platinum RTD that has a highly linear positive temperature coefficient. One side of the RTD sensor is grounded to minimize noise problems. The LT1004 2.5V reference establishes A_1's operating point, and A_1's output serves as a reference for the current source (Q_1 and Q_2).

The RTD is a constant-current device, so its voltage drop varies as a function of its resistance. A slight nonlinearity in the sensor's resistance curve causes several degrees of error over the circuit's 0 to 400°C operating range. A_2 amplifies R_P's output and simultaneously provides nonlinearity correction by feeding a portion of its (A_2's) output back to A_1's input via the 10-kΩ/250-kΩ resistive divider. Consequently, the current-source output shifts with R_P's operating point, compensating for sensor nonlinearity to within ±0.05°C.

A_3, which is also referenced to the LT1004, conditions the offset signal at A_2's inverting input so that 0V at A_2's output is equal to 0°C. The resistive divider at A_4's noninverting input establishes circuit gain.

You can calibrate this circuit by substituting a precision decade resistance box (eg, GenRad's 1432K) for R_P. You set the box for 100Ω (0°C value) and adjust the offset trim for a 0V output. Then you set the box for 154.26Ω (140°C), and adjust the gain trim for a 1.4V output. Finally, you set the decade box at 249Ω (400°), and trim the linearity adjustments until the circuit output equals 4V. By repeating this sequence until you fix all three points, you'll establish a total error range of

BASIC SPECS FOR THE LT1014 AND LT1017/1018 COMPONENTS

PARAMETER	LT1014	LT1017/1018
E_{OS} (μV)	150	500
E_{OS} TC (μV/°C)	2	5
BIAS CURRENT (nA)	20	100
SUPPLY CURRENT (μA)	500	60 (1017) 240 (1018)
GAIN	1.5×10^6	10^6
COMMON-MODE RANGE (V)	0 TO (V_S-1.5V)	0 TO (V_S-1.4V)
SUPPLY VOLTAGE (V_S)	3.4 TO 40V	1.2 TO 36V
NOISE (0.1 TO 10 Hz)	0.55 μV p-p	—
RESPONSE TIME (μSEC)	—	1 (1018)
OUTPUT CURRENT	—	25 mA PULL DOWN 60 μA PULL UP
OUTPUT SWING (V) NO LOAD 600Ω LOAD	 0.025 TO (V_S-1V) 0.01 TO (V_S-1.6V)	—

±0.05°C max over the entire temperature range.

Although the resistance values in **Fig 1** are for a sensor with a nominal 0°C resistance of 100Ω, you can use sensors with different nominal resistance values by factoring in the deviation from 100Ω. This deviation, specified by the manufacturer for each individual sensor, is an offset term that's caused by winding tolerances during RTD fabrication. The gain slope of platinum is primarily fixed by the purity of the material, and it represents a very small error term.

Fig 2 illustrates a second signal-conditioning circuit, this one for a thermocouple. The design features cold-junction compensation; one leg of the thermocouple is grounded, which minimizes noise problems. One switch section of the LTC1043 combines the compensation network's differential output with the thermocouple's output at the input of the LTC1052.

The 1043's second switch section generates a small negative potential, which allows the 1052's output stage to operate as a class A amplifier for low-level outputs, permitting a swing to zero volts.

The table in **Fig 2** lists optimum resistance values for various thermocouple types. By adjusting the R_F/R_I divider ratio, you can set output scaling to whatever slope you desire. Over a 0 to 60°C range, cold-junction compensation holds to within ±1°C.

Condition a pressure-transducer output

You can also signal-condition the bridge output of a strain-gauge pressure transducer **(Fig 3)**. Despite the 2-amplifier circuit's simplicity, it provides an auxiliary

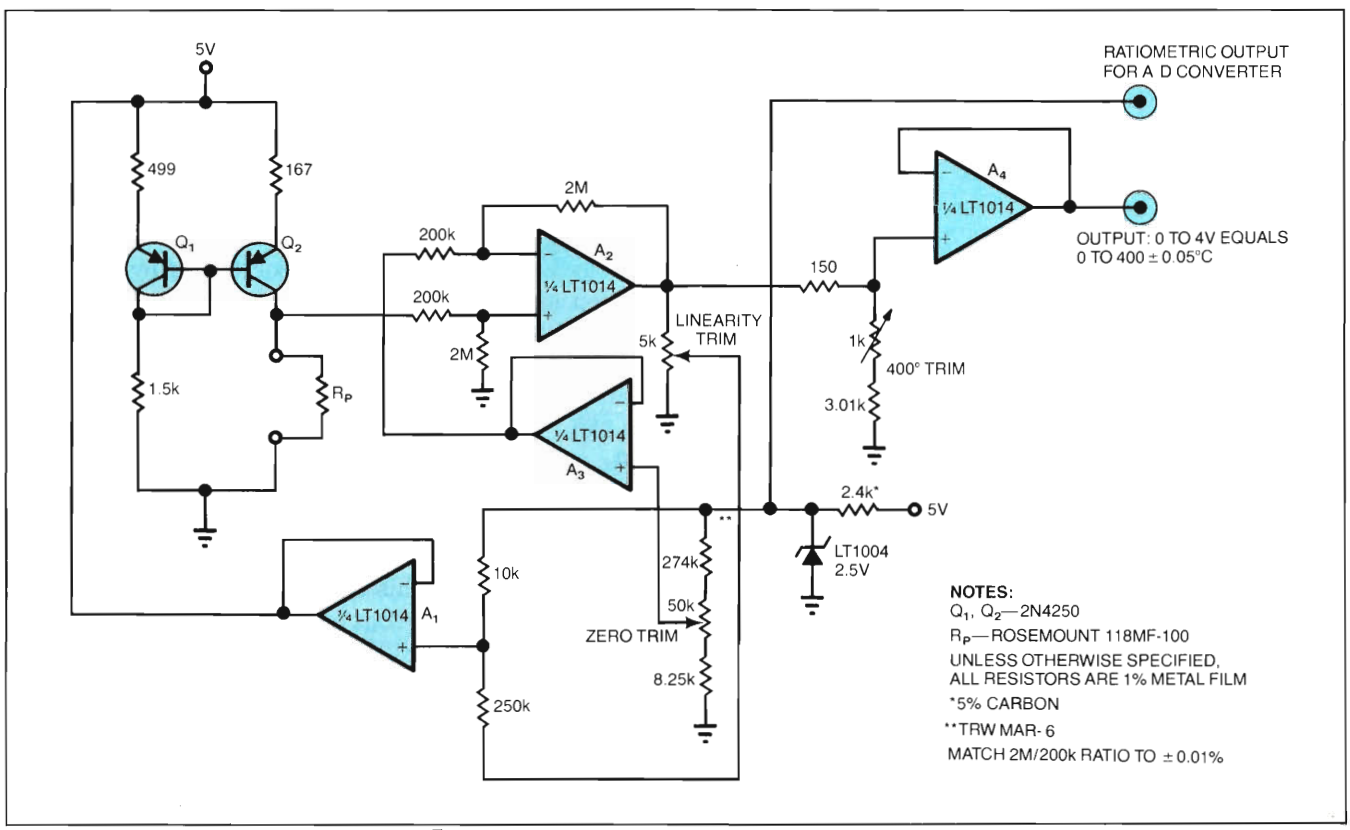


Fig 1—To minimize noise problems, *this signal-conditioning design scheme grounds one side of the RTD sensor.*

Theoretically, transducers with single-ended outputs don't require a differential-input instrumentation-type amplifier.

ratio output for a monitoring A/D converter, and it minimizes the need for precision resistors.

A_1 provides bias for the LT1044 positive-to-negative converter. As the 1044's output pulls the bridge output negative, it balances A_1's input at 0V. Thanks to this local-loop action, a single-ended amplifier (A_2) can handle the bridge's differential output.

A_2's gain is set to provide the desired output scale factor. The RC network at the amplifier's input provides noise filtering. Because the LT1004 reference provides the bridge drive, power-supply shifts have no effect on A_2's output.

To calibrate this circuit, apply (or electrically simulate) 0 psi, and trim the zero adjustment for 0V output. Next, apply (or electrically simulate) 350 psi, and trim the gain for 3.5V output. Repeat these adjustments until you fix both points.

Taking care of detection needs

The circuit in **Fig 4a** may look like just another scheme for signal conditioning; however, besides signal conditioning, it performs a more complex mathematical operation: It monitors the methane level detected by the specified transducer (the circuit's frequency output is directly proportional to the methane level). The transducer output varies approximately as

$$\frac{1}{\sqrt{\text{CONCENTRATION}}}, \qquad (1)$$

and the circuit linearizes this function.

A_1 converts the sensor's resistance value (vs methane concentration) to a voltage and feeds A_2. The LT1004 serves as a reference. The exponential relationship between a transistor's V_{be} and its collector current is used to generate a current in Q_3's collector that's proportional to the square of A_2's input current. This operation compensates for the sensor's square root term. Q_3's collector current establishes the operating point for the oscillator (A_3, A_4).

A_3, an integrator, generates a positive-going linear ramp (trace A in **Fig 4a**). The summing point at A_4 (trace B) compares the ramp with Q_3's current. A_4 is configured as a current-summing comparator (the diode-bound feedback network minimizes delay caused

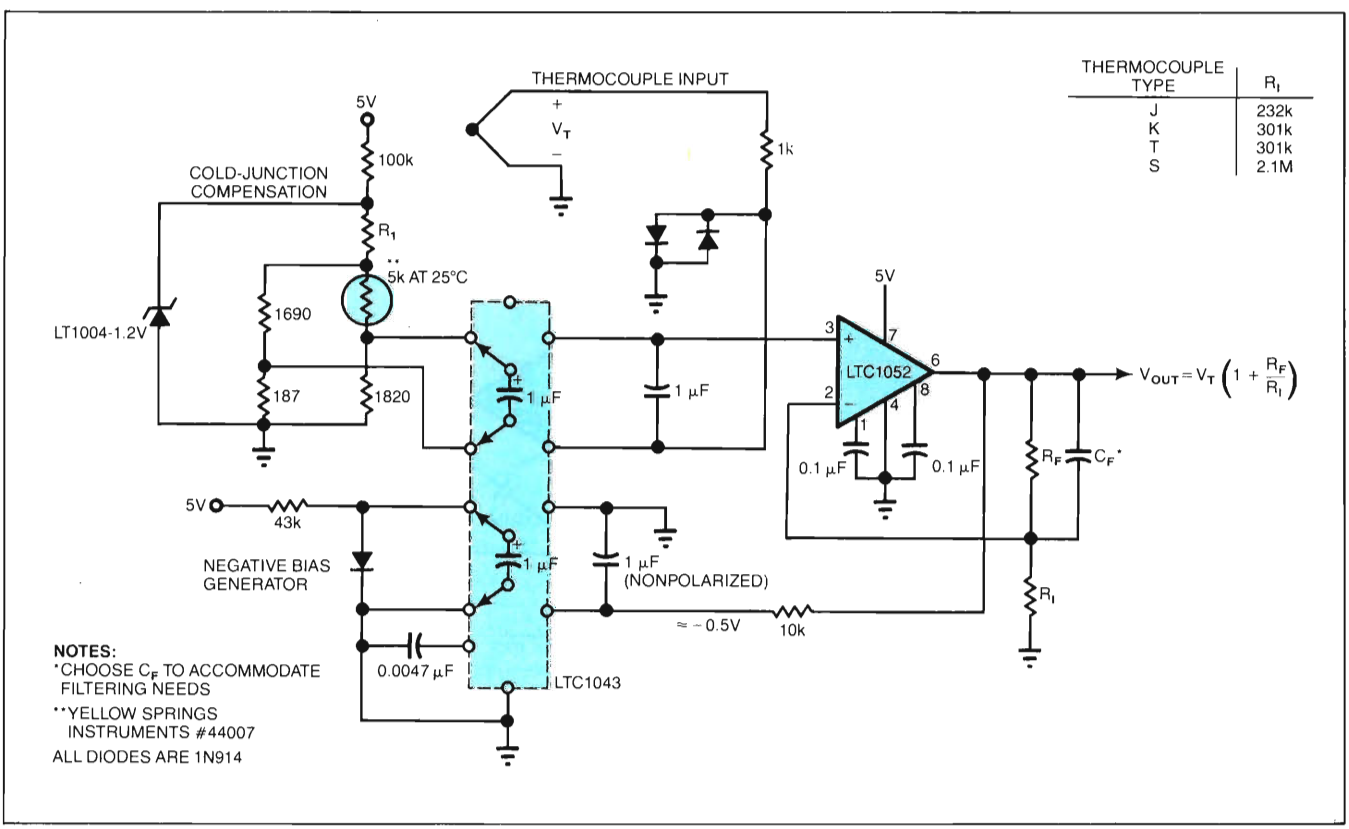


Fig 2—Featuring cold-junction compensation, *this signal conditioner works with a variety of thermocouple types.*

Clean supplies are not the rule in the digital world, they are the exception.

by output slew time). When the ramp forces the summing point positive, A_4's output (trace C) swings negative. The output of CMOS inverter A (trace D) goes high, turning on the C4016 switch to reset the integrator.

At the same time, the output of inverter B (trace E) goes low, supplying positive ac feedback to A_4's noninverting input (trace F). When the positive feedback decays, A_4's output goes high, enabling the integrator, and the entire cycle repeats.

Q_3's collector current determines how long A_3 generates the ramp before it's reset by A_4. The ramp time is directly proportional to Q_3's collector current; thus, the oscillation frequency is inversely related to the current.

The transfer function for the overall circuit takes the form $1/X^2$, which, in theory, should linearize the sensor's output. In practice, the sensor response deviates slightly from the ideal, and is actually

$$\frac{1}{\sqrt[1.9]{\text{CONCENTRATION}}} \qquad (2)$$

The reset time constants at A_4's input introduce enough oscillator down time to partially compensate for the deviation. Because the oscillator's down time retards frequency shifts, it affects the oscillator's high frequencies, providing a first-order compensation. The overall linearization achieved (**Fig 4b**) is within the sensor's manufacturing tolerances. The slight bump in the circuit's response curve is caused by the mismatch between the denominator terms of the sensor-response expression (**Eq 1**) and the circuit's transfer function. The down-time correction in the oscillator smoothes this error out above 4000 ppm.

The LT1044 voltage converter generates a negative supply voltage directly from the 5V rail. The sensor's heater is powered from the 5V rail, as the manufacturer specifies. To calibrate the circuit, place the sensor in a 1000-ppm-methane environment and adjust the 5-kΩ trimmer to develop a 100-Hz output. Circuit accuracy from 500 to 10,000 ppm is limited by the sensor's 10% specification.

Taking care of noise problems

Although many transducer-based analog functions are compatible with 5V-power-supply operation, you shouldn't overlook a source of possible trouble: noise. Theoretically, transducers with single-ended outputs don't require differential-input instrumentation-type amplifiers. In many applications, however, common-

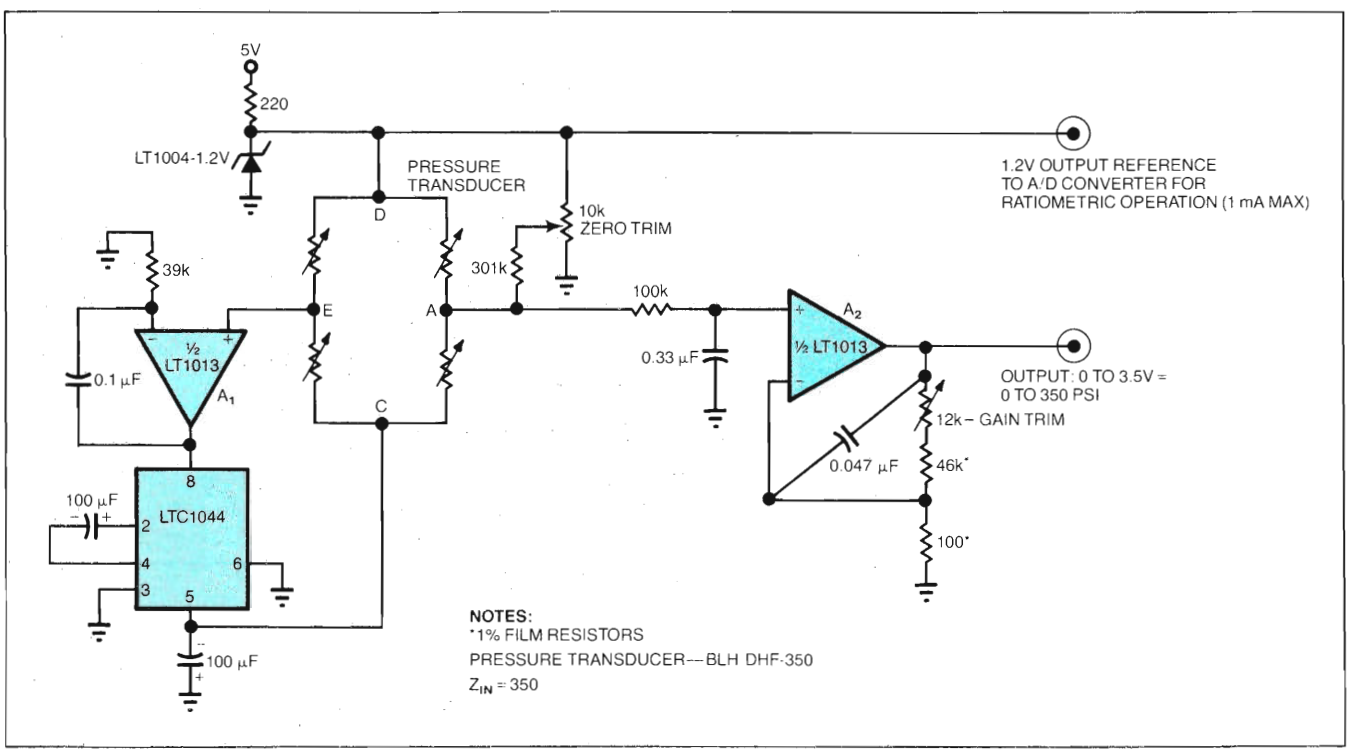
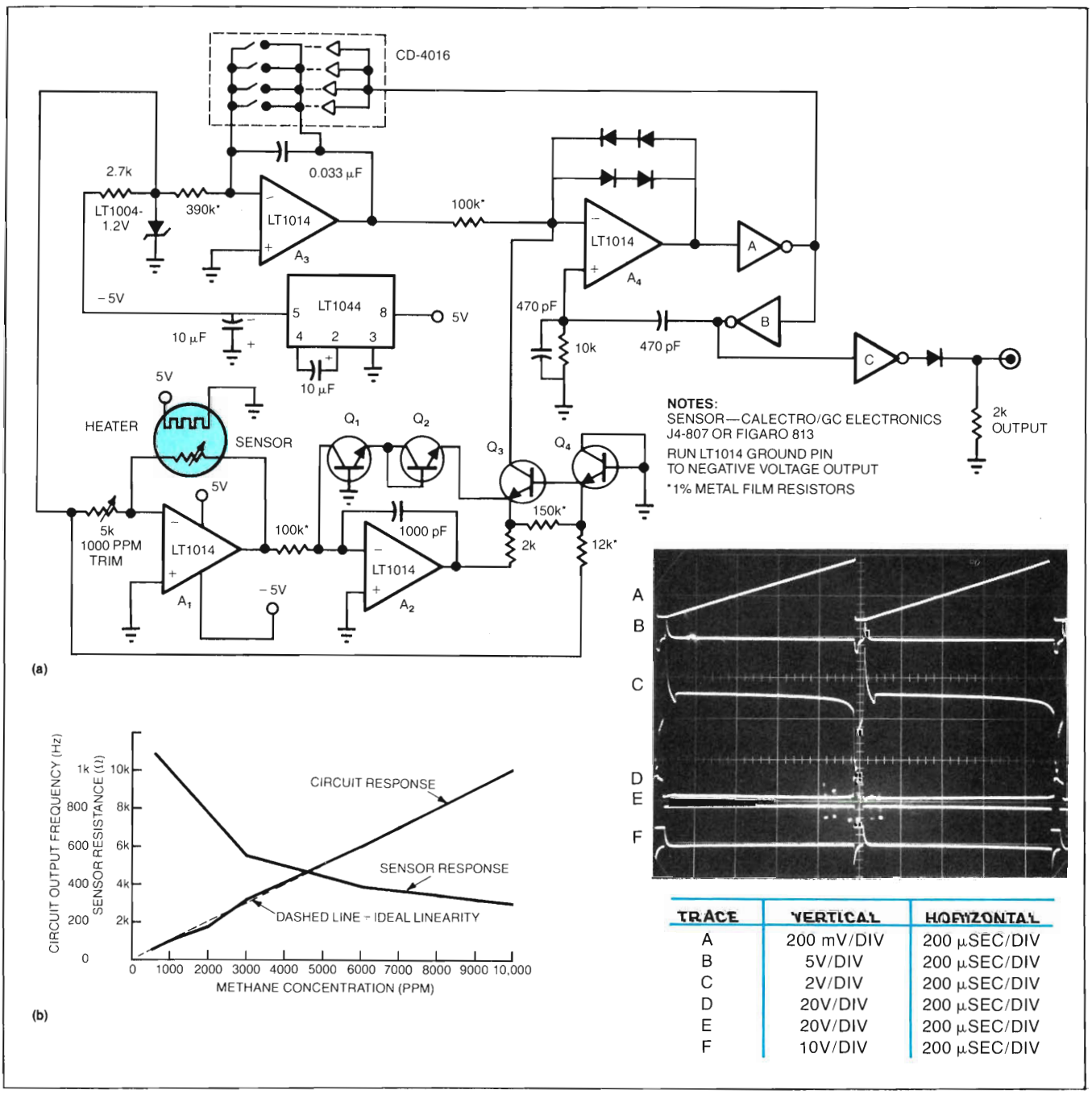


Fig 3—Despite its simplicity, *this circuit, which conditions a strain-gauge pressure transducer's output, minimizes the need to use precision resistors; in fact, you don't have to worry about resistor matching at all.*

mode noise is often larger than the signal of interest, so most transducer-based systems do employ instrumentation-type amplifiers.

If you need such an amplifier, you'll have to build your own, because no commercially available instrumentation amplifier will function from a 5V supply. You can use the circuits in **Fig 5** to build an instrumentation amplifier. The circuits feature input protection, filtering capability, and a shield-driver output.

In **Fig 5a**, A_1, A_2, and A_3 provide the differential-input to single-ended-output conversion; R_G sets the gain. Because of the offset and drift performance of this



TRACE	VERTICAL	HORIZONTAL
A	200 mV/DIV	200 µSEC/DIV
B	5V/DIV	200 µSEC/DIV
C	2V/DIV	200 µSEC/DIV
D	20V/DIV	200 µSEC/DIV
E	20V/DIV	200 µSEC/DIV
F	10V/DIV	200 µSEC/DIV

Fig 4—To linearize transducer output, *this detector circuit* ***(a)*** *takes advantage of the exponential relationship between a transistor's* V_{be} *and its collector current. Overall circuit linearization* ***(b)*** *is within the sensor's manufacturing tolerances.*

One key to achieving good design results is to consider power bus routing an integral part of the signal-processing chain.

circuit, the circuit will accommodate low-level transducers such as thermocouples and strain gauges.

The RC networks at the inputs filter out noise and 60-Hz pickup—the LT1014 is never exposed to high-frequency common-mode noise. The transistors and Schottky clamp diodes combine with the 100-kΩ resistors to prevent high voltage spikes or faults, which are common in industrial environments, from doing any damage to the circuit. To reduce the effects of input-cable capacitance, you can use A_4 to drive the cable shield at the input common-mode voltage level, which is derived from the output of the input amplifiers.

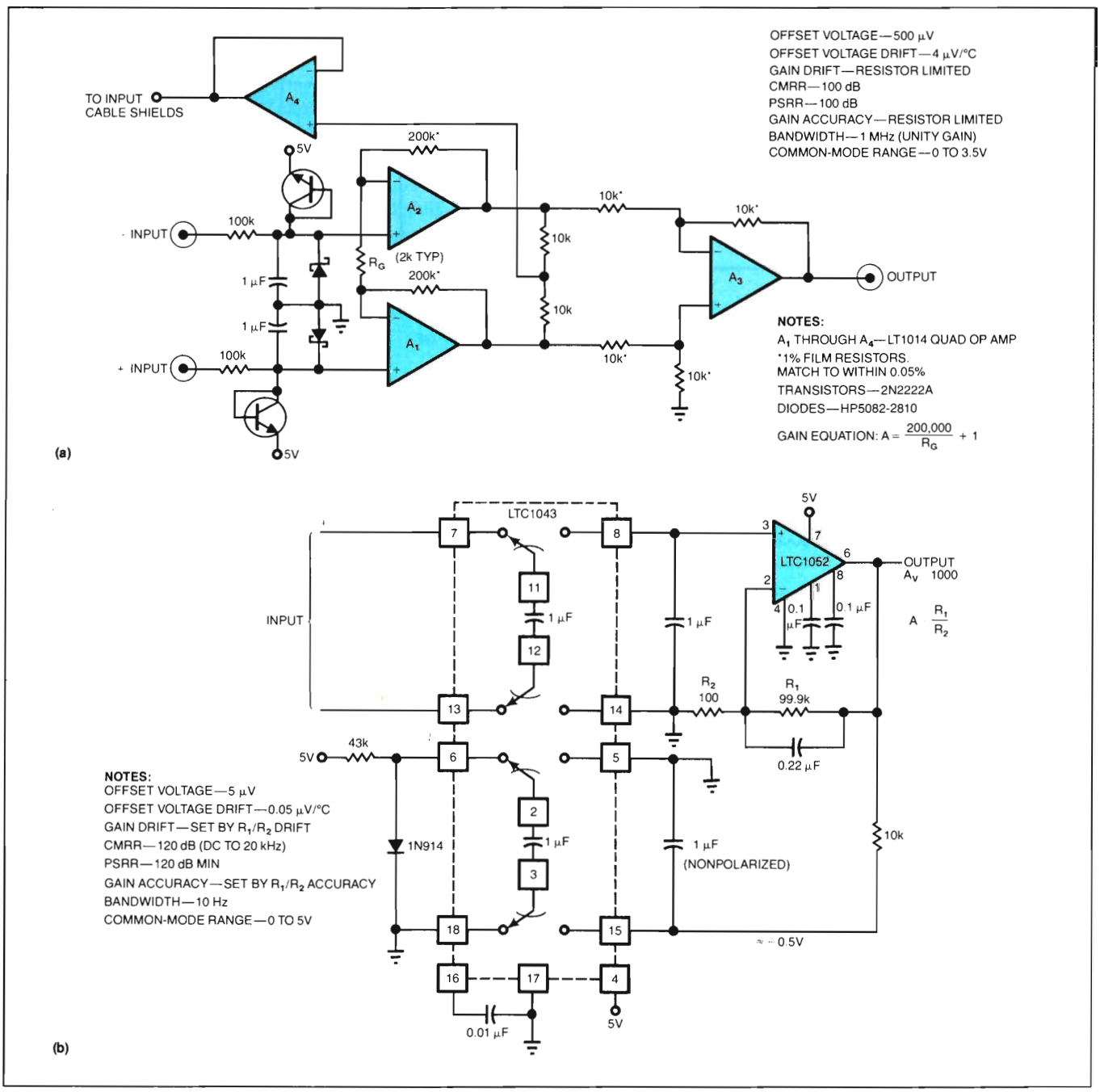


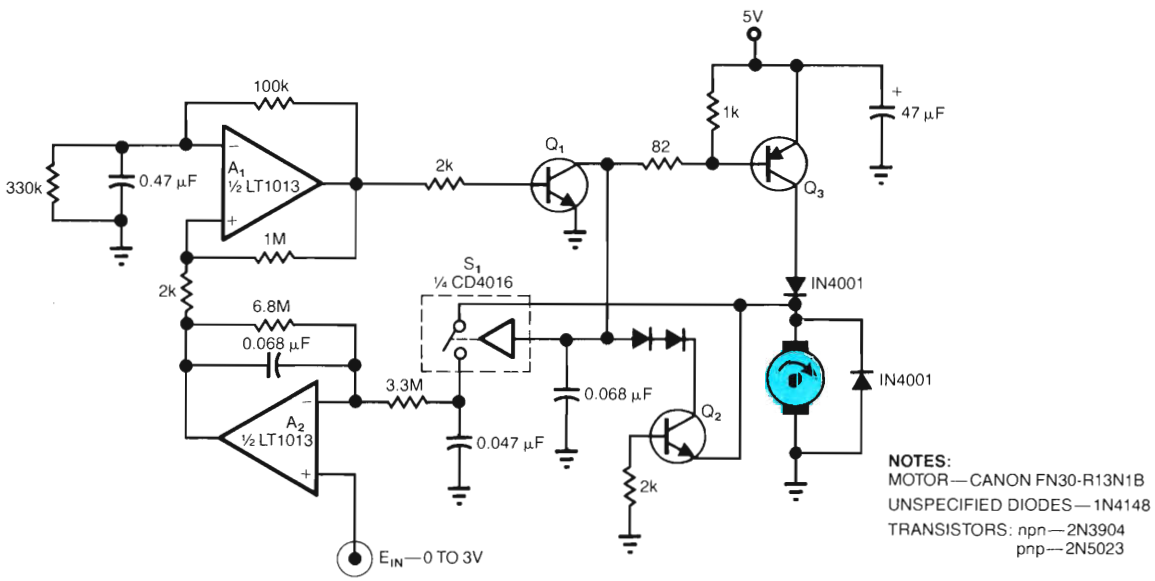
Fig 5—Input protection and filtering capability *are key features of these instrumentation-type amplifiers. What circuit you select depends on your application. You can opt for wide bandwidth* ***(a)*** *or trade bandwidth for high dc precision* ***(b).***

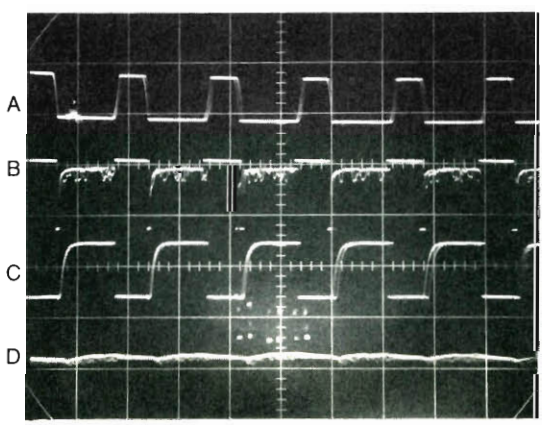
If you need a wider bandwidth, use the circuit in **Fig 5a**. If you need higher dc precision, use the circuit in **Fig 5b**, in which one section of an LTC1043 switched-capacitor building block provides the differential-to-single-ended conversion by alternately commutating a 1-μF capacitor between the circuit input and the LTC1052's input. This scheme allows the 1052 to make measurements referenced to ground. The 1043's other switch section generates a small negative potential, allowing the 1052 output to swing all the way to 0V.

Although the circuit bandwidth is limited to 10 Hz, dc precision is excellent, surpassing that available in all monolithic ±15V instrumentation amplifiers. The LTC1043's switching action, set at about 400 Hz by the 0.01-μF capacitor, simulates the performance of a low-pass filter. The switching action provides a high degree of noise rejection—CMRR specs in excess of 120 dB at 20 kHz.

You can also power circuits like motor controllers, current-loop transmitters, dc/dc converters, limit comparators, and A/D converters from the 5V logic rail. Of course, these applications will require novel designs. The circuit in **Fig 6**, for instance, provides a means of servo-controlling the speed of a dc motor. Because it operates from the 5V logic supply, this design doesn't require additional motor-drive supplies. The circuit senses the motor's back EMF to determine the motor's speed. It uses the difference between the speed and an established set point to close a sampling loop around the motor.

Specifically, A_1 generates a pulse train (trace A in **Fig 6**). When A_1's output is high, it turns on Q_1, and Q_3





TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	1 mSEC/DIV
B	5V/DIV	1 mSEC/DIV
C	5V/DIV	1 mSEC/DIV
D	5V/DIV (AC COUPLED)	1 mSEC/DIV

Fig 6—Offering a 20-rpm to full-speed control range, *this circuit senses a motor's back EMF to determine the motor's speed.*

Galvanically isolating the linear circuits is probably the most effective way to deal with digital-supply noise.

Using logic supplies

Operating linear components from logic supplies can be difficult because of the fast clocking and transient high currents characteristic of digital systems. One key to achieving good design results when you're running linear components from 5V supplies is to consider power-bus routing as an integral part of the signal-processing chain.

As **Fig A** shows, supply-rail impedances cause both dc and ac errors at various points in a system. This is true of any power distribution scheme, but it's especially troublesome in digitally oriented systems where fast current spiking and clock harmonics are present.

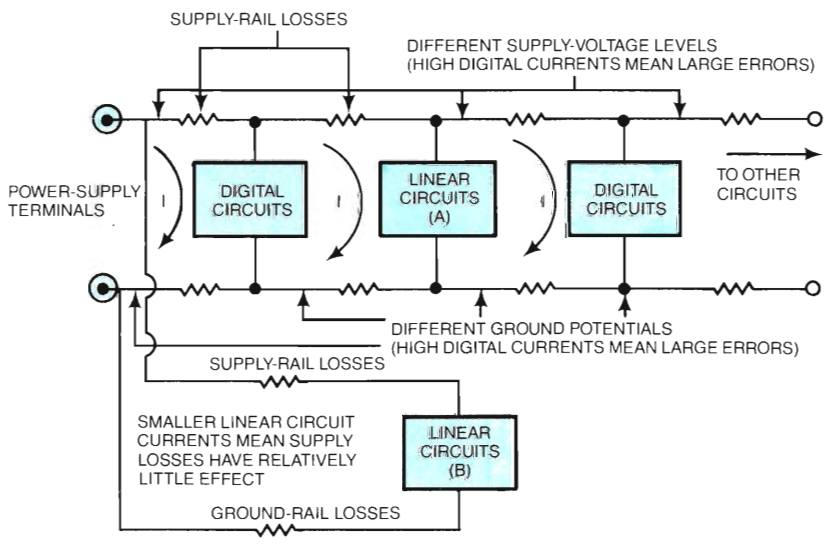
Circuitry located at position A, for example, will experience appreciable positive rail noise, and the relatively high currents returning through conductor impedances will corrupt the ground potential. Although you can reduce positive rail noise by bypassing the supply, ground-potential uncertainty can still cause unacceptable errors.

Locating linear circuits as shown at position B eliminates the digitally related currents and reduces both positive- and ground-rail problems. The linear device's lower operating current leads to fewer errors resulting from supply-distribution impedances.

For supply bypassing, LC filters are substantially more effective than simple capacitors are, especially in designs in which it's not practical to route the positive rail directly from the supply. When you use RC filtering, voltage drops across the resistor, but this is often acceptable because most linear components have low power requirements.

In many cases it's impossible to develop a clean power supply for the linear components. In such circumstances, it may be possible to have all noise-sensitive linear circuit operations occur between system clock pulses. This approach takes advantage of the synchronous nature of most digital systems. Also, supply bus disturbances are often at a minimum between clock pulses.

Finally, galvanically isolating the linear circuits is probably the most effective way to deal with digital-supply noise.



BYPASSING TECHNIQUES

TYPE	COMMENTS
+V	SIMPLE
+V, TO RAIL	THIS APPROACH IS MORE COMPLEX, BUT IT PROVIDES GOOD HIGH-FREQUENCY REJECTION WITH LOW DC LOSSES. INAPPROPRIATE FOR USE WITH FAST LINEAR CIRCUITRY.
+V, TO RAIL	THE RC FILTER IS EFFECTIVE FOR HIGH-FREQUENCY REJECTION, BUT IT HAS DC LOSSES. YOU CAN USE THIS APPROACH WITH LOW-CURRENT LINEAR CIRCUITS. DON'T USE THIS APPROACH WITH FAST LINEAR CIRCUITRY.

***Fig A—Errors caused by supply-rail impedances** are a major problem in digitally oriented systems where fast current spiking and clock harmonics are present.*

drives the motor's ungrounded terminal (trace B). When A_1 goes low, Q_3 turns off, and the motor's back EMF appears at the motor terminals after the inductive flyback ceases. During this period, S_1's input (trace C) turns on, and the 0.047-μF capacitor charges to the value of the back EMF. A_2 compares this value with the setpoint level, and the amplified difference (trace D) changes A_1's duty cycle to control motor speed. A_2 has the desirable characteristic of assuming unity gain when there's no feedback signal; as a result, start-up or input overdrive, which causes the loop to lose control of motor speed, cannot force the sampling loop to experience servo lock-up. The loop is self-restoring; that is, it will re-establish control over the motor speed when abnormal conditions cease.

For the circuit to operate properly, you must carefully control S_1's input signal. Q_2 prevents switch closure until the negative-going flyback interval is over, and the 0.068-μF capacitor slows the switch's turn-on speed. These measures ensure that the signal the circuit applies to the 0.047-μF storage capacitor will be clean. The diodes in Q_2's collector compensate for the motor's clamp-diode drops, ensuring that no destructive negative voltages appear at S_1's input. This circuit's control range extends from 20 rpm to full speed.

Note that the gain and roll-off terms in A_2's feedback loop are optimal for the motor shown; if you use a different motor, you have to change the values of the components in the feedback loop.

Generally, process-control circuitry used in industrial environments must transmit standard 4- to 20-mA current-loop signals to valves and other actuators. Because of resistive line losses and actuator impedances, industrial current-loop transmitters must be able to develop at least a 20V drive capability. Systems that operate from 5V usually don't meet this requirement.

The circuit in **Fig 7**, however, does meet industrial current-loop-transmitter requirements. The circuit's design uses a servo-controlled dc/dc converter to generate the compliance voltage necessary to meet current-loop requirements. The circuit can drive 4- to 20-mA signals into loads as high as 2200Ω (44V compliance), and it's inherently short-circuit protected.

Fig 7's amplifier A_2 accepts the circuit input and biases the noninverting input of A_1 via the offsetting

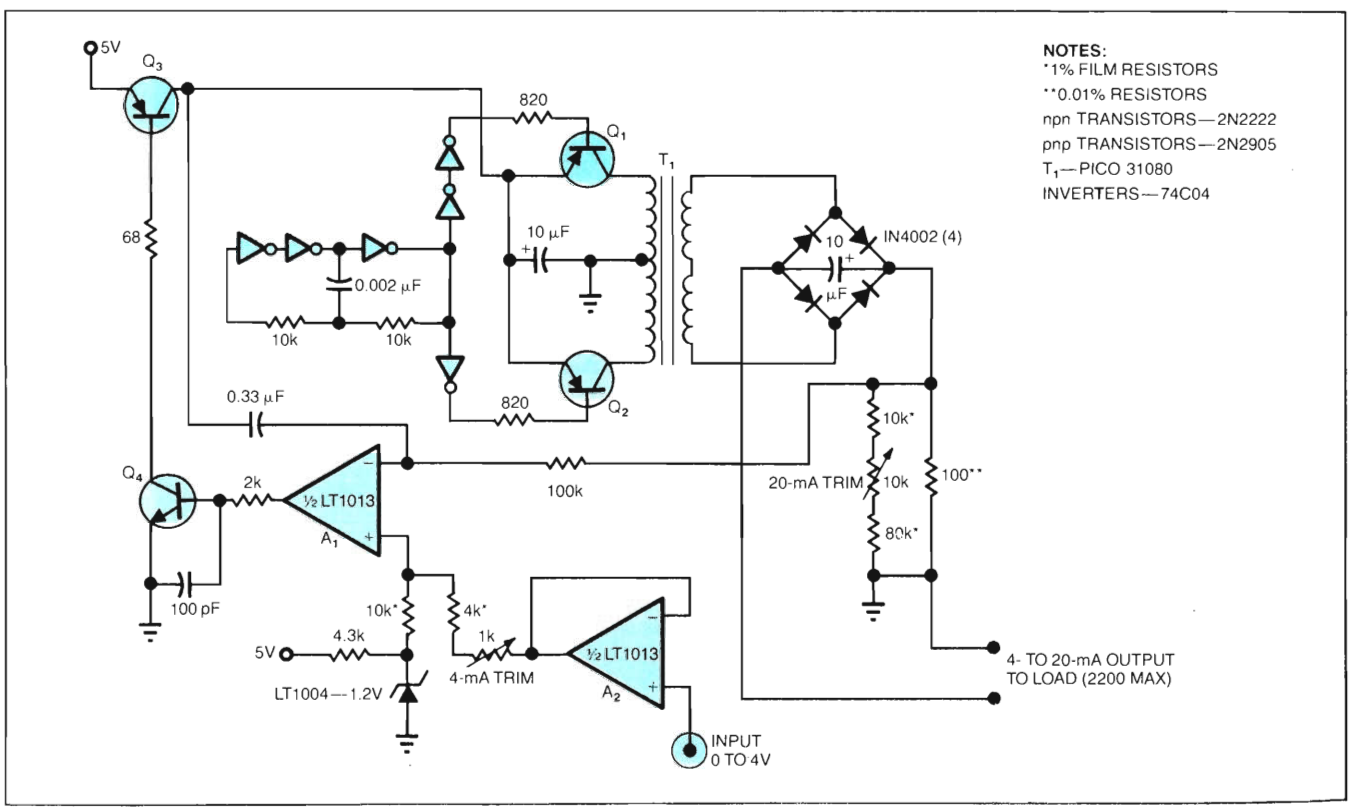


Fig 7—Using a dc/dc converter to generate the required compliance voltage, *this loop transmitter, which operates from a single 5V supply, can drive 4- to 20-mA current signals into loads as high as 2200Ω.*

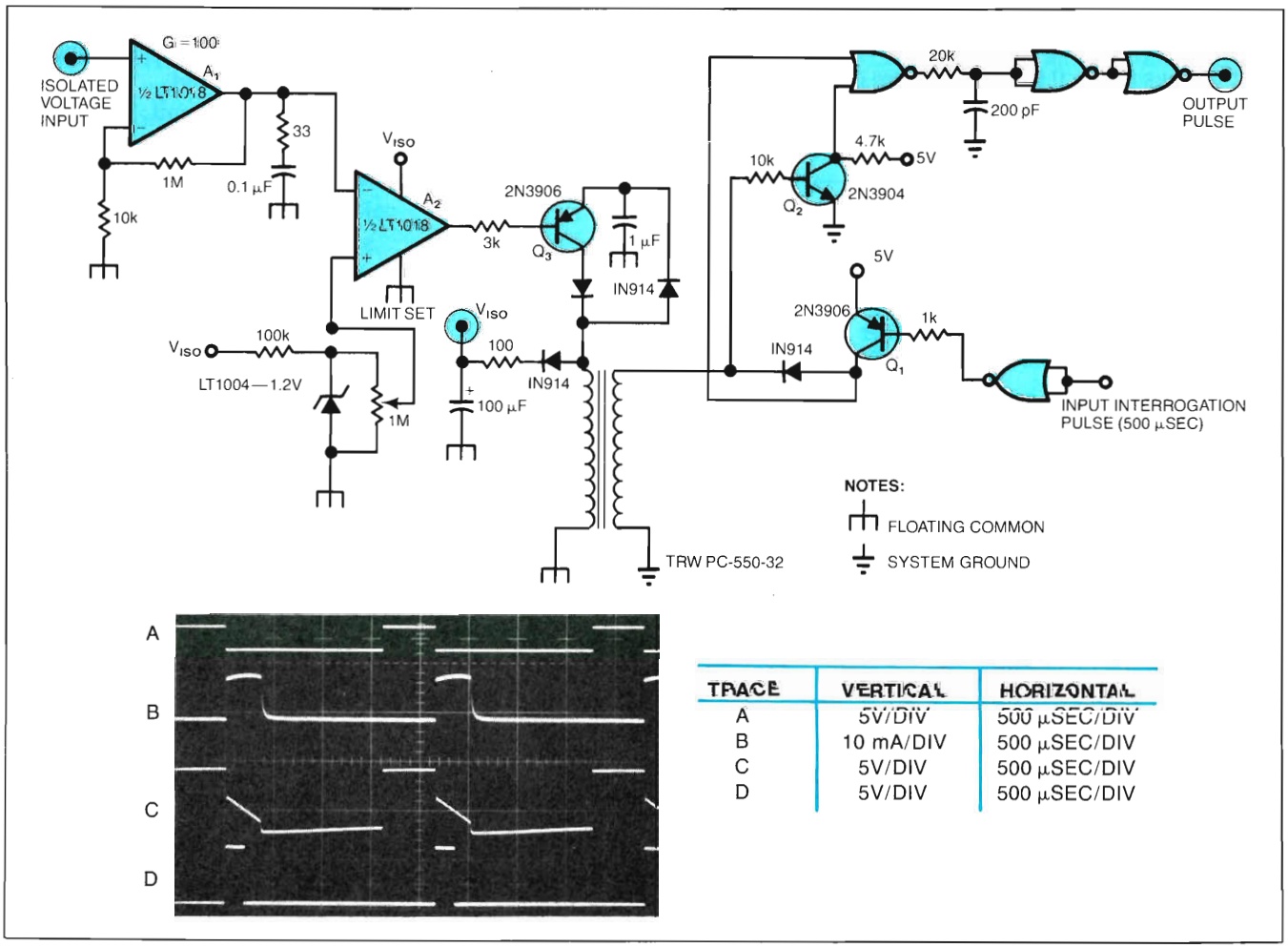
A move to lower power-supply voltages for digital circuits underscores the need for low-voltage, high-performance linear ICs.

network. A_1's output goes high, turning on Q_4 and Q_3. Q_3's collector drives the dc/dc converter (T_1, Q_1, Q_2), which the RC-gate oscillator clocks. T_1 steps up the voltage, and after rectification and filtering, secondary current flows through the 100Ω resistor and the load. A_1's inverting input measures the voltage across the 100Ω resistor, completing a current-control loop around T_1. The 0.33-μF capacitor provides stable loop roll-off, and the 100-pF capacitor suppresses local oscillation at Q_4. A_1 maintains constant output current within the compliance limit, regardless of load impedance shifts or supply changes.

Calibrating this circuit is a straightforward process. First, you short the output, apply 0V to the input, and adjust the 4-mA trim to develop 0.3996V across the 100Ω resistor. Next, shift the input level to 4V and adjust the 20-mA trim for 1.998V across the 100Ω resistor. Repeat this procedure until you fix both points. The odd voltage-trim target values result because the gain trim network shunts the 100Ω resistor.

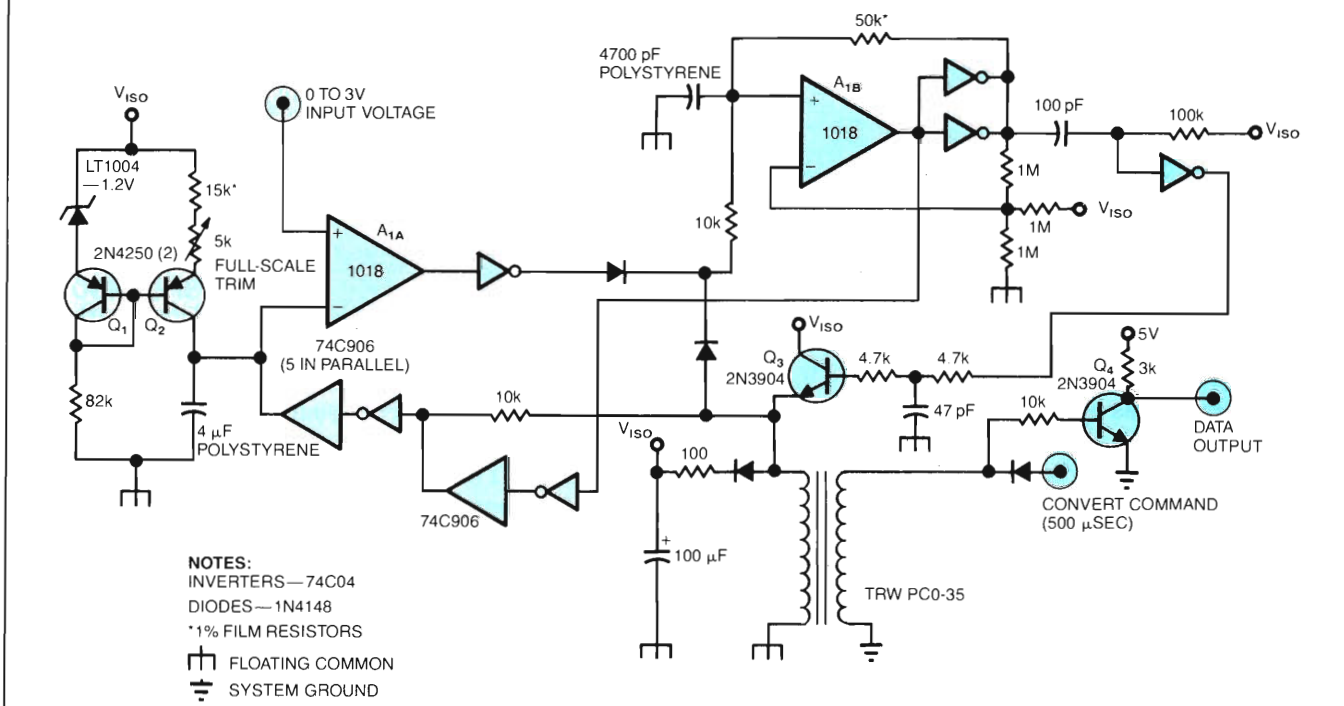
Another difficulty with operating analog circuits from 5V supplies is that such supplies are not often clean ones. The circuit in **Fig 8** minimizes the noise problems by performing a fully isolated limit comparison on low-level signals. It produces a digital output that indicates whether the input is above or below a preset limit. The circuit is well suited for process-control applications in which transducers operate at high common-mode voltages or in which large ground loops exist. The damper network in A_1's output allows it to function as an op amp for low-level signals, so this circuit will accommodate thermocouples and other low-level sources.

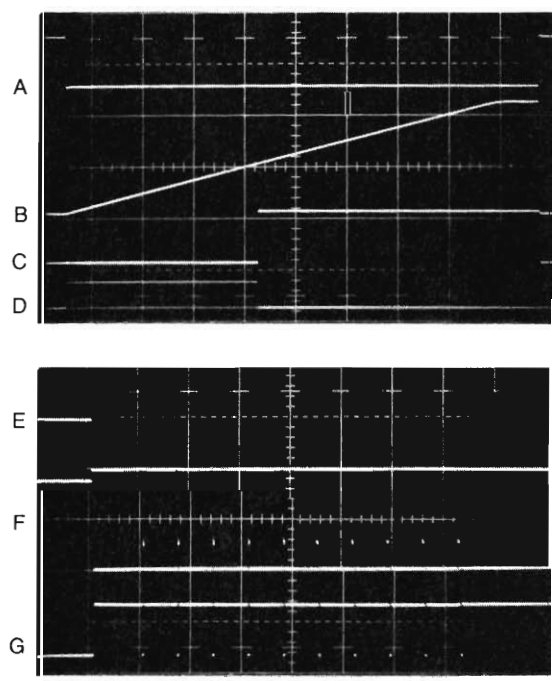
Fig 8's circuit functions by echoing an interrogation



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	500 μSEC/DIV
B	10 mA/DIV	500 μSEC/DIV
C	5V/DIV	500 μSEC/DIV
D	5V/DIV	500 μSEC/DIV

***Fig 8—Suitable for process-control** applications where transducers operate at high common-mode voltages, this circuit produces a digital output that indicates whether the input is above or below a preset limit.*





TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	50 mSEC/DIV
B	2V/DIV	50 mSEC/DIV
C	5V/DIV	50 mSEC/DIV
D	10V/DIV	50 mSEC/DIV
E	5V/DIV	500 μSEC/DIV
F	2V/DIV	500 μSEC/DIV
G	5V/DIV	500 μSEC/DIV

Fig 9—Completely floating from system ground, *this 10-bit A/D converter is useful in industrial environments, where noise and high common-mode voltages in transducer-driven systems are common problems. Scope-photo traces A, B, C, and D are described in the text; trace E shows the convert-command pulse; trace F, the transformer primary; and trace G, the TTL-compatible pulses at Q_4's collector.*

Linear components should not sacrifice performance when operating from logic supplies.

pulse only when the input is above the preset level. The transformer helps to establish a 2-way, galvanically isolated signal path; the energy contained in the interrogation pulse serves to power the circuits' floating elements.

When you apply an input interrogation pulse, Q_1's collector drives the transformer primary (trace A in **Fig 8**). If the input level is above the preset limit, comparator A_2's output will be low, biasing Q_3 on and allowing Q_3 to drive current into the transformer secondary (trace B). This current reflects into the transformer primary (trace C), where it's detected by a demodulator (Q_2 and its associated gate circuitry) that produces an output pulse (trace D). If A_2's output is high, the transformer receives no secondary drive and there's no output pulse.

The high common-mode noise that's characteristic of predominantly digital systems also poses problems for data converters. Because it completely floats from system ground, the 10-bit A/D converter shown in **Fig 9** solves the noise problem. The circuit readily accommodates high common-mode noise. The design is also useful in industrial environments, where noise and high common-mode voltages in transducer-driven systems are common problems.

You initiate circuit operation by applying a pulse to the convert-command input (trace A in **Fig 9**). The pulse appears at the transformer secondary and charges the 100-μF capacitor. This capacitor potential provides the supply voltage for the floating A/D conversion circuitry. The secondary's pulse provides two additional functions—it biases the inverter/open-drain buffer combination to discharge the 4-μF capacitor (trace B), and it biases a diode to disable the oscillator's (A_2's) 3-kHz output (trace D).

At the same time, A_1's output goes high, forcing the inverter in its output line to switch to a low state (trace C). When the convert-command pulse ceases, the current source (Q_1 and Q_2) charges the 4-μF capacitor with a linear ramp and enables the oscillator. When the ramp voltage exceeds the value of the input voltage, A_1's output goes low, and the inverter in its output line switches to a high state, disabling the oscillator.

The number of oscillator pulses that occur during this interval is proportional to the value of the input voltage. The differentiator at Q_3's base differentiates the oscillator pulses and feeds them to transformer driver Q_3. The spike transformer-drive scheme eases the power drain on the 100-μF energy-storage capacitor. The RC delay in Q_3's base, in conjunction with the inverter/buffer combination at A_{1B}'s output, prevents Q_3's emitter pulses from triggering a ramp reset.

Several factors contribute to the 10-bit performance of this circuit. The 4700-pF and 4-μF polystyrene capacitors both have −120-ppm/°C temperature coefficients. As a result, overall circuit gain drift is about 25 ppm/°C. The five 74C906 open-drain buffers in parallel provide an effective 0V reset for the 4-μF capacitor, thus minimizing offset errors that occur during reset. The parallel inverters in A_{1B}'s output line reduce errors related to saturation, thereby stabilizing the oscillator against shifts in supply voltage and temperature.

Finally, by synchronizing the oscillator with the conversion sequence, the diode path at Q_3's emitter prevents a ±1-count uncertainty error. The 5-kΩ potentiometer in the current source trims calibration so that a 3V input develops an output of 1024 counts. The transformer (TRW PCO-35) allows the converter to function at common-mode levels ranging to 175V. The circuit requires 330 msec to complete a 10-bit conversion and drifts less than 1 LSB over 0 to 50°C.

A move to lower voltages for digital circuits, which must occur, underscores the need for low-voltage, high-performance linear ICs. After all, increasing circuit-density requirements will dictate that digital-supply output levels decrease, lowering the IC breakdown requirements. And users will require new equipment to be portable, so its circuitry will have to be directly compatible with battery potentials.

However, linear components must not sacrifice performance to function in this low-voltage, digitally driven environment. Despite their narrower dynamic operating range, low-voltage linear circuits must still be able to provide the same precision that higher-voltage devices provide. **EDN**

Author's biography

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and -instrumentation design. He has served in related capacities at National Semiconductor Corp, Arthur D Little Inc, and the Instrumentation Development Lab at the Massachusettts Institute of Technology. Jim is a former student of psychology at Wayne State University, and he enjoys tennis, art, and collecting antique scientific instruments.

Design techniques extend V/F-converter performance

A number of design techniques can help you build V/F converters that suit your special applications. This article, part 1 of a 2-part series, covers some general design choices and describes in detail three circuits that show improved speed, dynamic range, and stability compared with commercial devices. Part 2 will detail circuits that feature improved linearity, low-voltage operation, sine-wave output, and nonlinear transfer functions.

Jim Williams, *Linear Technology Corp*

For many applications, commercially available V/F converters aren't adequate; you must build your own. Using new design techniques, you can extend converter performance and add a variety of special features. Three important parameters that you can manipulate to your advantage are dynamic range, speed, and stability.

You can use different approaches to build your ideal V/F converter, but what's ideal for one application might not be best for another. You make tradeoffs in design choices when you optimize for a particular capability (see **box,** "V/F-converter design: some basic choices"). Still, the tradeoffs don't prevent you from building circuits that outperform off-the-shelf V/F converters.

If improved speed and dynamic range are your goals, then consider **Fig 1a**'s circuit. It features a 1-Hz to 100-MHz frequency range and a 160-dB (8-decade) dynamic range. Its other specifications include a 0 to 10V input-voltage range, 0.06% linearity, a 25-ppm/°C gain temperature coefficient, and a 50-nV/°C offset-voltage shift.

The circuit includes a crude, but wide-range, voltage-controlled oscillator (VCO) and its feedback loop, which contains a divider chain, charge pump, servo amplifier, and current sink. Buffer IC_3 and ECL gate IC_5 form the VCO.

The VCO's output frequency, divided by 32, drives an LTC1043 switched-capacitor charge pump (IC_8). The divide-by-32 circuit consists of a divide-by-16 MC10136 (IC_6), a 2N5160 differential-pair level shifter (Q_3), and a CD4013 D flip-flop (IC_7), which is connected as a divide-by-2 circuit.

IC_8's output biases a chopper-stabilized LTC1052 servo amplifier (IC_1), closing the feedback loop around the VCO. The charge pump and the chopper-stabilized servo amplifier stabilize the VCO's operating point via current sink Q_1, which is a 2N3904.

A positive voltage input (between 0 and 10V) to the circuit causes IC_1's output to swing positive and switch Q_1 on. Q_1 pulls current (**Fig 1b,** trace A) from the MV209 varactor diode, which serves as an integrating capacitor for the VCO.

VCO circuit uses scope-type trigger

The VCO itself, a ramp generator, uses a trigger circuit similar to those used to trigger oscilloscopes. The trigger circuit contains IC_5 in parallel with a

A few design techniques help you build V/F converters that outperform off-the-shelf versions.

220Ω/4-pF RC combination (R_1C_1) and features voltage hysteresis and a 1-nsec response time. IC_3 pulls current from the varactor and biases this trigger circuit. When IC_3's output voltage descends to the trigger's lower trip point, the trigger's output reverses state.

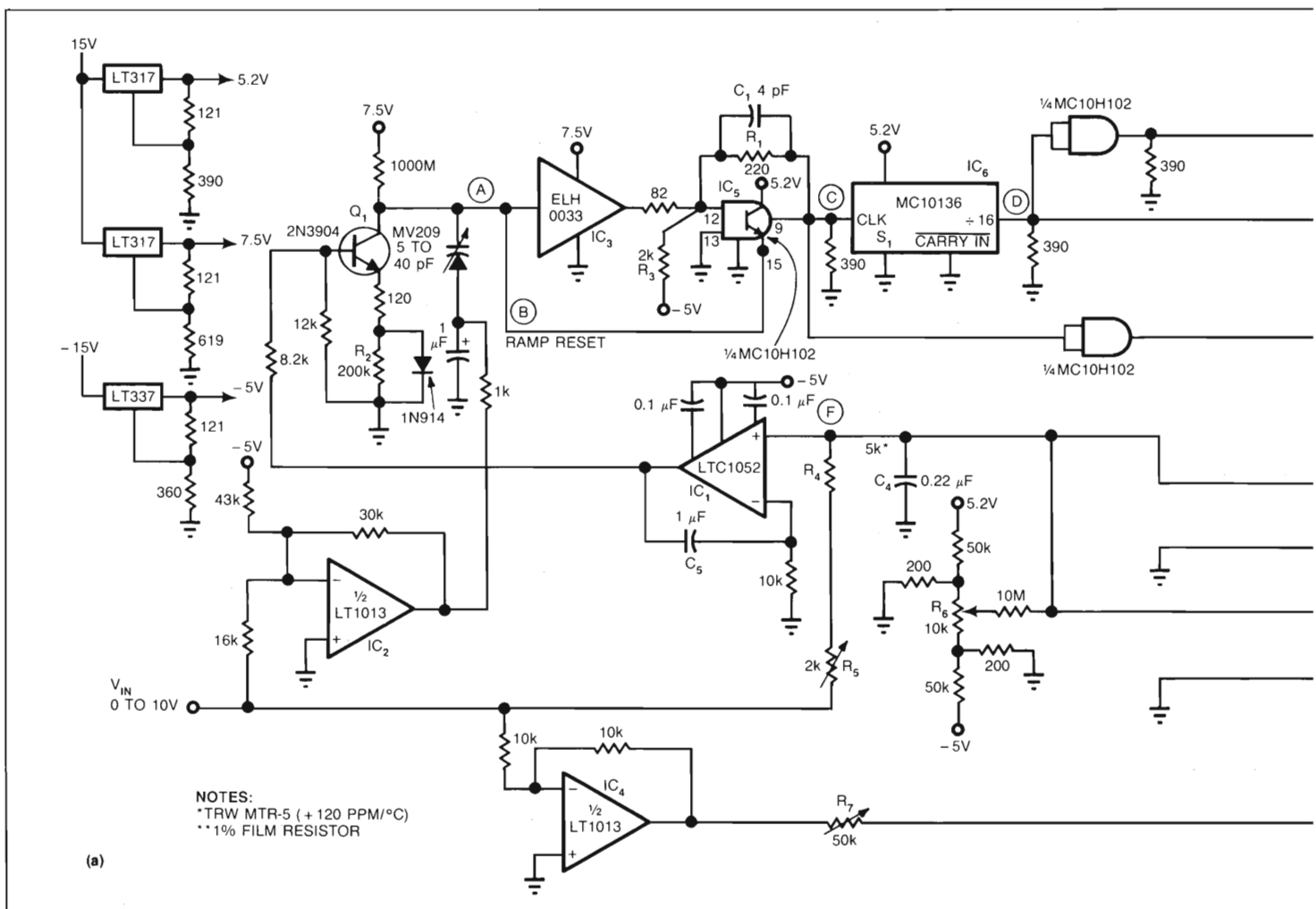
IC_5's inverting output (pin 15), acting as an unterminated emitter follower, deposits a short, positive-going current spike (trace B) into the varactor-diode integrator. IC_5's noninverting output (pin 9) supplies a positive-going pulse (trace C) to clock IC_6. IC_6's divided-down output (trace D), level-shifted by a differential pair of 2N5160s, clocks IC_7, which is connected in a divide-by-2 configuration. IC_7's Q output, a square wave, supplies the clock signal to IC_8.

The switched-capacitor pair in IC_8 (C_2 and C_3) runs 180° out of phase; the capacitors therefore alternately drive the servo amplifier's noninverting input (trace F) on each transition (positive or negative) of IC_8's clock input. The frequency of this input is the VCO's output frequency divided by 32 (about 3 MHz for this V/F converter's 100-MHz max operating frequency), and it's within the LT1043's operating range.

Accuracy depends on zener stability

The amount of charge delivered to the servo amplifier per cycle depends on the reference voltage supplied by the LT1009 zener diode and the values of C_2 and C_3 (Q=CV). In this case, the voltage and capacitor values are 2.5V and 100 pF, respectively. The charge pump's overall accuracy depends on the stability of both the

Fig 1—This V/F converter's 1-Hz to 100-MHz frequency range *results from the use of an exceptionally wide-range VCO with a charge pump and servo amplifier in its feedback loop.*



LT1009 and the 100-pF capacitors and also on its own low charge injection. A difference in the capacitors' values within their ranges of tolerance results in a slight difference in the charge delivered on the clock's rising and falling edges, but this difference doesn't influence circuit operation.

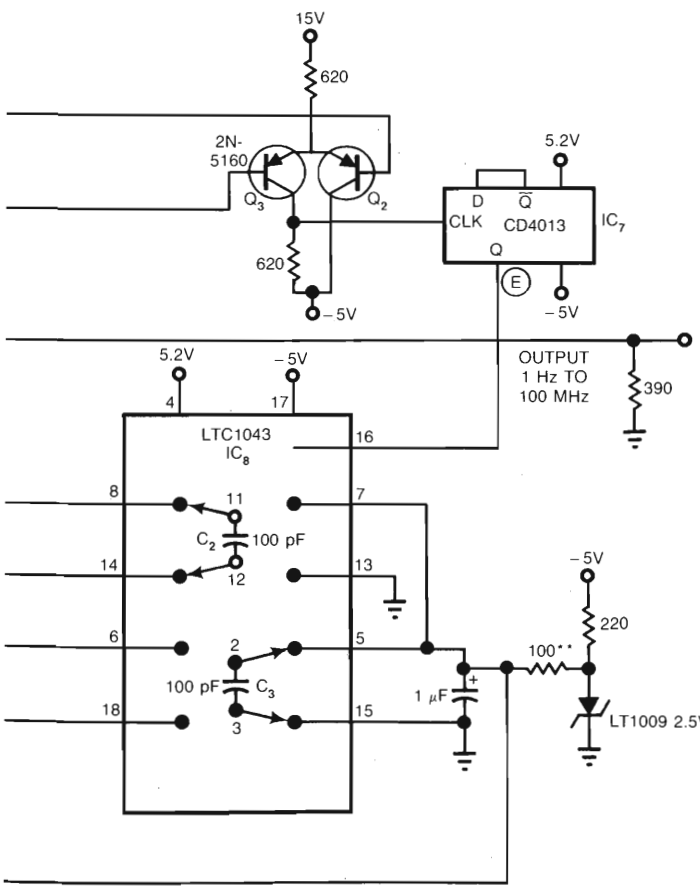
The 0.22-μF capacitor (C_4) on IC_8's output and IC_1's input integrates IC_8's output pulses to dc. IC_1 integrates the averaged difference between two currents: one current from the V/F converter's input, and the other current from IC_8's output. IC_1's output is thus a combination of the circuit's input voltage and its feedback signal. It drives current sink Q_1 and sets the VCO's (and, consequently, the V/F converter's) output frequency.

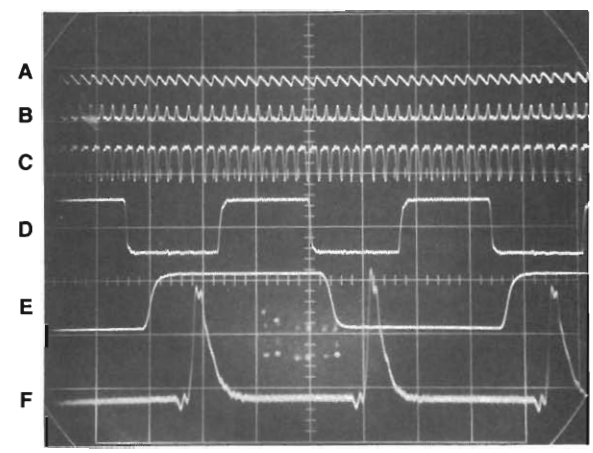
The input voltage also drives IC_2, a varactor-bias amplifier. This inverting amplifier provides a dc-bias voltage for the MV209 varactor diode. This dc-bias voltage causes the varactor diode's capacitance to vary inversely with the input voltage, helping the circuit achieve its 8-decade frequency range. The 1-μF capacitor connected between the varactor's anode and ground gives the relatively large ramp currents a low-impedance path to ground.

Circuit subtleties improve performance

A variety of circuit techniques allow the V/F converter to achieve its impressive specifications. The 1000-MΩ resistor between the 7.5V supply and Q_1 provides enough current to overcome the effects of any leakage current from Q_1's collector. This current source ensures that Q_1 always acts as a current sink and pulls current from the varactor-integrator to sustain VCO oscillation, even at the lowest frequencies of oscillation.

Text continues on pg 158





TRACE	VERT	HORIZ
A	1V/DIV (AC COUPLED)	100 NSEC/DIV
B	5 mA/DIV	100 NSEC/DIV
C	1V/DIV (AC COUPLED)	100 NSEC/DIV
D	1V/DIV (AC COUPLED)	100 NSEC/DIV
E	10V/DIV	100 NSEC/DIV
F	5 mA/DIV	100 NSEC/DIV

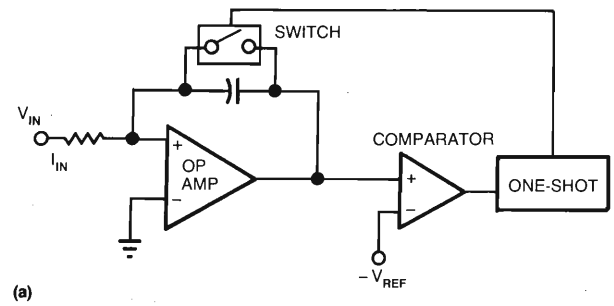
(b)

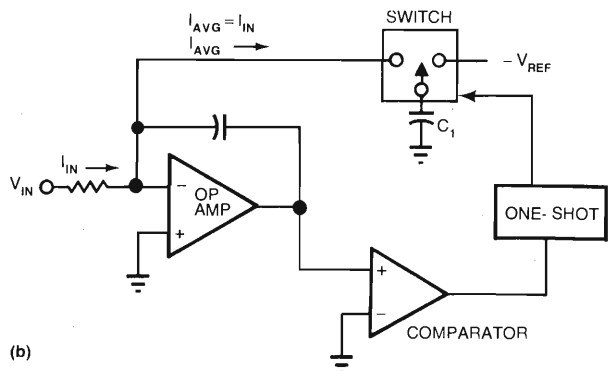
A 1-Hz to 100-MHz V/F converter uses a crude, but wide-range, voltage-controlled oscillator and its associated feedback loop.

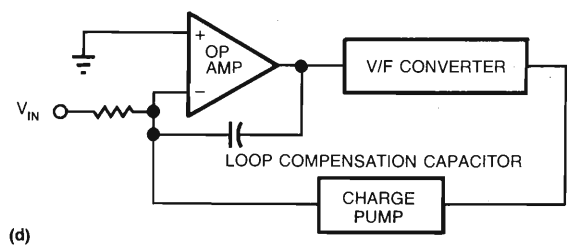
V/F-converter design: some basic choices

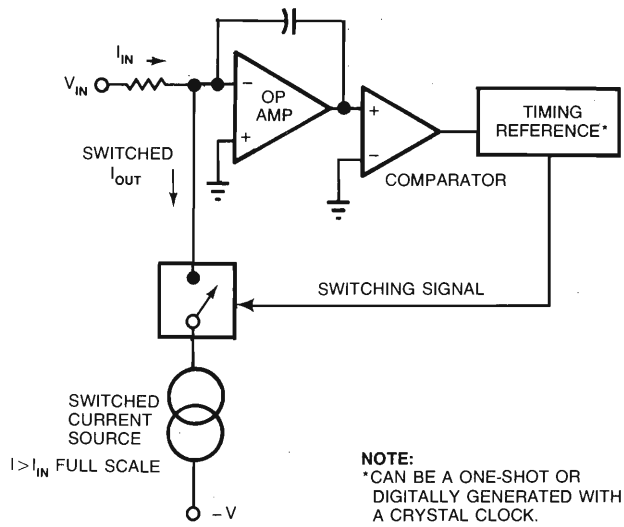
You can choose among many methods of converting a voltage to a frequency. The optimal approach for your application will vary with your requirements, which will place varying emphasis on precision, maximum output-frequency, response time, dynamic range, etc.

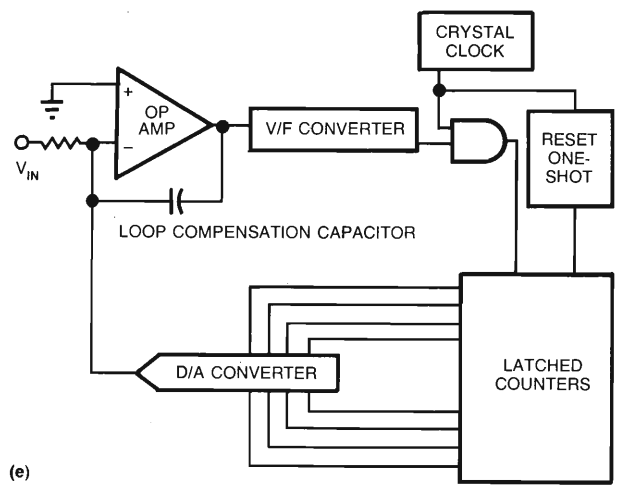
Part **a** of the **figure** shows a simple design. The input voltage (V_{IN}) drives an integrator. The slope of the ramp produced by the integrator varies with the input-derived current (I_{IN}). When the integrator's output crosses V_{REF}, the comparator closes the switch. The switch's closing causes the capacitor to discharge, the op amp's output to drop below V_{REF}, and the in-











You can choose from a variety of V/F-converter designs, *tailored to your specific needs. Part* ***b****'s circuit solves* ***a****'s integration-time problem by configuring the integrator in a charge-dispensing loop. Part* ***c****'s circuit uses feedback current instead of feedback charge to close the loop around the op amp. Circuits* ***d*** *and* ***e*** *achieve high linearity, high speed, and wide dynamic range.*

tegration to start over again. The frequency of this action is directly proportional to the input voltage. With careful design, one op amp can serve as both integrator and comparator.

A serious drawback of this approach is the capacitor's discharge-reset time. This time, "lost" in the integration, results in a serious error in linearity as the period of the operating frequency approaches it. For example, a 1-μsec reset interval produces a 0.1% error at 1 kHz, rising to 1% at 10 kHz. Variations in reset times also contribute linearity errors. Because of these two error sources, you have to restrict this type of circuit's operation to low frequencies in order to maintain good linearity and frequency stability.

Put integrator in loop

The circuit shown in **b** solves the problems introduced by integration-time errors by configuring the integrator in a charge-dispensing loop. In this circuit, capacitor C_1 charges to V_{REF} as the integrator's output voltage increases. When the comparator switches, the one-shot disconnects C_1 from V_{REF} and connects it to the op amp's inverting input. C_1 discharges into this node and sums with I_{IN}, forcing the op amp's output high.

Once C_1 has discharged, the op amp again begins to integrate, and the cycle repeats. Because the feedback loop forces the average value of the summing currents to zero, the integrator's time constant and its reset time don't affect the frequency of oscillation. This design approach results in circuits that maintain high linearity at high frequencies—typically within 0.01% at 1 to 10 MHz. Again, with careful design, you can make one op amp serve as both integrator and comparator.

The circuit shown in **c** is similar to that shown in **b,** except that it uses feedback current rather than feedback charge to close the loop around the op amp. Each time the op amp's output switches the comparator, the timing reference closes a switch and the current sink pulls current from the summing point at the op amp's inverting input.

Because the sink pulls current from the summing junction, the integrator's output swings positive. At the end of an interval determined by the timing reference, the switch opens, the current sink ceases pulling current from the summing junction, and the integrator's output again swings negative. The timing sequence causes the cycle to repeat and thereby sustain oscillation. The frequency of oscillation depends on I_{IN} and is therefore directly proportional to the V/F converter's input voltage.

DC loop correction

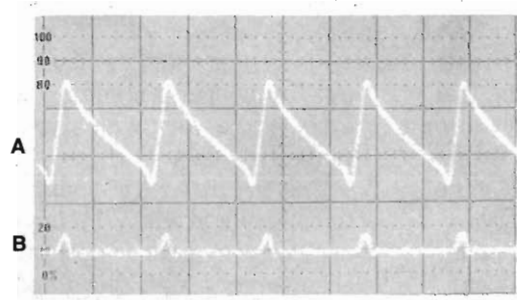
Circuit **d** uses dc loop correction. This type of feedback provides all the advantages of charge and current-balancing feedback except that its response time is slower. DC loop correction also offers exceptionally high linearity (0.001%), output frequencies exceeding 100 MHz, and a very wide dynamic range (160 dB).

The circuit uses a dc amplifier to control a crude V/F converter. The converter is designed to achieve very high speed and wide dynamic range at the expense of linearity and thermal stability. The converter's output switches a charge pump, whose output is compared to the converter's input voltage. The dc amplifier that performs the comparison changes the V/F converter's output frequency so that it's a direct function of the converter's input voltage (V_{IN}).

The dc amplifier's frequency compensation capacitor, which is required because of feedback-loop delays, limits the feedback loop's response time. The circuit shown in **e** replaces the charge pump with digital counters, a crystal-controlled time base, and a D/A converter.

Although it's not immediately obvious, the D/A converter's quantizing limitations don't determine the circuit's resolution: The dc-feedback loop forces the D/A converter's LSB to oscillate around its correct value. The loop-compensation capacitor damps these oscillations. Consequently, the circuit tracks input shifts that are much smaller than the D/A converter's LSB. For example, a 12-bit D/A converter (4096 steps) yields a resolution of one part in 50,000. The D/A converter's linearity specification, however, does determine the V/F converter's linearity.

Using a compensation capacitor with a 0.1-μF value improves circuit settling time, but it increases jitter below 1 kHz.



TRACE	VERT	HORIZ
A	200 mV/DIV (AC COUPLED)	10 NSEC/DIV
B	10 mA/DIV	10 NSEC/DIV

Fig 2—At 100 MHz, only 10 nsec are available *for a complete ramp-and-reset sequence in* ***Fig 1****'s V/F converter. Trace A shows the ramp, and trace B shows the reset current from the ECL-gate's open emitter.*

The parallel combination of the 200-kΩ resistor (R_2) and the 1N914 diode reduces the low frequency jitter caused by current-sink noise in Q_1 at low frequencies. It does so by increasing emitter resistance at low base bias voltages to reduce current-sink noise at low frequencies. The larger voltages encountered at higher operating frequencies force the diode to turn on, and Q_1 emitter current bypasses R_2. The use of a 2-kΩ pull-down resistor (R_3) at the input (pin 12) of the ECL-gate trigger IC ensures clean, quick transitions at low-frequency ramp slew rates, and it decreases low-frequency jitter.

The 5-kΩ resistor (R_4) between the converter's input and IC_1 has a +120-ppm temperature coefficient; this temperature coefficient counteracts the effects of the negative temperature coefficients of the 100-pF polystyrene capacitors in IC_8, thus lowering drift in the V/F converter.

A unity-gain, inverting amplifier (IC_4) supplies a small current—proportional to the V/F converter's input voltage—to the charge pump's voltage-reference input. This current cancels nonlinear terms caused by residual charge imbalance in the LTC1043. This method of correction is effective because both the correction current and the effects of the charge imbalance in the LT1043 are proportional to the operating frequency.

The V/F converter's 100-MHz range sets stringent speed requirements on the oscillator's cycle time: At 100 MHz, only 10 nsec are available for a complete ramp-and-reset sequence in the VCO. This time requirement for resetting the varactor/integrator places the overall limitation on the circuit's maximum operating frequency. The combination of a small-amplitude ramp and the ECL gate's short switching time provides the necessary high-speed operation. Trace A in **Fig 2** shows the ramp, and trace B shows the reset current from the ECL gate's open emitter. Note that the reset occurs in 3.5 nsec, with little overshoot.

Jitter: causes and cures

Fig 3 plots output frequency vs jitter. Jitter is 0.01% at 100 MHz and falls to 0.002% at 1 MHz. In this frequency range, noise in the current source and ECL trigger dominates jitter. Below 1 MHz, the jitter slowly rises as the V/F converter's operating frequency approaches the servo amplifier's low-frequency limit.

At 1 kHz, jitter is still below 1%. At 1 Hz, jitter exceeds 10% for a value (C_{COMP}) of 1 μF for the servo amplifier's compensation capacitor (C_5). If C_5 had a value of 0.1 μF, jitter would be even greater below 1 kHz (10% at 100 Hz, for example), and the converter would not be able to operate at frequencies of less than 10 Hz because of loop instability and IC_1's noise floor. There is, however, a tradeoff between jitter and the V/F converter's frequency range: loop settling time. Using the 0.1-μF compensation capacitor, the feedback loop settles in 60 msec. Using the preferred 1-μF

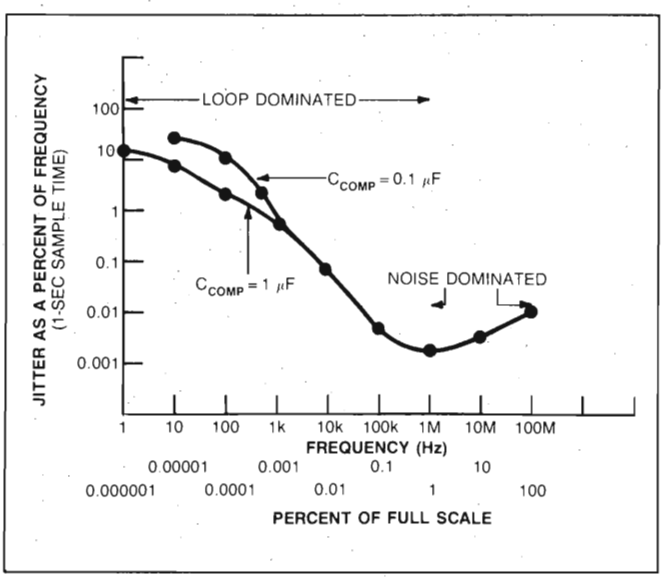
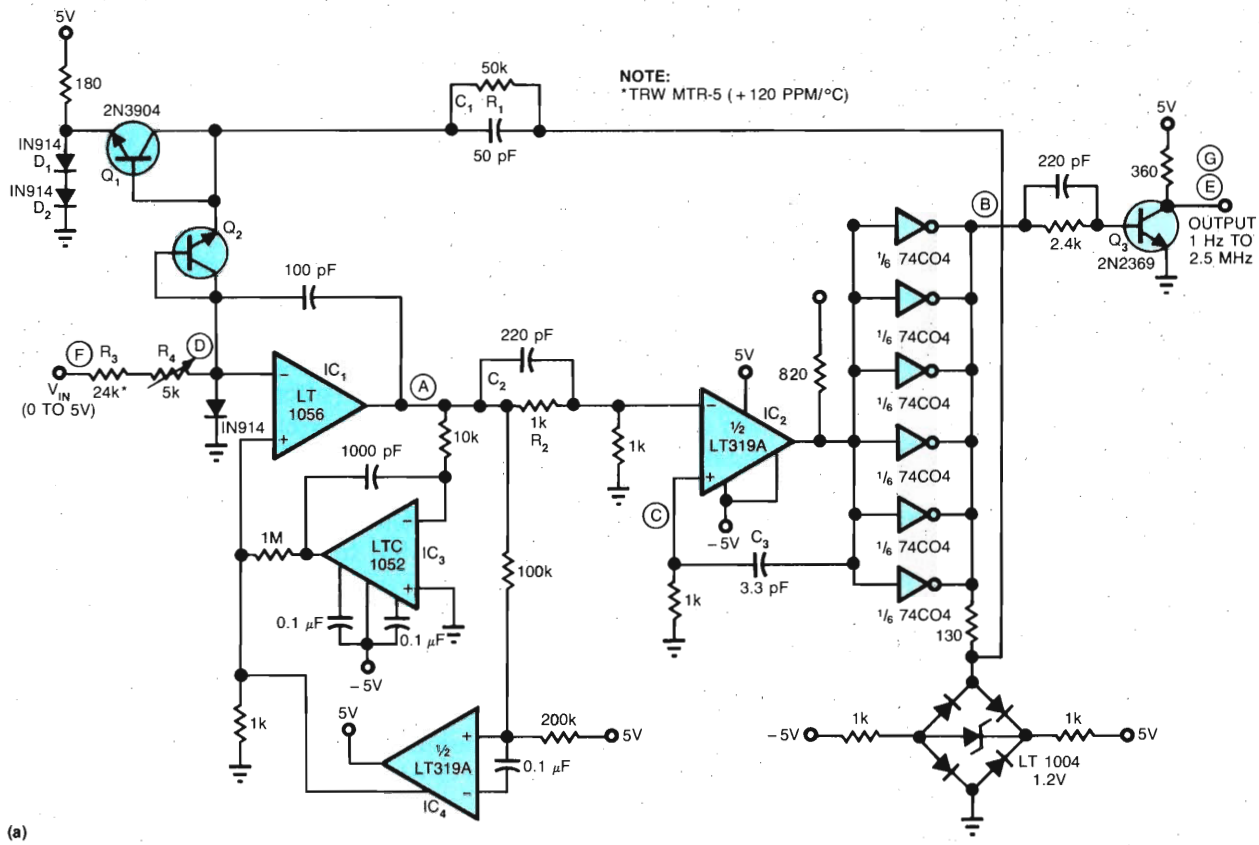
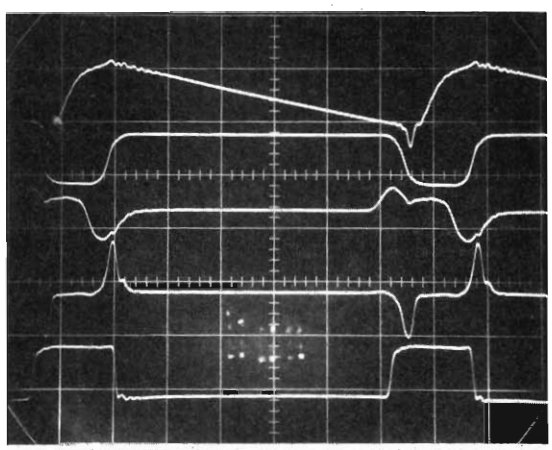


Fig 3—A V/F converter's jitter varies with output frequency. *The jitter decreases as output frequency increases and is a function of the value of the compensation capacitor in the servo amplifier.*

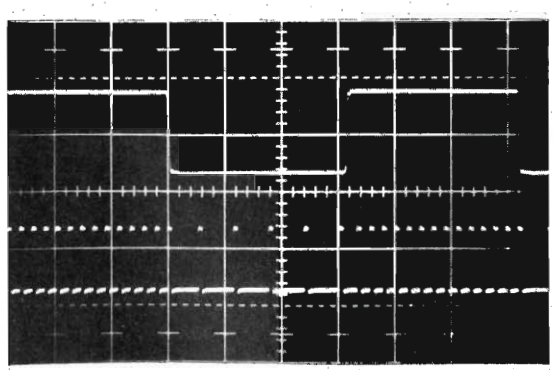


(a)



(b)

TRACE	VERT	HORIZ
A	500 mV/DIV	100 NSEC/DIV
B	10V/DIV	100 NSEC/DIV
C	500 mV/DIV	100 NSEC/DIV
D	10 mA/DIV	100 NSEC/DIV
E	5V/DIV	100 NSEC/DIV



(c)

TRACE	VERT	HORIZ
F	5V/DIV	2 μSEC/DIV
G	5V/DIV	2 μSEC/DIV

Fig 4—This V/F converter uses feedback *directly from a charge pump to achieve its 3-μsec settling time and 2.5-MHz max output frequency. These specifications make the converter a good candidate for applications that require a rapid response to a change in input signal.*

Some applications require a rapid response to a change in input signal. You can build a V/F converter that specs a 3-μsec settling time.

compensation capacitor, the feedback loop settles in 600 msec.

To calibrate this V/F converter, you have to set its output frequencies to 1 Hz, 50 MHz, and 100 MHz for 0, 5, and 10V inputs, respectively. First apply 10V to its input and adjust the 100-MHz trim resistor (R_5) for 100 MHz at the circuit's output. If you don't have a frequency counter capable of 100-MHz resolution, then use the $f_0 \div 32$ signal available at pin 16 of the LTC1043 charge pump. For a 100-MHz output frequency, this signal should be 3.125 MHz.

Next, remove the 10V input to the converter and ground the converter's input. Install C_5 between IC_1's inverting input and its output. Adjust the 1-Hz trim potentiometer (R_6) so that the converter oscillates at 1 Hz. Finally, apply a 5V input to the converter and adjust the linearity trim potentiometer (R_7) for a 50-MHz converter output. Repeat these three adjustments until you achieve the desired output-frequency settings.

Converter settles quickly

Although **Fig 4a**'s circuit doesn't have anywhere near the frequency range of **Fig 1a**'s circuit, its 2.5-MHz full-scale output settles from a full-scale step input in only 3 μsec. This quick response time makes the circuit a good candidate for applications—such as frequency modulation—that require a rapid response to a change in input signal. The circuit also features 0.05% linearity with a 50-ppm/°C gain temperature coefficient. A chopper-stabilized correction network, built around IC_3, holds zero-point frequency drift to 0.025 Hz/°C.

Like **Fig 1a**'s circuit, **Fig 4a**'s circuit uses charge feedback. This converter, a high-speed charge-dispensing type, does not use a servo (integrating) amplifier, but instead supplies charge feedback directly, so the converter responds quickly to input steps. Although this approach realizes a fast-response circuit, it does have a drawback: You must minimize circuit parasitics to achieve high voltage-vs-frequency linearity and prevent output-frequency drift.

V/F reference includes diode bridge

Integrator IC_1, comparator IC_2, the 74C04 inverters, and the LT1004 diode bridge form the V/F converter. The feedback path is from the diode bridge to IC_1's inverting input through a 50-kΩ/50-pF RC combination (R_1C_1). (C_1 is a polystyrene capacitor with a −120-ppm/° temperature coefficient.)

When you apply a 0 to 5V input to this V/F converter, IC_1's output goes low (**Fig 4b,** trace A). When IC_1's output crosses zero, IC_2's output switches from negative to positive, thereby causing the paralleled inverters' outputs to go low (trace B). The parallel combination of a 220-pF capacitor and a 1-kΩ resistor (R_2C_2) in series with IC_2's inverting input provides a lead to extend the converter's high-frequency response.

The low output of the inverters causes the LT1004-based diode bridge to reach its limit of −2.4V dc. Positive feedback (trace C) through a 3.3-pF capacitor (C_3) to IC_2's noninverting input reinforces the IC_2 output's positive swing. While IC_2's output is going high and the inverters' outputs are going low, the negative voltage at the diode bridge pulls charge through the R_1C_1 from the summing junction at IC_1's inverting input (trace D).

Input determines oscillation frequency

This loss of charge at IC_1's input causes its output to swing positive and the IC_2/inverter combination to switch the inverters' output high and pull the diode bridge's output to its positive bound at +2.4V. When the charge removal decays, IC_1's output again swings negative, and the cycle repeats. The frequency of this oscillation is a linear function of the V/F converter's input voltage.

Diodes D_1 and D_2 compensate for the voltage drops of the diodes in the bridge. Q_1 compensates for Q_2. These diode-connected transistors feature lower leakage currents than conventional diodes. Q_2 thus provides low leakage current from IC_1's summing (inverting) junction. Chopper-stabilized op amp IC_3 provides offset trimming for IC_1, eliminating the need to zero-trim the amp.

Op amp IC_4, connected as an emitter follower, prevents the oscillator from latching up, an outcome made possible by the inclusion of the ac-coupled feedback loop. If the circuit does latch up, then IC_1's output swings to the negative rail and stays there. This action causes IC_4's output to go high, which in turn forces IC_1's output high and restarts oscillation. The diode connected to ground at IC_1's inverting input ensures that the start-up loop can override any input condition by limiting the maximum voltage at this terminal.

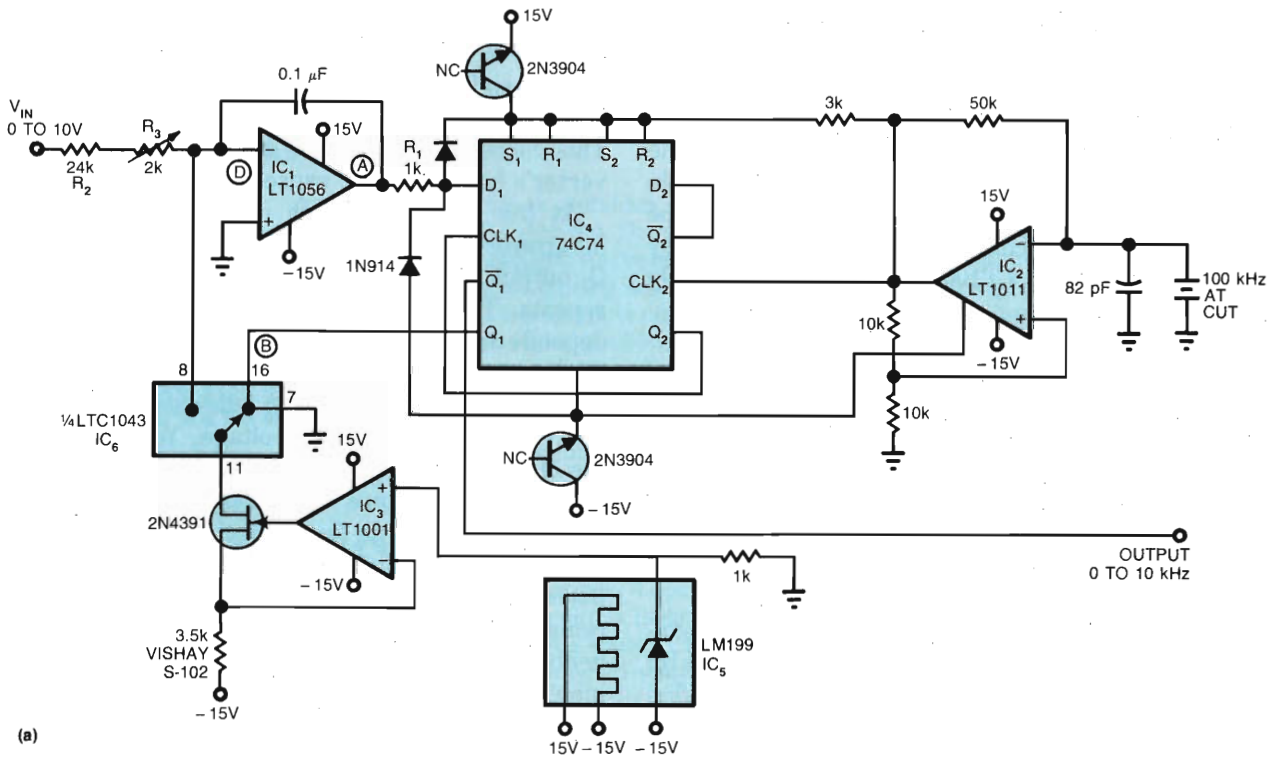
RC combination improves linearity

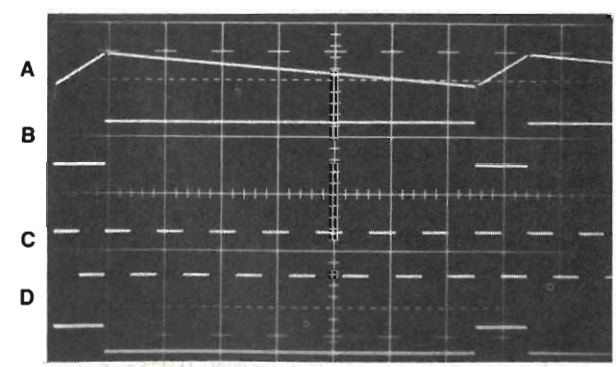
The R_1C_1 combination improves the circuit's V/F-conversion linearity by permitting complete capacitor discharge on each oscillator cycle. The 24-kΩ resistor (R_3) at the V/F converter's input has a +120-ppm/°C

temperature coefficient; this temperature coefficient compensates for C_2's −120-ppm/°C coefficient.

Fig 4c's scope photo shows the circuit's response to a step in input voltage. Trace F shows the circuit's input voltage, and trace G shows the response in the circuit's output waveform. The frequency shift is quick and clean, with no evidence of poor transient response or delayed response caused by time constants.

To calibrate this V/F converter, simply apply 5V to the converter's input and adjust the 2.5-MHz trim potentiometer (R_4) for 2.5 MHz at the converter's TTL-compatible output (**Fig 4b,** trace E). Because IC_3, which compensates for IC_1's offset voltage, itself has a low-offset voltage output, the converter doesn't need a zero-trim adjustment. Once calibrated, the V/F converter maintains 0.05% linearity with 50-ppm/°C drift





TRACE	VERT	HORIZ
A	0.5V/DIV (AC COUPLED)	20 μSEC/DIV
B	20V/DIV	20 μSEC/DIV
C	20V/DIV	20 μSEC/DIV
D	5 mA/DIV	20 μSEC/DIV

Fig 5—This V/F converter achieves high stability *by using a quartz crystal instead of a capacitor as the reference element in its charge pump.*

The fast-settling converter has a quick, clean frequency shift. There's no evidence of poor transient response or delayed response caused by time constants.

across the 1-Hz to 2.5-MHz range.

In the previous two V/F-converter circuits, the +120-ppm/°C drift in the charge-pump capacitors (C_2 and C_3 in **Fig 1a**'s circuit and C_1 in **Fig 4a**'s circuit) affect the gain temperature coefficient. Although compensation schemes (the use of resistors with −120-ppm/°C temperature coefficients) minimize the effects of this drift, you need to use another approach to achieve significantly lower gain drift.

The circuit shown in **Fig 5a** has a gain temperature coefficient of 5 ppm/°C. It achieves this high degree of stability by using a quartz crystal instead of a capacitor as the reference element in its charge-pump circuit.

In the charge-pump circuits of **Figs 1a** and **4a,** the amount of charge used as feedback is based on the relationship Q=CV, where Q is the amount of charge in coulombs, C is the capacitance in farads, and V is the voltage across the capacitor. This voltage is supplied by reference circuits (the LT1009, etc) in the previously discussed circuits.

Reference checks capacitance drift

The crystal-based reference governs the amount of charge used as feedback according to a different relationship: Q=IT, where I is the current in amperes from a stable current source and T is the interval of time in seconds derived from the crystal-based clock. This relationship eliminates the change in the amount of charge caused by the drift in the C value.

In this circuit, the crystal-based reference is a relaxation oscillator (IC_2). The oscillator supplies a 100-kHz signal to the CLK_2 input of a 74C74 dual D flip-flop (IC_4). This section of the flip-flop, connected as a divide-by-2 circuit, provides a 50-kHz reference for the flip-flop's CLK_1 input. This 50-kHz reference provides a clock for a circuit that gates a precision current sink and thus controls this V/F converter's charge feedback. The precision current sink comprises IC_3, an LM199 voltage reference (IC_5), a 2N4391 FET, and half an LTC1043 switch (IC_6).

Reverse-biased 2N3904 transistors serve as zener diodes and provide approximately 15V across the CMOS flip-flop. The 1N914 diodes across the flip-flop's D_1 input prevent damage to the flip-flop that may be caused by transients from IC_1 during the converter's power-on transition.

Fig 5b's photo shows selected waveforms from the circuit. A positive input voltage causes integrator IC_1's output to swing negative (trace A). This output drives IC_4's D_1 input through a 1-kΩ resistor. IC_4's Q_1 output (trace B) changes state at the first low-to-high clock transition that occurs after the input to D_1 has crossed D_1's switching threshold.

Flip-flop controls current-sink output

IC_4's Q_1 output controls the output gating of the precision current sink. When integrator IC_1's output swings negative, IC_4's Q_1 output is high, causing IC_6 to switch the current sink's output to ground via the switch's pins 7 and 11.

The change in Q_1's output causes IC_6 to close the connection between its pins 8 and 11. The precision current sink draws a current with a fast rise time from the summing junction at IC_1's inverting input (trace D). This current, scaled to be greater than the V/F converter's input current, causes IC_1's output to go high.

At the first low-to-high clock transition after the integrator's output has become a high input to D_1, IC_4's Q_1 output again changes state and the entire process repeats. The frequency at which this process repeats depends on the current supplied from the V/F converter's input voltage to the IC_1's summing junction. The frequency of oscillation is therefore a direct function of the V/F converter's input voltage. You can use either the Q_1 or $\overline{Q_1}$ outputs of IC_4 as the converter's output.

As noted, the use of the crystal-based reference circuit for the charge-feedback circuit reduces converter drift to about 5 ppm/°C. The contribution to drift made by the reference circuit is about 0.5 ppm/°C. The remaining drift is a function of the current-sink components, the LT1043's switching-time variations, and the input resistors. These resistors are a 24-kΩ fixed Vishay S-102 (R_2) and a 2-kΩ, 10-kHz trim potentiometer (R_3).

Crystal restricts frequency range

A V/F converter using a crystal-based reference is usually restricted to a relatively low full-scale output frequency range, such as 10 to 100 kHz. This restriction is the result of a speed limitation on the LT1043's ability to switch the current sink accurately. In addition, short-term jitter may occur because of the uncertain timing relationship between the point at which IC_1's output changes state and the arrival of the clock's next low-to-high transition. This timing relation is normally not a problem, because the converter's output is usually read over many clock cycles (eg, 0.1 to 1 sec) and the jitter averages out.

Other features of **Fig 5a**'s circuit are 0.005% linearity, a 5-ppm/°C gain temperature coefficient, and a

10-kHz full-scale output frequency. The zero-point error is 0.005 Hz/°C because of the LT1056's low input offset. To calibrate this circuit, apply a 10V input and adjust R_3 for 10 kHz as measured at the flip-flop's Q_1 or $\overline{Q_1}$ outputs.

The next article in this series will discuss design techniques for improving converter linearity and for adding such capabilities as low voltage operation, sine-wave output, and nonlinear transfer functions. **EDN**

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Author's biography

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and -instrumentation design. He has served in related capacities at National Semiconductor Corp, Arthur D Little Inc, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. Jim is a former student of psychology at Wayne State University, and he enjoys tennis, art, and collecting scientific instruments.

Refine V/F-converter operation with novel design techniques

Although commercially available V/F converters can adequately satisfy a number of design needs, in many cases you can realize a better applications match by designing your own converter. This second article of a 2-part series adds to your list of design hints a variety of techniques that allow you to improve converter linearity and develop the ideal V/F converter for other modes of operation.

Jim Williams, *Linear Technology Corp*

Because commercially available devices must be universal in nature, they don't always offer the best solution in specific applications. Such is the case with off-the-shelf V/F converters. The first article in this series (EDN, May 16, 1985, pg 153) showed that by designing your own circuits, it's possible to develop converters that offer the ideal solution for specific application needs. The design examples there covered such performance factors as speed, dynamic range, settling time, and stability.

This article will begin by describing design techniques for improving converter linearity. Subsequent discussion will highlight converter circuits that feature low-voltage operation, sine-wave output, and deliberately nonlinear transfer functions.

The V/F converter circuit shown in **Fig 1a** is optimized for very high linearity. Although it can operate in a stand-alone mode, it's primarily intended for processor-driven applications (such as weighing scales) that require 17-bit accuracy. This circuit has a 1-ppm resolution, and its linearity is better than 7 ppm (0.0007%). A processor-driven gain/zero calibration loop gives the circuit negligible zero and gain drift. To further ease the interface with a processor-based system, the circuit functions from a single 5V power supply.

This design is conceptually similar to the 100-MHz converter circuit discussed in part 1. IC_1, half an LTC1013, servo-controls a crude V/F converter composed of Q_1 (a current source in this case) and a set of 74C04 gates. The V/F output is divided digitally and drives an LTC1043 charge pump (IC_3) whose output closes a loop back to IC_1. This division process allows the LTC1043 to achieve much higher precision than would be possible with direct feedback.

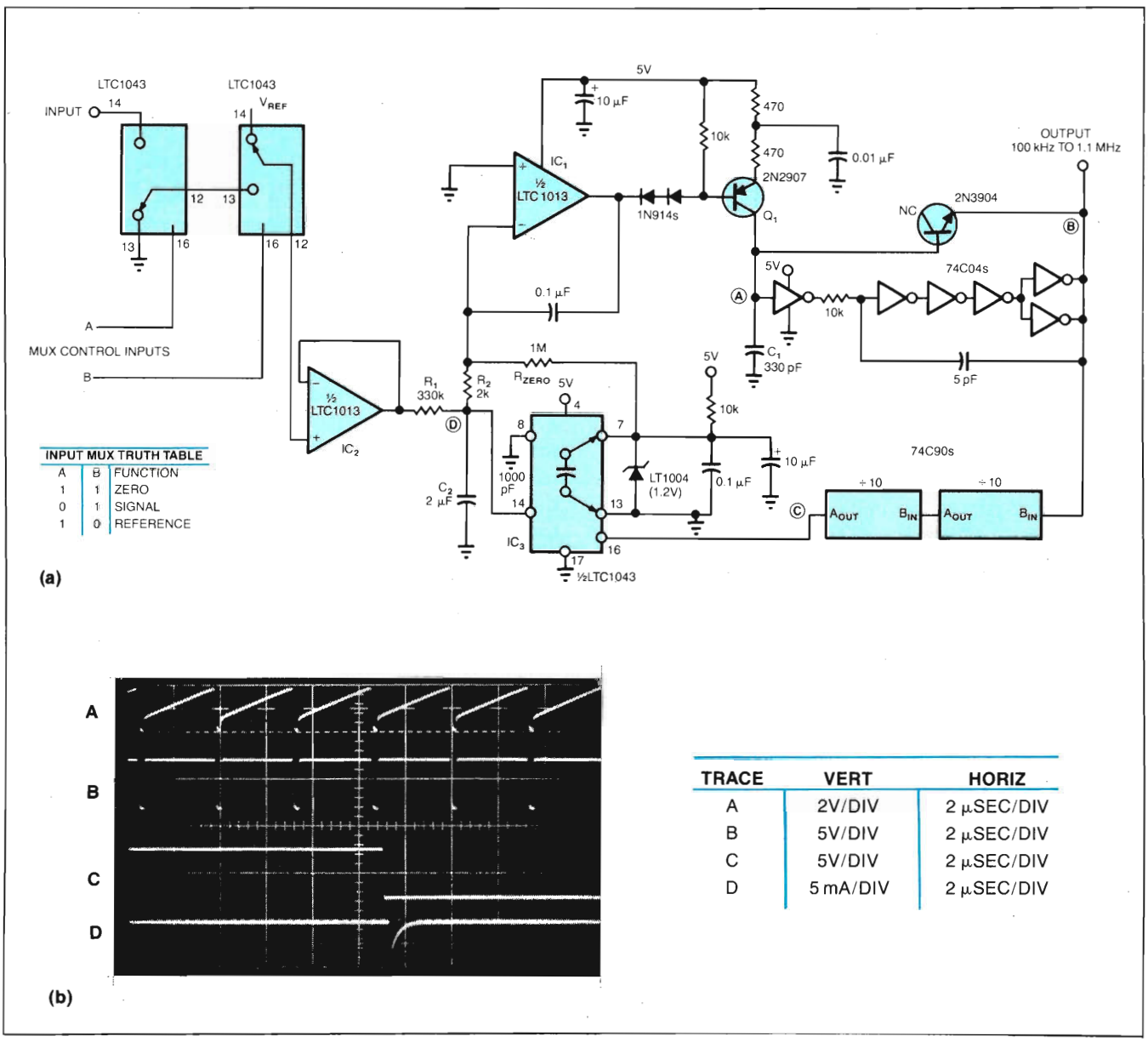
Before you try to master processor-driven operation, you should become familiar with the basics. To begin, assume that IC_2 and R_{ZERO} are absent, and that a positive voltage is present at the left end of R_1. This input forces IC_1's output to move in the negative direction, turning on Q_1 and thereby developing a positive-going ramp voltage across C_1 (trace A in **Fig 1b**). When C_1's ramp crosses the 74C04 inverters' threshold, its output moves toward ground, causing the

Although off-the-shelf components strive to provide a universal solution, they're not necessarily best for all applications.

entire inverter chain to switch. Positive ac feedback from the two paralleled inverter outputs enhances switching.

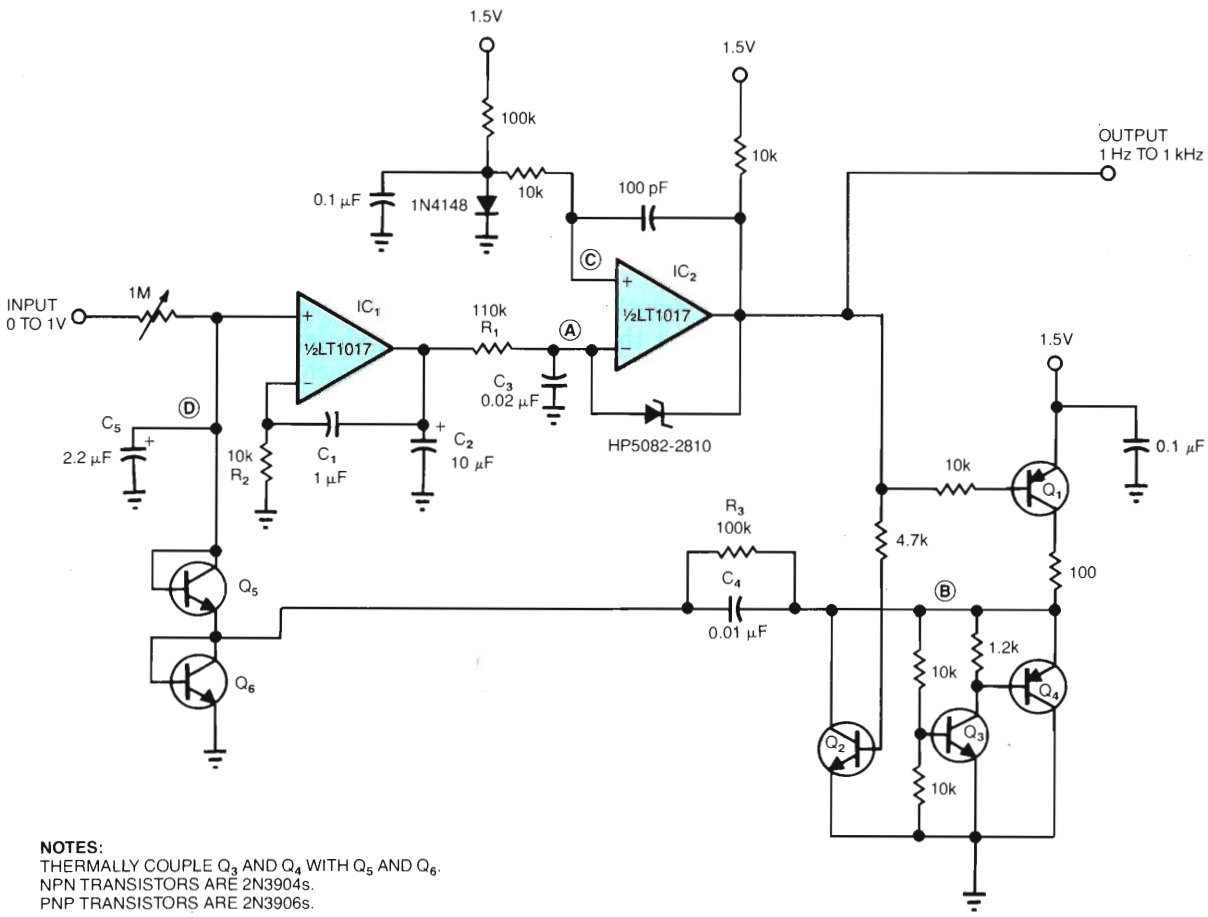
The output inverter's signal (trace B) also drives the ÷100 counter chain, which contains two ÷10 74C90s. The counter's output (trace C) clocks IC_3, which is configured to pump negative charge (trace D) into the $R_1R_2C_2$ junction. C_2 integrates the discrete charge events to dc, closing a loop around IC_1. As a consequence, IC_1 biases Q_1 at whatever point is necessary to balance its input. This action renders the crude V/F converter's output as a direct function of the input voltage over a 0- to 1-MHz range. The relatively low LTC1043 clock frequency is what provides the 0.0007% linearity.

The input multiplexer and R_{ZERO} are necessary for



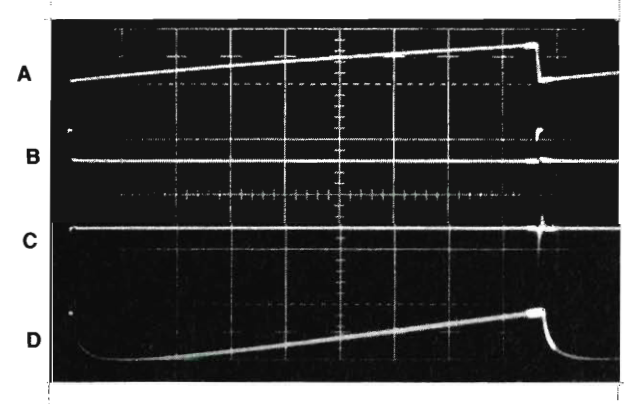
TRACE	VERT	HORIZ
A	2V/DIV	2 µSEC/DIV
B	5V/DIV	2 µSEC/DIV
C	5V/DIV	2 µSEC/DIV
D	5 mA/DIV	2 µSEC/DIV

Fig 1—This converter (a) furnishes 17-bit accuracy *and is well suited to processor-driven applications. It features a 1-ppm resolution and a linearity of better than 7 ppm. The waveforms* ***(b)*** *show that circuit output is a direct function of the input voltage over a 0- to 1-MHz range.*



NOTES:
THERMALLY COUPLE Q_3 AND Q_4 WITH Q_5 AND Q_6.
NPN TRANSISTORS ARE 2N3904s.
PNP TRANSISTORS ARE 2N3906s.

(a)



TRACE	VERT	HORIZ
A	100 mV/DIV	100 μSEC/DIV
B	2V/DIV	100 μSEC/DIV
C	1V/DIV	100 μSEC/DIV
D	10 mV/DIV	100 μSEC/DIV

(b)

Fig 2—Drawing only 125 μA from a 1.5V cell, *this circuit* ***(a)*** *uses an LT1017 dual micropower comparator operating in a servo-controlled charge-pump configuration. As the curves in* ***b*** *show, oscillator frequency is linear.*

Applications involving high speed or precision are not the only areas in which enhanced V/F converters prove useful.

processor-driven autozero/gain loop operation. When the multiplexer is set for the zero function (see **Fig 1a**'s truth table), IC_2's input is grounded, so there's no drive for R_1. IC_1 receives bias via R_{ZERO}, however, and the circuit oscillates at approximately 100 kHz. Once the processor reads this frequency, it shifts the multiplexer to the signal function, and IC_2's output becomes a buffered version of the signal input. This input and the current through R_{ZERO} now determine the circuit's output frequency. Typical outputs range from 0.1 to 1 MHz.

After detecting a frequency, the processor selects the multiplexer's reference state and determines the frequency's value. The reference voltage must be greater than the highest input-signal voltage level. The reference can be a stable potential, or one ratiometrically related to the signal input, which is the case in many transducer-based systems. Once this measurement sequence is complete, the processor has enough information to determine mathematically the value of the input signal.

Because the multiplexing sequence is relatively fast, it cancels V/F-converter drifts. This circuit requires no precision components, although the 1000-pF, polystyrene capacitor in the LTC1043 is a must for high linearity.

Satisfy portable-equipment needs

Applications involving high speed or precision (or both) are not the only areas in which enhanced V/F converters prove useful. **Fig 2a** shows a circuit that runs from a single 1.5V cell and features a current drain of only 125 μA. Such a converter would serve well in portable equipment. The design uses an LT1017 dual micropower comparator operating in a servo-controlled charge-pump configuration.

The 10- and 1-μF compensating capacitors (C_1 and C_2) around input comparator IC_1 allow it to function as an op amp. IC_1's output drives the R_1C_3 network, developing a ramp voltage across C_3 (trace A in **Fig 2b**). This ramp voltage serves as the input for IC_2. During the ramp period, IC_2's output is high, which biases Q_1 off and Q_2 on. The potential across the Q_3Q_4 V_{BE} multiplier reference (trace B) is zero, so capacitor C_2 receives no charge.

When the ramp potential equals the potential at IC_2's noninverting input, IC_2's output goes low and C_3 discharges. Positive ac feedback (trace C) maintains IC_2's state long enough to develop a ramp reset of about 80 mV. Concurrently, Q_1 comes on and Q_2 goes off. The Q_3Q_4 reference switches on and charges C_4 via the grounded Schottky diode (D_2).

After the ac feedback around IC_2 decays, IC_2's output returns high, cutting off Q_1 and turning on Q_2. C_4 then discharges, forcing current to flow from IC_1's summing-point capacitor (C_5) via Q_5 (trace D). In this manner, IC_1 servo-controls the oscillator to whatever frequency is necessary to maintain the oscillator's summing point near zero. Because the current into IC_1's input is a linear function of the input voltage, the oscillator frequency is also linear. The 10-kΩ/1-μF R_2C_1 combination at IC_1 provides loop stability. The 100-kΩ resistor (R_3) in parallel with C_4 influences the circuit's discharge characteristics in such a way that it improves overall circuit linearity.

The junction temperature coefficients of Q_5 and Q_6 compensate for the temperature coefficient of the 1.2V Q_3Q_4 reference, giving the overall circuit a 250-ppm/°C gain drift. Battery discharge introduces less than 1% error over a 1000-hr operating span.

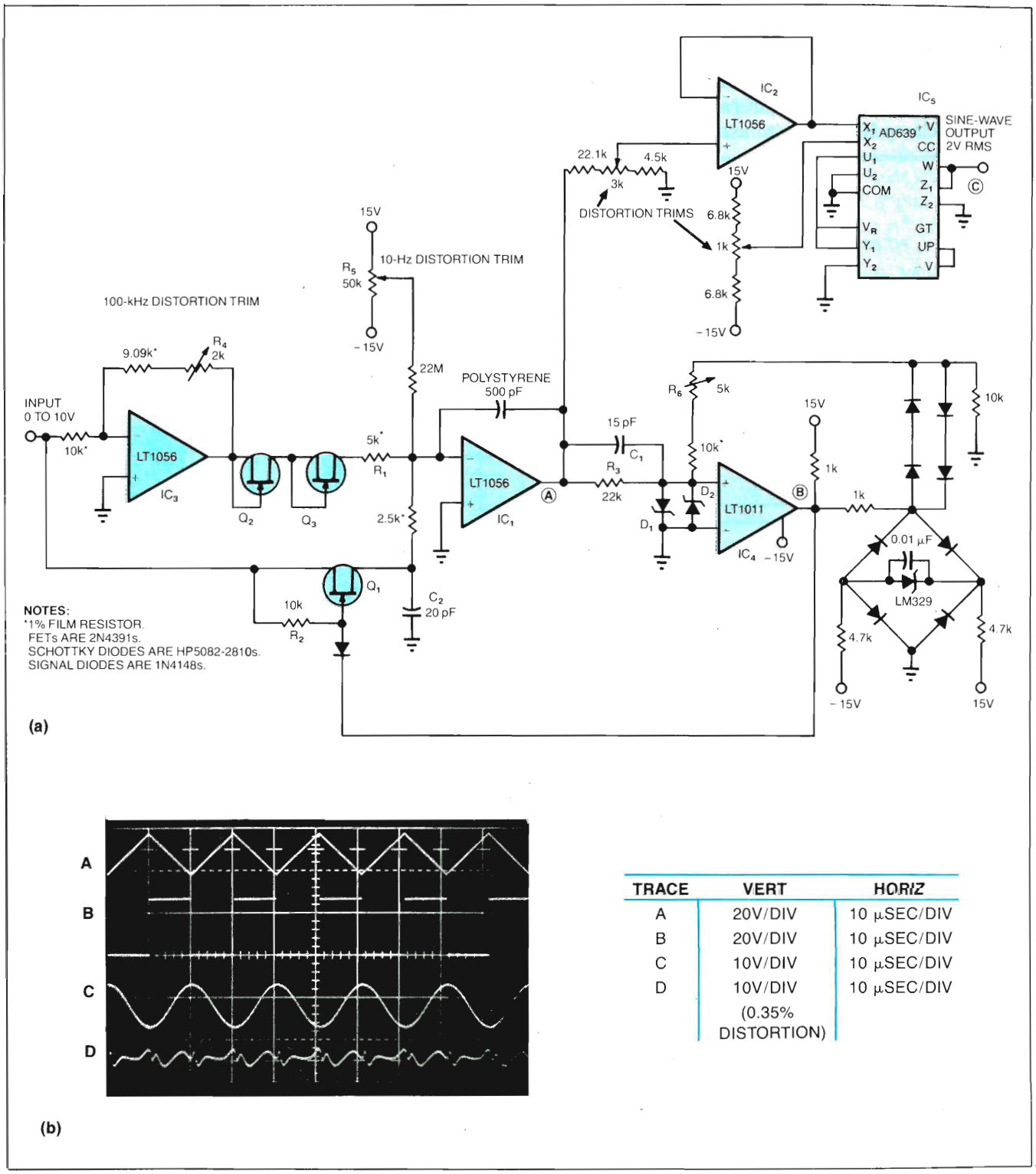
Sine-wave outputs come in handy

Almost all V/F converters have a pulse or square-wave output. In many applications, however (audio, filter testing, ATE), a sine-wave output would be more appropriate. Spanning a 1-Hz to 100-kHz range (100 dB or five decades) for a 0 to 10V input, the circuit shown in **Fig 3a** satisfies this need. It maintains a 0.1% frequency linearity and specs 0.2% distortion. Its settling time is 1.7 μsec.

To understand circuit operation, begin by assuming that IC_4's output is low, which means that Q_1 is off. IC_3 inverts the positive input voltage and biases integrator IC_1's summing node through R_1 and self-biasing FETs Q_2 and Q_3. This action pulls current (−I) from the node. IC_1's output (trace A, **Fig 3b**) ramps in a positive direction until IC_4's input crosses 0V. At this time IC_4's output goes positive (trace B), allowing Q_1 to turn on.

R_2 (from Q_1's gate to drain) is scaled to produce a current (+2I) that's exactly twice the absolute magnitude of the current being drawn from IC_1's summing node. As a result, the net current into IC_1's summing junction equals +I, and the output ramps negatively at a rate equal to that of the positive ramp. IC_1's output ramps in the negative direction until IC_4's noninverting input goes negative, at which time its output switches. This switching of the output turns Q_1 off, and the entire cycle repeats.

This operating sequence develops a triangular waveform at IC_1's output. The frequency of this wave is a



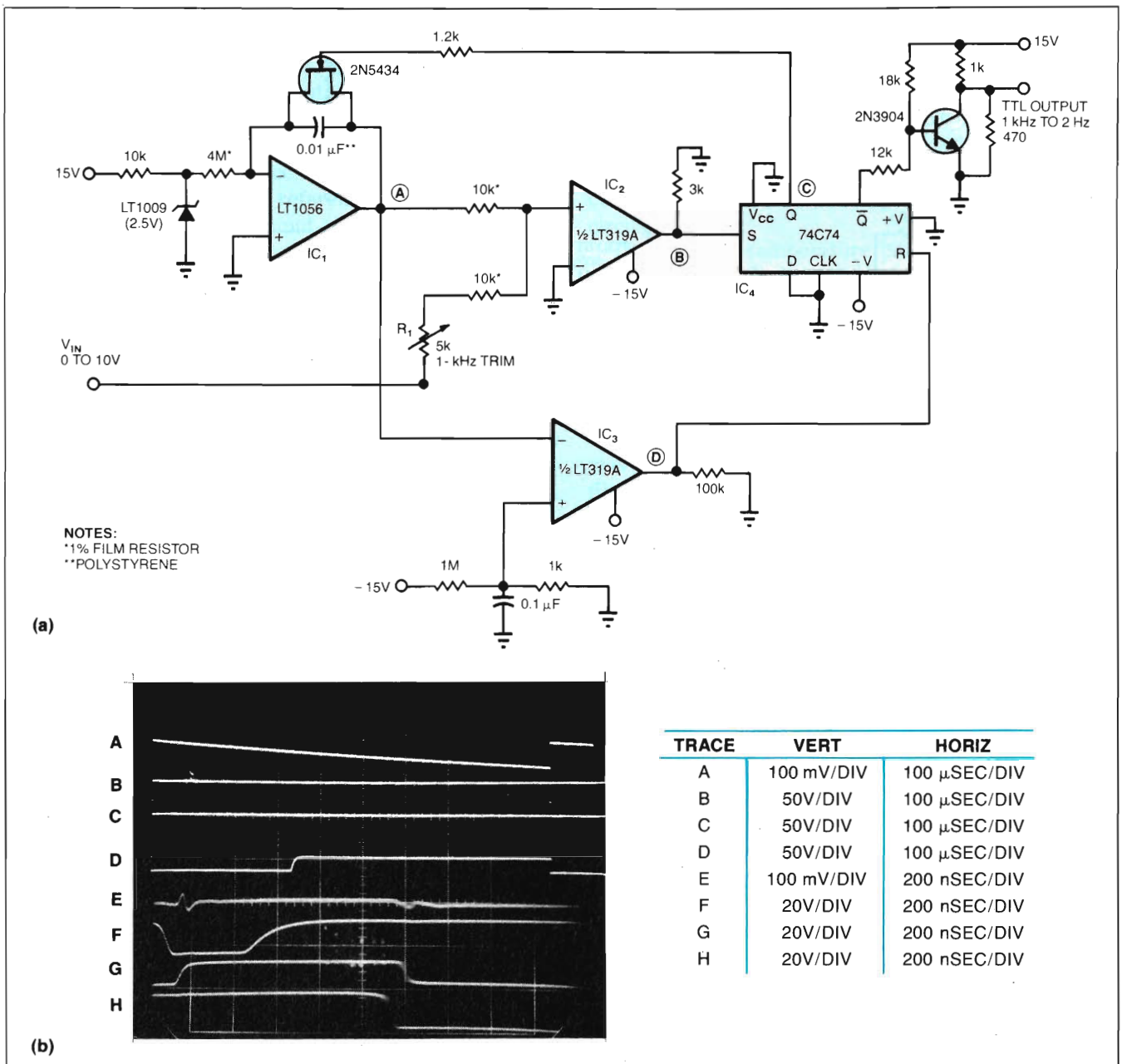
TRACE	VERT	HORIZ
A	20V/DIV	10 µSEC/DIV
B	20V/DIV	10 µSEC/DIV
C	10V/DIV	10 µSEC/DIV
D	10V/DIV (0.35% DISTORTION)	10 µSEC/DIV

Fig 3—Featuring a 1-Hz to 100-kHz sine-wave output *for a 0 to 10V input, this converter* ***(a)*** *maintains a 0.1% frequency linearity. As trace C* ***(b)*** *illustrates, output distortion is minimal—just 0.2% over the entire 100-kHz range.*

Pulse or square-wave outputs are typical for V/F converters, but sine-wave outputs are more appropriate in some cases.

function of the circuit's input voltage and varies from 1 Hz to 100 kHz with a 0 to 10V input. The LM329 diode bridge combines with the series-parallel diode network to provide a stable, bipolar reference that always opposes the sign of IC_1's output ramp. Schottky diodes D_1 and D_2 clamp IC_4's input to assure a clean recovery from any overdrive that may develop.

The AD639 trigonometric function generator, biased via IC_2, converts IC_1's triangular output into a sine wave (trace C). The AD639's triangular-wave input must not vary in amplitude, or output distortion will result. At high frequencies, delays in IC_1's integrator

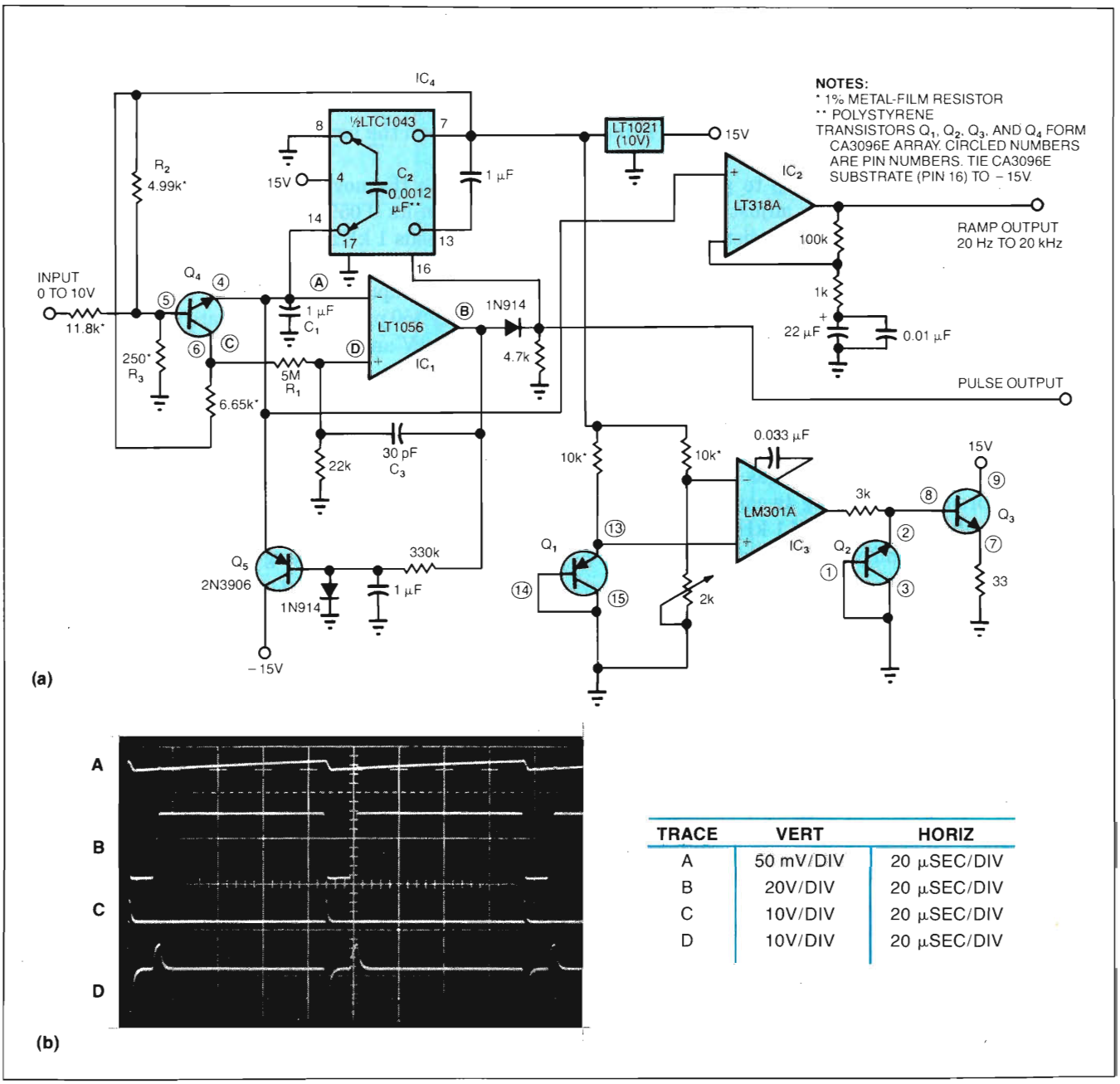


TRACE	VERT	HORIZ
A	100 mV/DIV	100 µSEC/DIV
B	50V/DIV	100 µSEC/DIV
C	50V/DIV	100 µSEC/DIV
D	50V/DIV	100 µSEC/DIV
E	100 mV/DIV	200 nSEC/DIV
F	20V/DIV	200 nSEC/DIV
G	20V/DIV	200 nSEC/DIV
H	20V/DIV	200 nSEC/DIV

Fig 4—Aimed at applications that require you to linearize a transducer output, *this network* ***(a)*** *transforms a 0 to 10V input into a 1-kHz to 2-Hz output and maintains a 1/X conformity accuracy of 0.05%. Expanded waveforms E through H* ***(b)*** *show detail of the ramp-resetting sequence.*

switching loop cause Q_1 to switch (ie, turn on and off) late. Unless the effects of the delays are minimized, triangular-wave amplitude will increase with frequency, causing distortion levels to increase commensurately. The 22-kΩ/15-pF R_3C_1 feedforward network at IC_4's input compensates for the delays, keeping distortion to just 0.2% over the entire 100-kHz range. At 10 kHz, distortion is less than 0.07%.

C_2, positioned in Q_1's source line, minimizes the effects of gate-source charge transfer, which occurs every time Q_1 switches. Without this capacitor, a sharp spike would be present at the triangular waveform's



TRACE	VERT	HORIZ
A	50 mV/DIV	20 µSEC/DIV
B	20V/DIV	20 µSEC/DIV
C	10V/DIV	20 µSEC/DIV
D	10V/DIV	20 µSEC/DIV

Fig 5—This converter's (a) output responds exponentially *to the input voltage. Exponential conformity is within 0.13% over a 10-Hz to 20-kHz range, and drift measures 150 ppm/°C. The positive ac feedback at IC_1's noninverting input (trace D in* ***b****) ensures that C_2 has enough time to discharge fully.*

Circuits that have a deliberately nonlinear transfer function represent another dimension in converter design.

peaks, increasing distortion. FETs Q_2 and Q_3 compensate for the temperature dependence of Q_1's on-resistance, keeping the +2I/−I relationship constant with temperature. The circuit's gain temperature coefficient and zero-point drift spec at 150 ppm/°C and 0.1 Hz/°C, respectively.

This circuit responds very quickly to input changes—a rarity for most sine-wave generators. To calibrate the circuit, apply a 10V input and trim the 2-kΩ potentiometer (R_4) for a symmetrical triangular-waveform output at IC_1. Next, apply a 100-μV input and trim the 50-kΩ potentiometer (R_5) for output-waveform symmetry at IC_1. Apply a 10V input and trim the 5-kΩ frequency-trim potentiometer (R_6) to generate a 100-kHz output frequency. Finally, adjust the distortion-trim potentiometers for minimum distortion as measured on a distortion analyzer (trace D). You may have to readjust the other trim potentiometers slightly to realize the lowest possible distortion.

Handling transducer outputs

Circuits that have a deliberately nonlinear transfer function represent another dimension in V/F-converter design. These converters are useful for linearizing outputs from such transducers as gas sensors and flow meters. The circuit shown in **Fig 4a** converts inputs of 0 to 10V to an output frequency of 1 kHz to 2 Hz, and it maintains a 1/X conformity accuracy of 0.05% (X represents the input).

IC_1 integrates current from the LT1009 2.5V reference. Using a current-summing network, IC_2 compares IC_1's negative output ramp (trace A in **Fig 4b**) with the input voltage. When IC_2's input goes negative, its output (trace B) falls and triggers flip-flop IC_4's Q output high (trace C). Q_1 turns on and resets IC_1's output ramp. When the ramp reset gets close to ground, IC_3 triggers (trace D). IC_3's output goes low and resets IC_4 (the Q output goes low). Q_1 turns off, and the entire cycle repeats. Waveforms E through H are expanded versions of A through D, respectively, and they show detail of the ramp-resetting sequence.

In most V/F converters, the input signal controls the integrator slope. In this circuit, the integrator runs at a fixed slope. The time required for the integrator to intersect the input voltage level is inversely proportional to the input's amplitude, and loop oscillation is related to the input according to the 1/X ratio.

Because the ramp-reset time is lost in the integration, this reset time is a first-order error term. Ramp-reset-time errors are minimal at low frequencies, even though reset takes longer; the ramp has to run longer before it intersects the input. The reset period becomes significant at higher frequencies (even though it's shorter), because its dead time represents a substantial percentage of the oscillation frequency. This circuit's 2-comparator/flip-flop reset scheme helps reduce this error by adaptively controlling and minimizing the ramp-reset time regardless of peak ramp amplitude. A simple, fixed ac feedback scheme would not perform as well, because its time constant would have to be long enough to satisfy worst-case conditions—ie, resetting the ramp from the large amplitudes encountered at low frequencies.

Even with the novel reset scheme, this circuit will not maintain its 0.05% conformity accuracy if the frequency exceeds 1 kHz. Note that the circuit has almost 10 times the accuracy of analog multipliers and other analog 1/X computing techniques. Circuit drift is approximately 150 ppm/°C. To calibrate the circuit, set the input at 50 mV and adjust the 5-kΩ trim potentiometer (R_1) to develop a 1-kHz output.

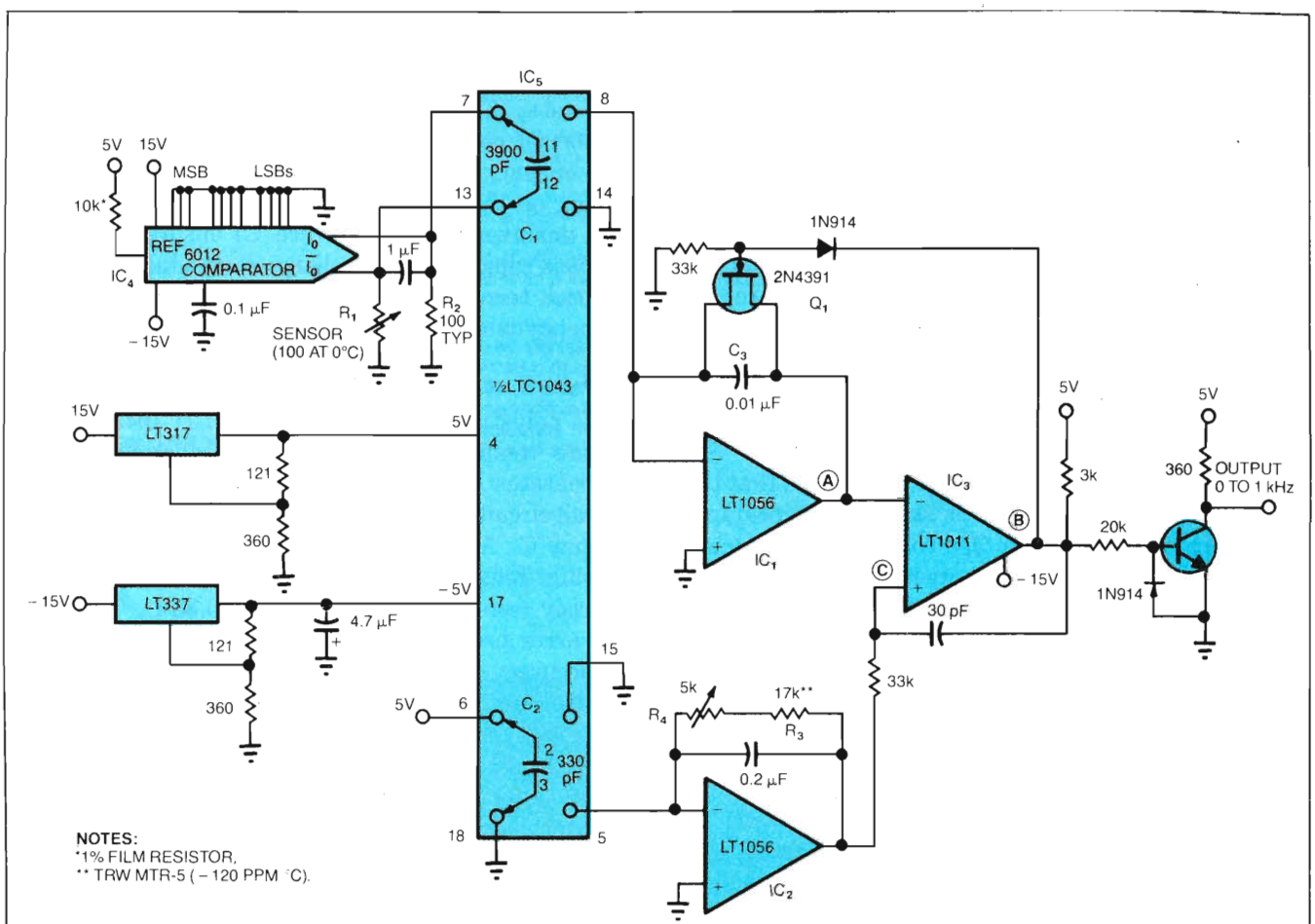
Exponential response yields tone output

The converter shown in **Fig 5a** responds exponentially to its input voltage. Suitable for electronic music synthesizers, it has an I/O scale factor of 1V/octave of frequency. Exponential conformity is within 0.13% over a 10-Hz to 20-kHz range, and drift measures 150 ppm/°C. In addition to a pulse output, the circuit provides a ramp output for applications that require substantial power at the fundamental frequency.

The 1-μF capacitor (C_1) at Q_4 integrates emitter current to form a ramp at IC_1's inverting input (trace A, **Fig 5b**). When the ramp crosses zero, IC_1's output switches (trace B), causing the LTC1043 (IC_4) to change states. Polystyrene capacitor C_2, charged to the LT1021's 10V potential, switches and pulls current from IC_1's summing point (trace C). C_3 provides positive ac feedback to IC_1's noninverting input (trace D) to ensure that C_2 has enough time to discharge fully. This action forces IC_1's input ramp to reverse direction and start resetting toward zero. When the positive feedback around IC_1 decays, the cycle repeats.

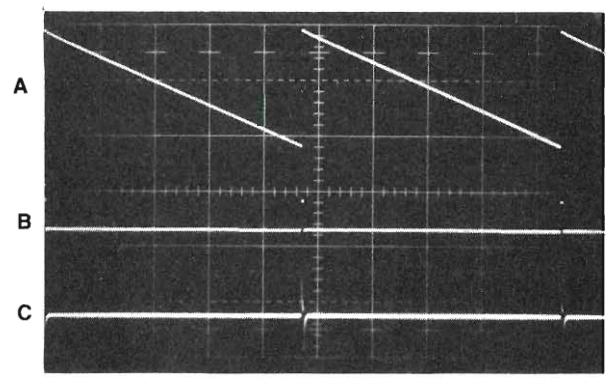
Q_5 and its associated circuitry form a local loop that ensures a proper start-up sequence. For example, input overdrive could force IC_1's output to go to the negative rail and stay there. If this event were to occur, Q_5 would turn on, pull IC_1's inverting input toward −15V, and initialize the circuit.

The oscillation frequency of this charge-pump-type



NOTES:
*1% FILM RESISTOR.
** TRW MTR-5 (– 120 PPM °C).

(a)



(b)

TRACE	VERT	HORIZ
A	1V/DIV	200 µSEC/DIV
B	5V/DIV	200 µSEC/DIV
C	2V/DIV	200 µSEC/DIV

Fig 6—Designed for resistive-based transducers, *this circuit* ***(a)*** *has an output frequency that's proportional to the ratio of the voltages across R_1 and R_2. A 0 to 100°C excursion at the platinum sensor (R_1) produces a 0- to 1-kHz output.*

Converters with ramp outputs satisfy applications that require substantial power at the fundamental frequency.

current-to-frequency converter is linearly related to Q_4's emitter current. This current, in turn, is exponentially related to the V_{BE} of Q_4. Normally, Q_4's operating point would be quite sensitive to changes in temperature. In this case, however, Q_4 is part of a transistor array that's effectively stabilized by IC_3 in the following manner.

Q_1, also part of the array, monitors temperature. IC_3 compares Q_1's V_{BE} value with a bridge potential and drives array transistor Q_3 to close a thermal-control loop. This action stabilizes the array and prevents ambient temperature shifts from influencing Q_4's operation. Q_2, operating as a clamp, guards against loop lock-up conditions and ensures that Q_3 never becomes reverse-biased.

The thermal control loop around Q_4 ensures that this circuit's exponential behavior is stable and repeatable. The 5-MΩ resistor (R_1) in Q_4's collector circuit introduces a slight shift in IC_1's operating point at high frequencies. This shift compensates for Q_4's bulk-emitter-resistance term and maintains good exponential performance to 20 kHz. The 4.99-kΩ resistor (R_2) in Q_4's base circuit sets the 0V input frequency at about 10 Hz, and the 250Ω resistor (R_3) establishes the circuit's scale factor.

Handling resistive-based transducers

The circuit in **Fig 6a** produces an output frequency that's proportional to the ratio of the voltages across R_1 and R_2. In this case, R_1 is a platinum resistance sensor, and the value of R_2 is selected to match the sensor's 0°C value. Using decade resistance boxes, you can fine-trim at the grounded end of R_2 without running into excessive noise problems. And because R_1 is also referred to ground, it can serve as a termination for a cable run and provide similar noise-rejection properties.

The 6012 D/A converter (IC_4) serves as a simple dual-current source. With only the MSB set high, the converter's output currents are equal. The constant and equal current flow through R_1 and R_2 produces a voltage differential that's sampled by the LTC1043 switched-capacitor configuration (C_1 and C_2 in IC_5). The LTC1043 continuously switches (at its internal clock rate) the 3900-pF capacitor across the resistor pair, and then it dumps the charge into IC_1's summing point. The quantity of charge delivered per cycle is a direct function of the voltage difference across R_1 and R_2 ($Q=CV$).

IC_3 compares the negative ramp output from IC_1 (trace A, **Fig 6b**) with amplifier IC_2's dc output, which is a function of IC_5's clock frequency, IC_2's 17-kΩ feedback resistor, and IC_5's 330-pF charge-pump capacitor. Because IC_1 and IC_2 are receiving charge at the same rate, IC_5's oscillator drift affects each equally, so IC_5 doesn't contribute error. When IC_1's ramp crosses IC_2's output value, IC_3's output goes high (trace B), turning on the FET (Q_1). The positive ac feedback to IC_3's noninverting input (trace C) ensures that IC_1's feedback capacitor will discharge completely. When the feedback terminates, the cycle repeats; the oscillation frequency is a linear function of the R_1/R_2 ratio.

Dead-time error is within accuracy spec

The polystyrene capacitors in the LTC1043 network provide temperature-coefficient cancellation, and R_3 compensates IC_1's polystyrene feedback capacitor (C_3). Overall circuit temperature coefficient is approximately 35 ppm/°C. As shown, a 0 to 100°C excursion at the platinum sensor produces a 0- to 1-kHz output whose accuracy (sensor-limited) measures 0.35°C. The dead-time error produced by IC_1's reset time is well within this accuracy spec, so the circuit contributes no appreciable measurement error.

In practice, you may have to trim R_2's value slightly to compensate for individual R_1 tolerances at 0°C. You set the 5-kΩ full-scale trim potentiometer (R_4) in IC_2's feedback loop to develop a 1-kHz output at a sensor temperature of 100°C. You can use this circuit with any resistive-based transducer; with negative-temperature-coefficient devices, simply reverse the positions of R_1 and R_2. **EDN**

Author's biography

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and -instrumentation design. He has served in related capacities at National Semiconductor Corp, Arthur D Little Inc, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. Jim is a former student of psychology at Wayne State University, and he enjoys tennis, art, and collecting antique scientific instruments.

Article Interest Quotient (Circle One)
High 488 Medium 489 Low 490

Follow design rules for optimum use of fast comparator IC

To fully exploit a high-speed comparator IC's capabilities, you must understand both the IC's innate attributes and the influences of the circuit environment surrounding the device. This article, first in a 3-part series, explores these attributes and influences, and provides guidelines for optimizing high-speed circuit performance.

Jim Williams, *Linear Technology Corp*

A recent high-speed comparator, the LT1016, offers complementary, TTL-compatible outputs and 10-nsec response time. The outputs directly drive all TTL families, including high-speed AS and Fairchild Advanced Schottky TTL (Fast) parts. The TTL outputs make the device easy to use in linear-circuit applications, where ECL output levels are often inconvenient. This article, first of a 3-part series, covers application and measurement techniques and discusses a number of problems associated with the high-speed circuitry the LT1016 would normally inhabit. The other two articles will provide a variety of circuit applications that exploit the device's capabilities.

The LT1016 is relatively easy to use; it's less prone to oscillation and other vagaries than some other comparators (see **box,** "A fast TTL comparator"). Unfortunately, the laws of physics dictate that you properly prepare the circuit *environment* in which the device works. The performance limits of high-speed circuitry often stem from layout considerations or from such parasitic effects as stray capacitance and ground impedance. Some of these considerations also exist in digital systems, in which you're perfectly comfortable describing bit patterns and memory-access times, for example, in terms of nanoseconds.

The LT1016 is, of course, useful in the mentioned fast digital systems; **Fig 1** gives an idea of just how fast the device is. The simple test circuit allows you to see that the comparator's response (trace B) to the pulse generator's output (trace A) is faster than that of a TTL inverter (trace C). In fact, the inverter's output never attains a TTL zero level. Linear circuits that operate with this order of speed make many designers justifiably wary. Nanosecond-domain linear circuits are widely associated with oscillations, mysterious shifts in circuit characteristics, unintended modes of operation, and outright failure to function.

Among other common problems of such high-speed

To use a high-speed comparator effectively, you must understand not only the IC itself, but also the influences and vagaries of the circuit environment surrounding the device.

linear circuits are differing measurement results when you use various pieces of test equipment, the inability to make measurement connections to the circuit without inducing spurious responses, and dissimilar operation between two supposedly identical circuits. When a circuit's design and the components used in it are sound, you can usually trace all the cited problems to an improper circuit environment. To provide a proper environment, you must study the causes of the mentioned difficulties.

The most common high-speed-circuit problem is improper power-supply bypassing. Bypassing is necessary to maintain low supply impedance. Inductance and dc resistance in supply wires and pc-board traces can easily attain unacceptable levels. These parasitics allow the supply line to fluctuate in response to changes in the

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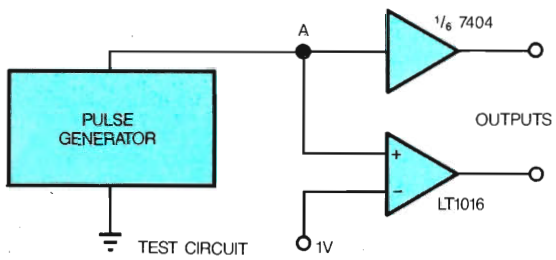


TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	5 nSEC/DIV
B	5V/DIV	5 nSEC/DIV
C	2V/DIV	5 nSEC/DIV

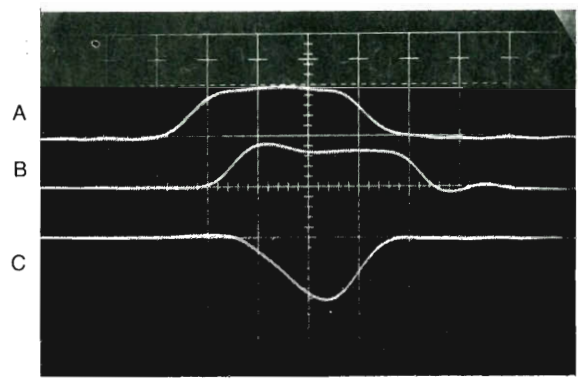
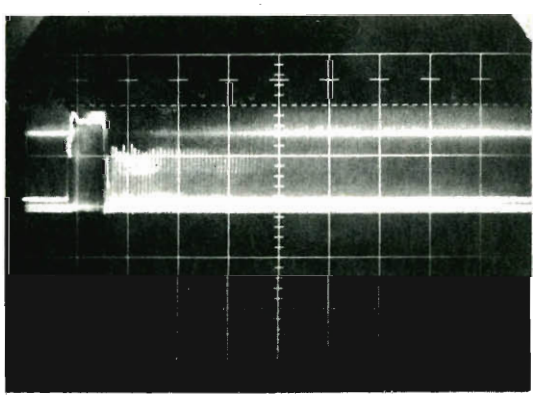
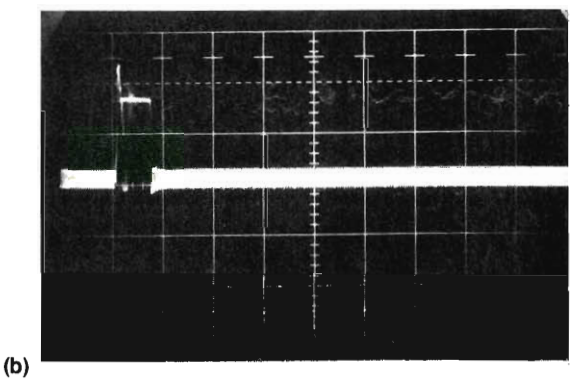


Fig 1—Faster than a TTL inverter, *the LT1016 switches (trace B) in less than 10 nsec after application of an input pulse (trace A). The TTL circuit's output (trace C) never attains 0V.*





VERTICAL	HORIZONTAL
2V/DIV	100 nSEC/DIV

Fig 2—Proper bypassing is important, *as shown by these scope photographs. The unbypassed case appears in* ***a; b*** *shows the result of inefficient bypassing (capacitors either too distant from the LT1016 or excessively lossy).*

A fast TTL comparator

The LT1016 is a fast (10-nsec typ propagation delay) comparator that provides a direct interface to TTL logic while operating from either one 5V supply or dual ±5V supplies. The IC offers matched complementary outputs and a latch pin for input-data retention at the outputs.

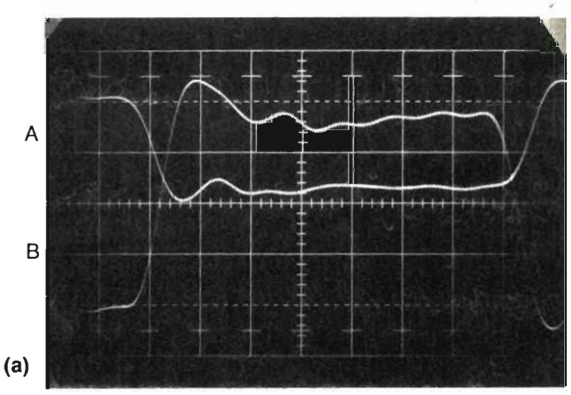
The LT1016's output stage provides active drive in both directions for high-speed drive into TTL logic or passive loads, yet does not exhibit the large current spikes usually found in totem-pole output stages. This attribute eliminates the need for a minimum slew-rate spec for the input signal, a spec that typically encumbers other very fast comparators.

TABLE1—LT1016A KEY SPECIFICATIONS

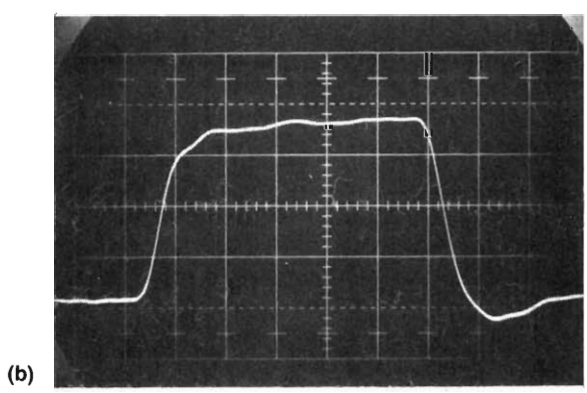
PARAMETER	SPEC
INPUT OFFSET VOLTAGE	1.5 mV MAX
OFFSET-VOLTAGE DRIFT	10 μV/°C MAX
INPUT BIAS CURRENT	10 μA MAX
INPUT-VOLTAGE RANGE	V_{CC} – 1V V_{EE} + 1.25V
COMMON-MODE REJECTION	80 dB MIN
VOLTAGE GAIN	2000 MIN
PROPAGATION DELAY (5-mV OVERDRIVE)	12 nSEC MAX
V_{CC} CURRENT	35 mA MAX
V_{EE} CURRENT	5 mA MAX

Another factor that makes the LT1016 easier to use than other high-speed comparators is the fact that its outputs are stable when the device operates in its linear region, regardless of how slowly the input signal changes. This trait eliminates the problem of output chatter in the presence of slow-moving or dc-input signals.

Finally, the LT1016's quiescent negative-supply current is typically 2.5 mA—approximately 10 times lower than that of other very fast, bipolar comparators. This feature allows you to drive the negative-supply pin from any negative supply by using a simple resistive divider.



VERTICAL	HORIZONTAL
2V/DIV	10 nSEC/DIV



VERTICAL	HORIZONTAL
1V/DIV	50 nSEC/DIV

Fig 3—Proper selection and use of probes *is all important. In* ***a,*** *a miscompensated probe yields a grossly exaggerated output (8V vs the true 5V); in* ***b,*** *an overcompensated (or insufficiently fast) probe delivers an unduly slow output to the oscilloscope.*

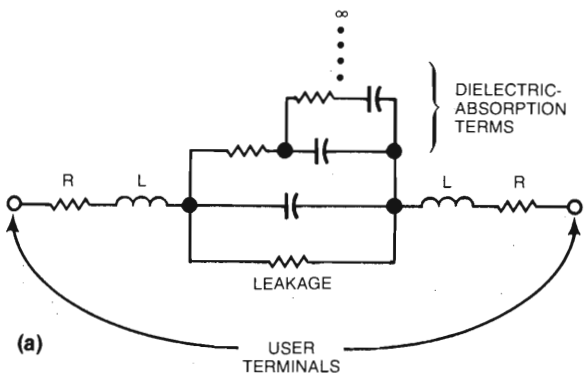
Choose bypass-capacitor types and values with care

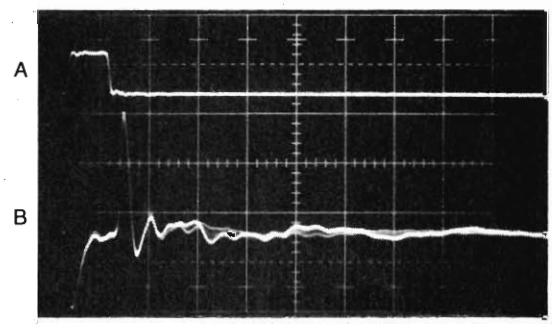
Bypass capacitors serve to maintain low power-supply impedance at the point of load. Because of parasitic resistance and inductance in supply lines, the supply impedance can often be very high. As frequency rises, the inductive parasitic becomes particularly troublesome. Even if these parasitic terms did not exist, or if you use local regulation, bypassing is still necessary because no power supply or regulator has zero output impedance at, say, 100 MHz.

The type of bypass capacitor to use is a function of the application, frequency domain of the circuit, cost, board space, and many other considerations. However, you can make some useful generalizations. All capacitors' equivalent circuits contain parasitic terms, some of which appear in **Fig Aa.**

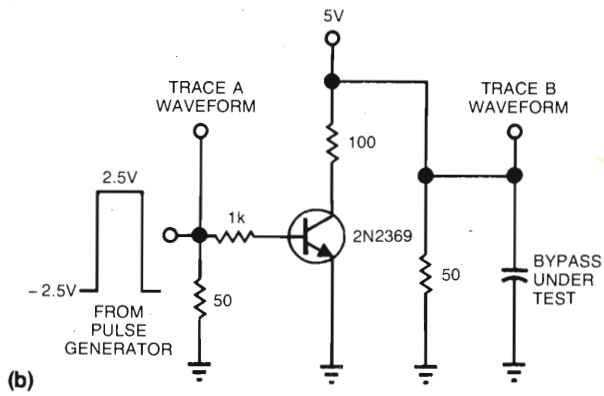
In bypass applications, leakage and dielectric absorption are secondary terms, but series inductance and resistance are not. These last two terms limit the capacitor's ability to damp transients and to maintain low supply impedance. Bypass capacitors must often have large values so they can absorb long transients. In these cases, it's necessary to use electrolytic types, which exhibit high-value series inductance and resistance.

Different types of electrolytics —both polar and nonpolar—have markedly different characteristics, and the type (or types) to use is sometimes a subject of debate. In choosing a bypass ca-





TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	100 nSEC/DIV
B	1V/DIV	100 nSEC/DIV



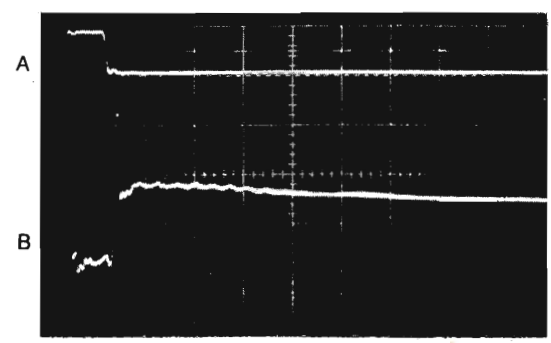


Fig A—Understand the all-important bypass capacitors *when you're designing high-speed circuitry. The diagram in* ***a*** *is the equivalent circuit of a capacitor. The important parasitics for bypassing are series inductance and resistance. The circuit in* ***b*** *allows you to test bypass capacitors. The scope photographs show the response with the various bypass combinations described.*

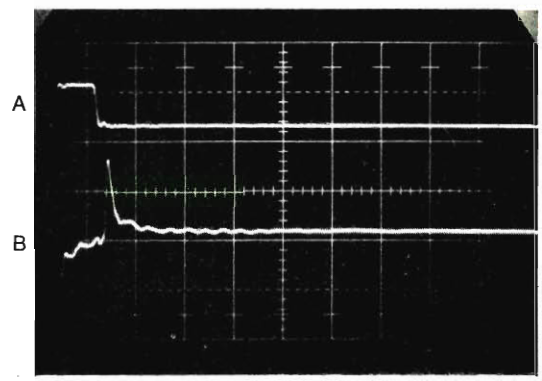
pacitor, the test circuit in **b** and the accompanying scope photos can perhaps be useful. The photos show the response of five bypassing methods to the transient generated by the test circuit.

The photo in **c** shows an unbypassed line, whose voltage sags and ripples badly at high amplitudes. In **d**, a 10-μF aluminum electrolytic cuts the disturbance considerably, but the potential for trouble still exists.

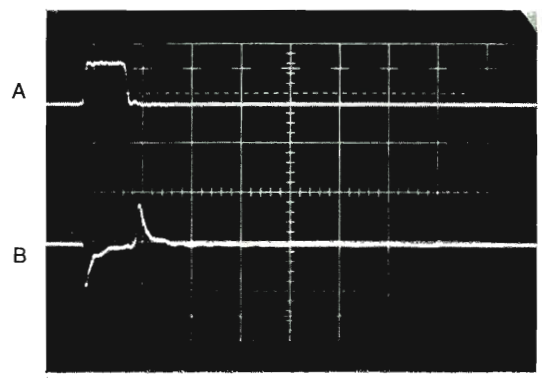
A 10-μF tantalum unit (**e**) offers cleaner response; a 10-μF aluminum combined with a 0.01-μF ceramic type (**f**) is even better. Combining electrolytics with other capacitor types (usually ceramic) is a popular way to obtain good response, but beware of picking the wrong duo.

Choosing the right pair is not an easy task. Circuit characteristics (including line inductance and the nature of the signals you're dealing with) and the capacitors' parasitic terms both play a role. The photo in **g**, for example, shows the results of using a parallel combination of a 10-μF aluminum electrolytic and a 0.1-μF ceramic capacitor in the test circuit. Note the resonant, ringing response.

The preceding example shows that you must tailor bypass capacitors and capacitor combinations to your particular system. And this tailoring is more an empirical task than an analytical one. In other words, experiment with various bypass components in your system until you achieve the best results.



(e)



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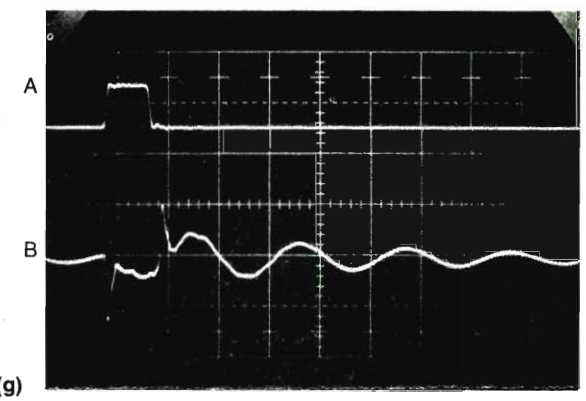

(g)

TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	100 nSEC/DIV
B	0.1V/DIV	100 nSEC/DIV

A high-speed IC needs a rock-stable and impedance-free supply to do its job properly. Therefore, supply bypassing is not only beneficial, but crucial.

internal characteristics of the devices connected to it. This fluctuation almost always causes unruly operation.

What's more, several devices connected to an unbypassed supply can effectively communicate through the finite supply impedances, thereby provoking erratic operating modes. Bypass capacitors, by providing local reservoirs of energy at the device level, represent a simple way to eliminate this communication. The bypass capacitor acts like an electrical flywheel that keeps supply impedances low at high frequencies. The choice of capacitor type for bypassing is a critical issue, so weigh your decision carefully (see **box,** "Choose bypass-capacitor types and values with care").

Fig 2a shows the response of an unbypassed LT1016 to a pulse input. The power supply that the comparator sees at its terminals has high impedance at high frequencies. This impedance forms a voltage divider with the LT1016, allowing the supply voltage to move in response to changes in the comparator's internal conditions. The supply instability causes local feedback, and oscillation occurs. Although the LT1016 responds to the input pulse, its output is a blur of 100-MHz oscillation.

In **Fig 2b,** the comparator's supplies are bypassed, but it still oscillates. This oscillation has two possible causes: The bypass units are either too far from the LT1016, or they're lossy capacitors. These examples suggest two rules: *Use capacitors with good high-frequency characteristics, and mount them as closely as possible to the LT1016.* Even an inch of wire between the capacitor and the comparator can cause problems.

Perhaps number two in the list of circuit-environment problems is the use of improper—or the improper use of—oscilloscope probes. In **Fig 3a,** the comparator is properly bypassed, but a new problem arises. The photo shows both outputs of the comparator. Trace A appears normal, but trace B shows an excursion of almost 8V—quite a feat for a device running from one 5V supply. This anomaly is commonly reported in high-speed circuits, and it can be very confusing.

The anomaly arises from a grossly miscompensated or improperly selected oscilloscope probe. This example prompts another rule of thumb in working with high-speed circuitry: *Use probes that match your oscilloscope's input characteristics, and compensate the probes properly.* (For a further discussion of probes, see **box,** "Oscilloscopes and probes: Choose and use wisely.")

Fig 3b shows another probe-induced problem. Here, the amplitude seems correct, but the 10-nsec-response LT1016 exhibits 50-nsec edges. In this case, the probe

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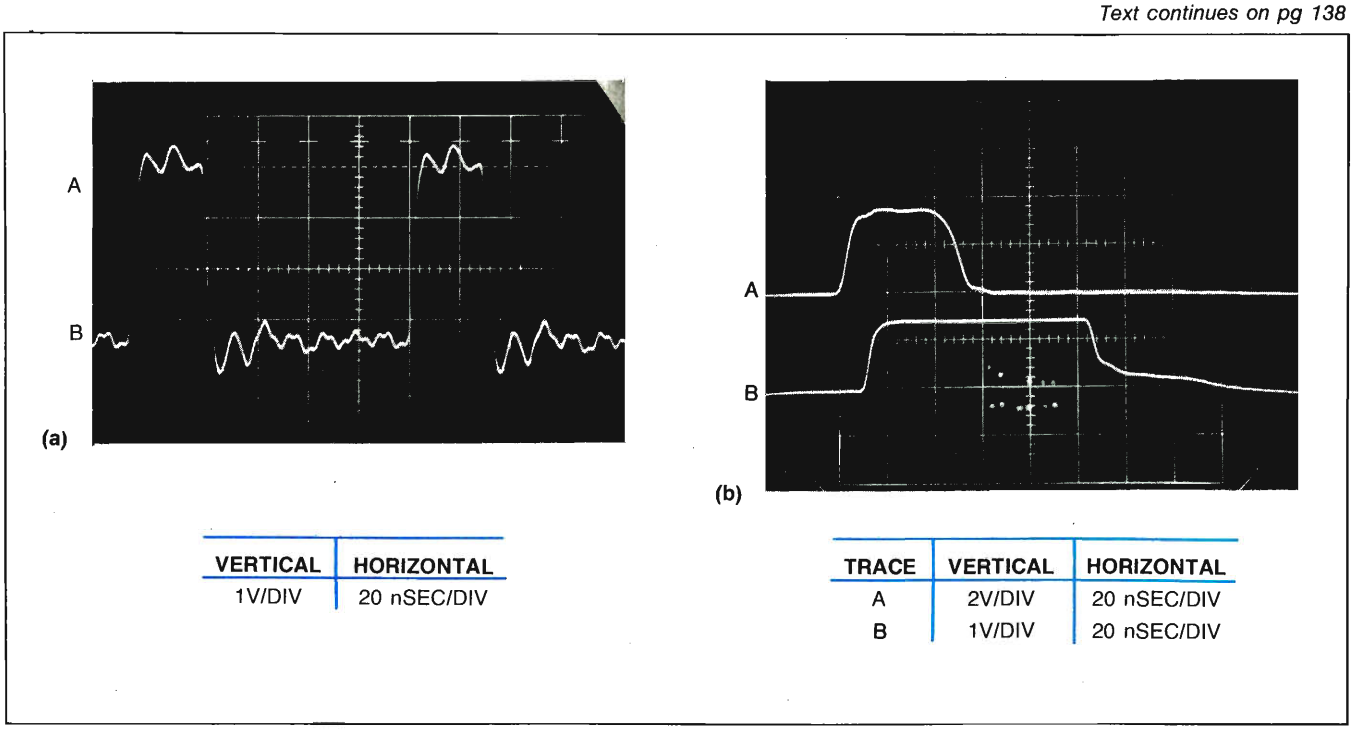
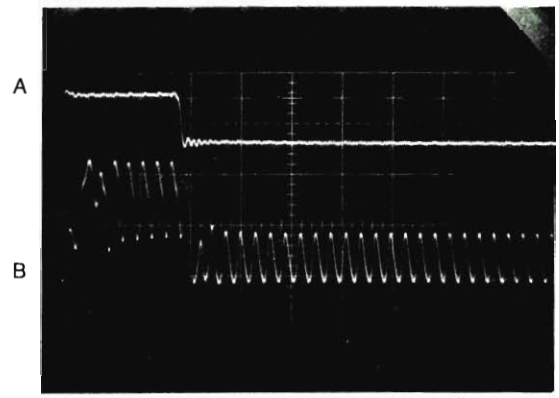


VERTICAL	HORIZONTAL
1V/DIV	20 nSEC/DIV

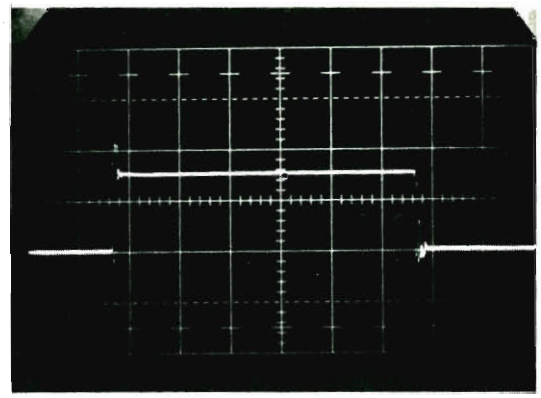
TRACE	VERTICAL	HORIZONTAL
A	2V/DIV	20 nSEC/DIV
B	1V/DIV	20 nSEC/DIV

Fig 4—More probing-caused problems *afflict these waveforms. In* ***a,*** *the probe's too-long ground lead causes ringing and distortion; in* ***b,*** *a badly overdriven FET probe delivers false information to the oscilloscope.*



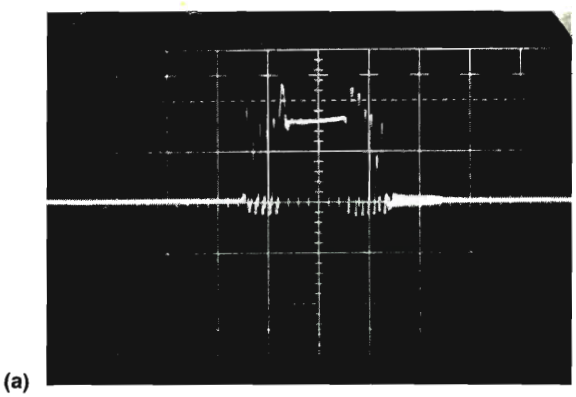
TRACE	VERTICAL	HORIZONTAL
A	1V/DIV	100 nSEC/DIV
B	2V/DIV	100 nSEC/DIV

Fig 5—Improper grounding of high-speed ICs *can lead to disaster. Trace B is the output of an LT1016 whose ground lead is 1 in. in length. The comparator oscillates at approximately 40 MHz. To avoid such problems, keep the IC's ground lead to less than ¼ in. in length.*

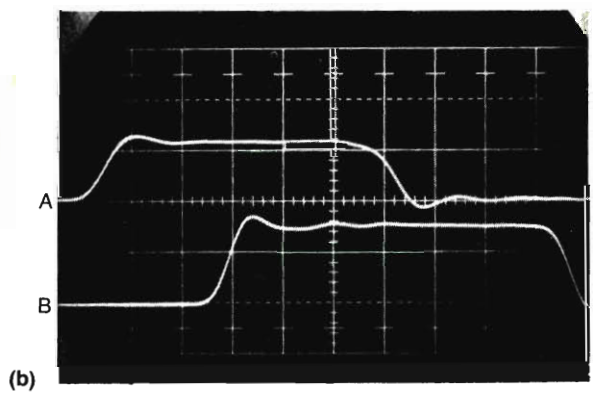


VERTICAL	HORIZONTAL
2V/DIV	100 nSEC/DIV

Fig 6—Failure to use a ground plane *provokes the chattering edges on this waveform. A ground plane in this example would have reduced inductance sufficiently to eliminate the chatter.*



VERTICAL	HORIZONTAL
2V/DIV	50 nSEC/DIV



VERTICAL	HORIZONTAL
2V/DIV	10 nSEC/DIV

Fig 7—Stray capacitance from output to input *causes the singing on the edges of the waveform in* ***a****. A lower source impedance at the comparator's input and some attention to input and output lead routing would cure this condition. More stray-capacitance-induced woes are evident in* ***b****, where the culprit is the stray capacitance to ground at the comparator's input.*

Oscilloscopes and probes: Choose and use wisely

In high-speed-design work, the choice of an oscilloscope-probe combination is the most important decision you must make. Ideally, the oscilloscope should have at least 150-MHz bandwidth for work with the LT1016, but slower instruments are acceptable if you have a good understanding of their limitations. Be aware of your scope's behavior with respect to input impedance, noise, overdrive recovery, sweep nonlinearity, triggering, channel-to-channel feedthrough, and other characteristics.

Probes are the most overlooked cause of oscilloscope mismeasurement. All probes have some effect on the points they measure. The most obvious effect usually stems from the probe's input resistance, but input capacitance usually dominates in high-speed measurements. You can lose much time investigating circuit events that actually stem from improperly selected or applied probes.

An 8-pF probe observing a point with 1-kΩ source impedance, for example, will produce an 8-nsec lag—similar to the LT1016's response time. Low-impedance probes (with 50Ω to 1-kΩ resistance) usually have input capacitance of 1 or 2 pF; these probes are a good choice if you can tolerate the low resistance.

FET probes maintain high input resistance and keep capacitance at the 1-pF level, but have substantially more delay than passive probes. FET probes also impose limitations on common-mode input range; you must respect the limits or serious measurement errors will occur. Contrary to popular belief, FET probes do not have *extremely* high input resistance—for some types, it's as low as 100 kΩ.

The passive, transformer-based types of current probes are fast and they introduce less delay than the versions based on the Hall effect. The Hall-effect types, however, respond at dc and low frequencies, while the transformer-based probes typically roll off at approximately 100 to 1000 Hz. Both types have saturation limitations which, when exceeded, cause odd CRT-display results that can be confusing.

When using different probes, remember that each has a different delay time; therefore, apparent timing errors will occur on the oscilloscope screen. Know what the individual probe delays are, and account for them in interpreting the CRT display.

The greatest source of error by far in probe use is improper grounding. Poor probe grounding can cause ripples and discontinuities in the observed waveform. In some cases, the choice and placement of a probe's ground connection can affect waveforms on another channel. In the worst case, connecting a probe's ground wire can virtually disable the circuit you're measuring.

The cause of the cited problems is parasitic inductance in the probe's ground connection. In most oscilloscope measurements, the inductive effect is not a problem, but at nanosecond speeds it becomes critical. Fast probes are always supplied with a variety of spring clips and accessories designed to aid in minimizing the inductance of the connection to ground. Most of these attachments assume a ground plane is in use (as it should be). Always try to make the shortest possible connection to ground—anything longer than 1 in. can cause trouble.

The simple network in **Fig Aa** shows just how easy it is for poorly chosen or improperly used probes to cause bad results. A 9-pF input-capacitance probe with a 4-in. ground strap monitors the output, seen in **b**, trace B. Although the input (trace A) is clean, the output contains ringing.

Using the same probe with a ¼-in. spring-tip ground-connection accessory seems to clean up everything (**c**). However, substituting a 1-pF FET probe (**d**) reveals a 50% amplitude error in **b**'s measurement. The FET probe's low input capacitance allows a more accurate display of the circuit's action.

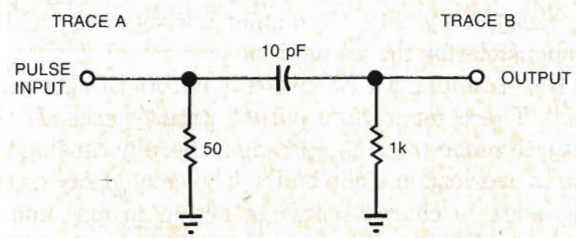
The FET probe does, however, contribute its own form of error. Note that the probe's response is tardy by 5 nsec, owing to the delay in its active circuitry. Hence, you must make separate measurements with each probe to determine the amplitude and timing parameters of the output.

In **e**, probes A, B, E, and F are standard types equipped with various forms of low-impedance grounding attachments. The conventional ground lead used with probe G is the most convenient to work with, but causes ringing and other effects at high frequencies, thereby rendering the probe virtually useless.

Probe H has a very short ground lead. This lead is better, but can still cause trouble at high speeds. C is a FET probe. The active circuitry in the probe and a very short ground connector ensure low parasitic capacitance and inductance. D is a separate FET-probe attenuator head. Such heads allow use of the probe at high voltage levels (eg, ±10 or ±100V). You can mount the miniature coaxial connector on the circuit board, then mate the probe to it. The coaxial technique provides the lowest possible parasitic inductance; therefore, it's recommended.

Probe I is a current probe; it usually doesn't require a ground connection. However, at high speeds, the ground connection might result in a cleaner CRT presentation. Because no current flows in the ground lead of these probes, a long strap is usually permissible.

A final form of probe is the human finger (J). Probing the circuit with a finger can accentuate desired or undesired effects, thereby giving clues to circuit behavior. You can use a finger, for example, to introduce stray capacitance into a suspect circuit node while observing results on a CRT. You can use two fingers, lightly moistened, to provide an experimental resistance path. Some high-speed-circuit engineers are particularly adept at these techniques, and can estimate the simulated capacitive and resistive effects with surprising accuracy.



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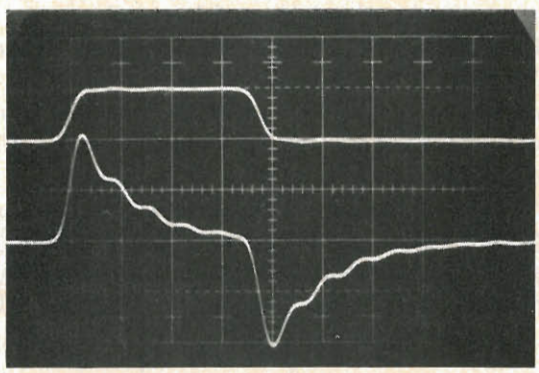

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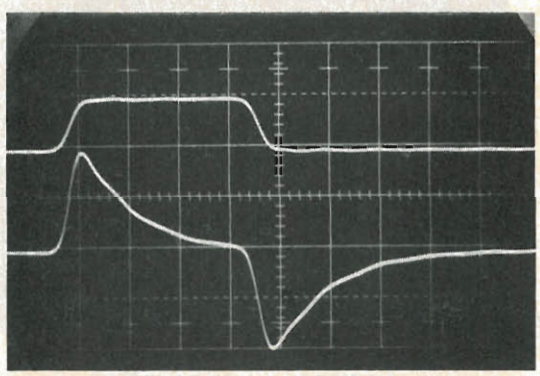
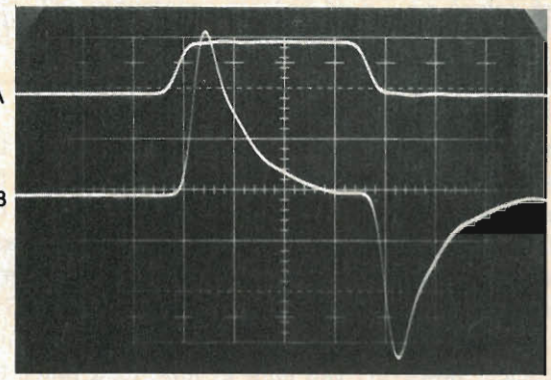
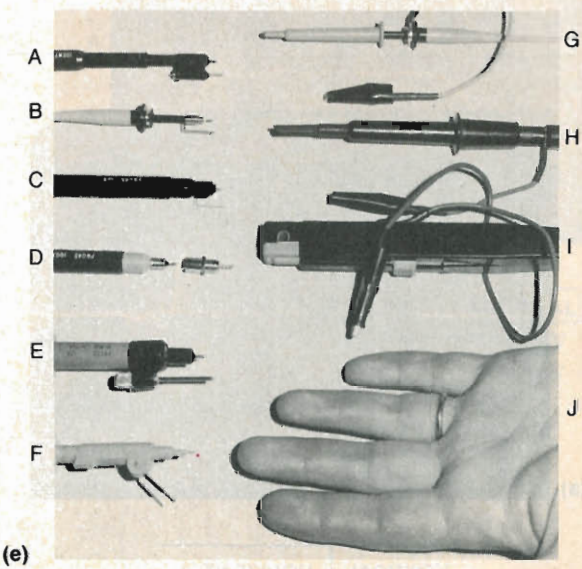


(c)



(d)

TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	10 nSEC/DIV
B	1V/DIV	10 nSEC/DIV



(e)

Fig A—Choosing, and correctly using, appropriate probes *is crucial in working with high-speed circuitry. The test network in* ***a*** *serves as an evaluation vehicle for various probes. In* ***b,*** *the probe's long ground lead causes ringing. A shorter ground strap* ***(c)*** *cleans up the ringing, but the FET probe's low input capacitance shows in* ***d*** *that the previous probe's high capacitance led to amplitude errors. Various types of probes and ground attachments are shown in* ***e.***

A prevalent cause of measurement problems, the improper choice or use of scope probes can lead to misleading or false results when testing high-speed circuitry.

used is too heavily compensated or too slow for the oscilloscope. Never use, for example, 1X (unattenuated) probes. Their bandwidth is 10 to 20 MHz or less, and their capacitive loading is high. The rules: *Check probe bandwidth to ensure that it's adequate for the measurement. Equally important, use an oscilloscope with adequate bandwidth.*

Additional probe problems

Limited bandwidth and capacitive loading are not the only sources of probe-induced woes. In **Fig 4a,** the probes are properly selected and compensated, but the LT1016's output rings and distorts badly. In this case, the probe's ground lead is too long. For general-purpose work, most probes use ground leads about 6 in. long. At low frequencies, this length is fine—at high frequencies, however, the long ground lead takes the form of an inductor, and the illustrated ringing occurs.

High-performance probes are always supplied with some short ground straps to deal with the problem. Some come with very short spring clips that mate directly with the probe tip to facilitate a low-impedance ground connection. For high-speed work, the ground connection to the probe should not exceed 2 in. in length. *Keep the probe's ground connection as short as possible.*

A final probe-induced problem causes the aberrations of **Fig 4b.** The problems in trace B are delays and insufficient amplitude. A small delay on the leading edge is followed by a long delay before the falling edge begins. In addition, a lengthy, tailing response stretches to 70 nsec before finally settling. The amplitude rises to only 1.5V. A common oversight in probing is responsible for these conditions.

In this example, a FET probe monitors the LT1016's output. The comparator's output greatly exceeds the probe's common-mode input range, thereby causing the probe to overload and clip badly. The small delay on the rising edge is characteristic of active probes and is legitimate. During the time the LT1016's output is high, the probe is driven deeply into saturation. When the output drops, the probe's recovery is lengthy and uneven, causing the delay and long tail.

Thus, some final probe-related rules: *Know your FET probe. Take account of the delay of its active circuitry. Avoid saturation effects arising from common-mode input limitations (typically ±1V). Use 10X and 100X attenuator heads when required.*

Fully as important as—and closely related to—the bypassing issue, proper grounding is crucial in any high-frequency application of the LT1016 (or any other high-speed IC). **Fig 5,** for example, shows the LT1016's

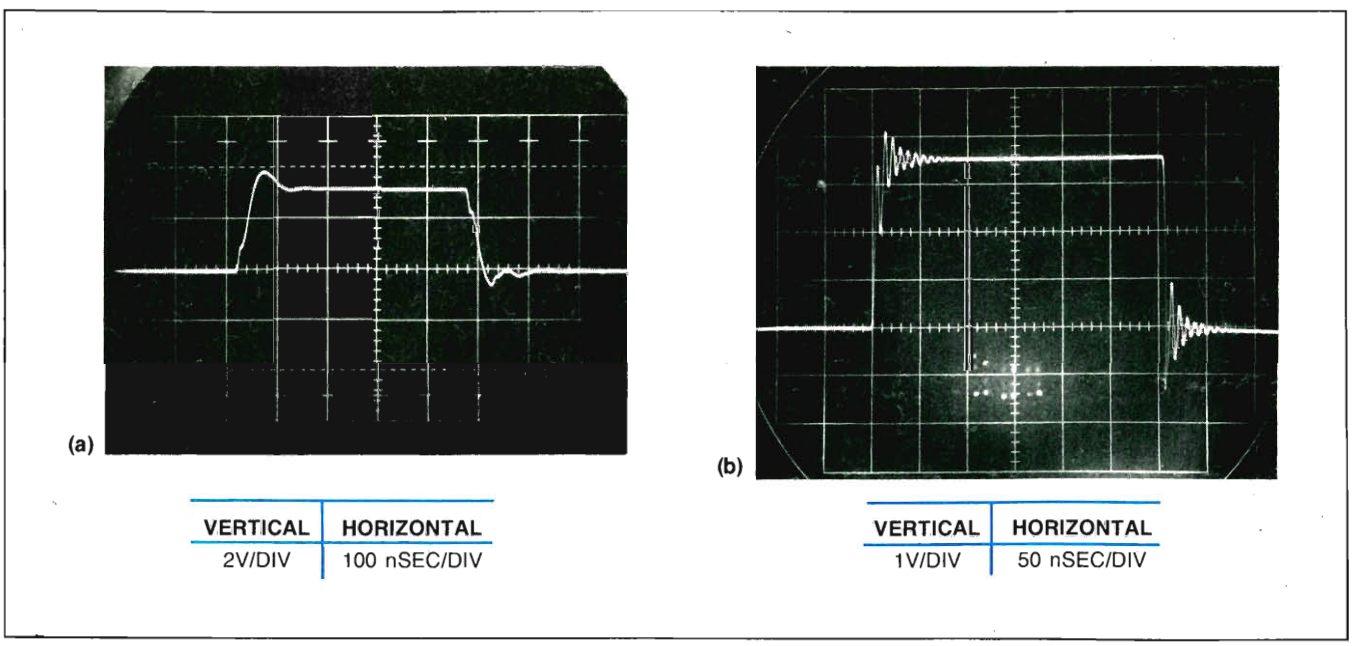
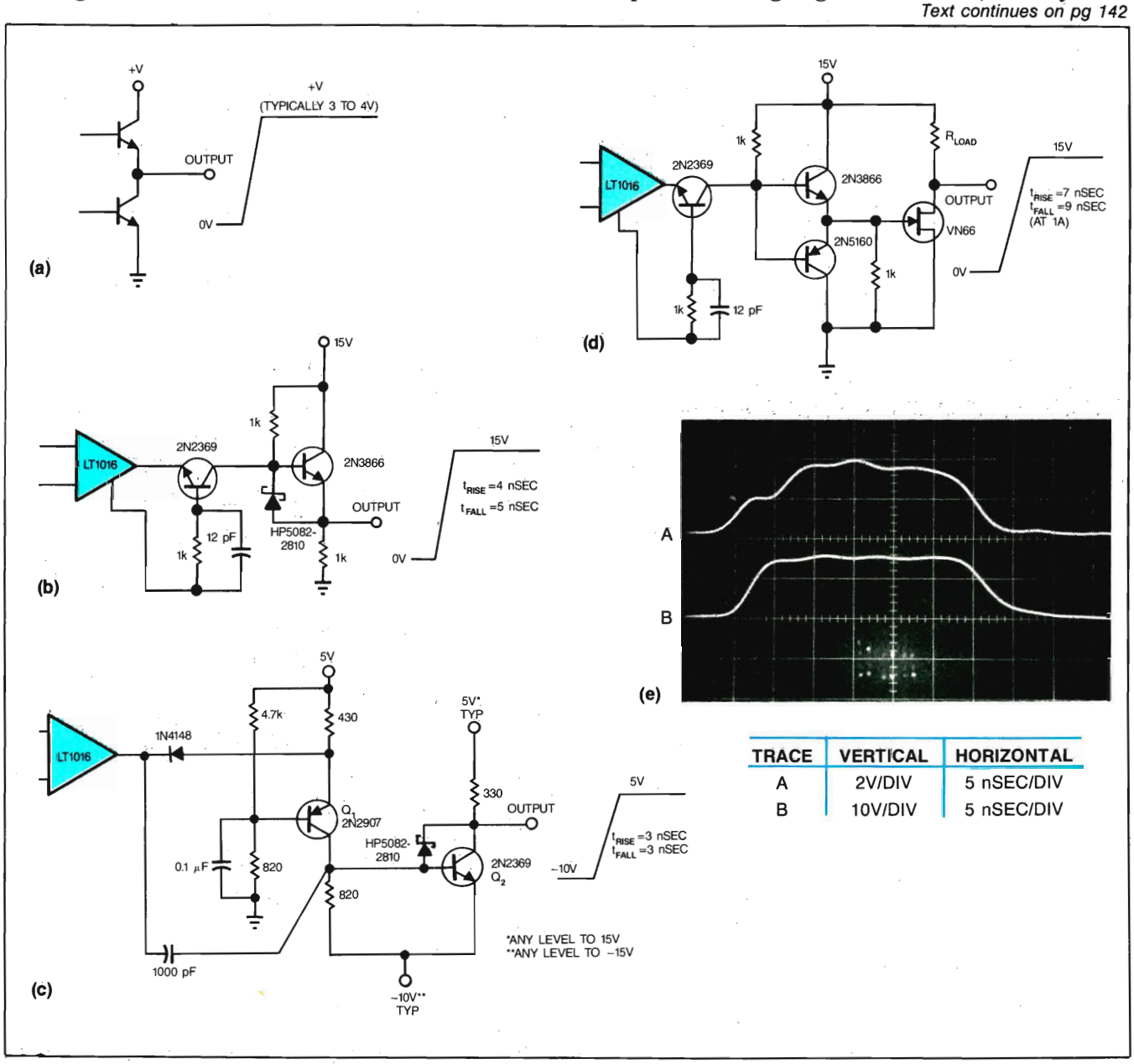


***Fig 8—Beware of output-loading problems** in using the LT1016. In **a,** a large capacitive load causes distortion and slow response on the output's edges. For heavy capacitive loads, use a buffer. In **b,** the LT1016 faces a load that resembles an unterminated transmission line. The solution is to terminate the line with a resistor, or to shorten the output-lead length.*

output (trace B) oscillating at approximately 40 MHz as it responds to an input (trace A). Note that the input signal shows traces of the oscillation. The problem in this example is improper grounding of the comparator. In this case, the LT1016's ground-terminal connection is 1 in. long.

The ground lead of the LT1016 must be as short as possible, and it must be connected directly to a low-impedance ground point. Any substantial impedance in the comparator's ground path will generate effects like those shown in **Fig 5.** The source of the malady is related to the necessity for bypassing the power supplies. The inductance created by a long device ground lead permits mixing of ground currents, thereby caus-

Text continues on pg 142



TRACE	VERTICAL	HORIZONTAL
A	2V/DIV	5 nSEC/DIV
B	10V/DIV	5 nSEC/DIV

Fig 9—Level shifting is not a trivial task. *These level-shifting circuits take advantage of the LT1016's sink-source output* **(a)** *to provide shifting with very small delays. The shifters suit various applications. The circuit in* **b,** *for example, provides a 15V unipolar output. The configuration in* **c** *allows you to vary the levels;* **e** *shows waveforms for this circuit. The setup in* **d** *provides a 15V, 1A output.*

Understand the rules for ground planes

The term "ground plane" crops up frequently in discussions of high-frequency circuit layout, most often as a mystical and ill-defined cure for spurious circuit operation. In fact, there is little mystery surrounding the usefulness and operation of a ground plane, and—like so many phenomena—its fundamental operating principles are surprisingly simple.

Ground planes are primarily useful for minimizing circuit inductance; they do so in accordance with basic magnetic theory. Current flowing in a wire produces an associated magnetic field. The field's strength is proportional to the current and the distance from the conductor.

You can thus visualize a current-carrying wire (**Fig Aa**) surrounded by magnetic-field lines. The unbounded field diminishes with distance from the wire. A wire's inductance is defined as the energy stored in the field set up by the wire's current. Computing the inductance requires integrating the field over the wire's length and the total radial area of the field.

The inductance calculation implies integrating the magnetic field on the radial line from the wire's radius to infinity. However, consider **Fig Ab**, in which two parallel wires in space carry the same current in opposite directions. The fields essentially cancel, and the inductance in this case is much lower than in the case of the single wire. You can make this inductance arbitrarily small by reducing the distance between the two wires.

The reduction of inductance between current-carrying conductors is the underlying operating principle of ground planes. In a normal circuit, the path that a current takes from its signal source, through a conductor, then back to ground includes a large loop area. The loop area gives rise to a high inductance for the conductor, thereby producing ringing because of tank-circuit effects. It's worth noting that 10 nH at 100 MHz has an impedance of 6.3Ω, so a mere 10 mA produces a 63-mV drop.

A ground plane provides a return path directly under the signal-carrying conductor, a path through which return currents can flow. Thanks to the small separation of the conductors, the inductance is low. The return current has a direct path to ground, regardless of the number of branches associated with the conductor. Currents always flow through the return path of lowest impedance. In a properly designed ground plane, this path is directly under the signal conductor.

In a practical circuit, it's desirable to make a ground plane of one entire side of the pc card —usually the component side, for wave-soldering considerations—and run the signal conductors on the other side. This technique provides a low-impedance path for all return currents.

There are some practical hints about ground planes.

- On the component side of the board, devote as much area as possible to a ground plane (especially under traces that operate at high frequencies).
- Mount components that conduct substantial fast-changing currents as closely as possible to the board. Such items include termination resistors, ICs, transistors, and decoupling capacitors.
- Where common ground potential is important (eg, at comparator inputs), try to ground the components at one point on the ground plane, thereby avoiding ac drops.
- Keep trace lengths short. Inductance varies directly with length, and no ground plane provides perfect cancellation.

In the circuit in **c**, for example, good practice dictates that, insofar as possible, grounds 2, 3, 4, and 5 connect to one point. Fast-changing, large currents must flow through R_1, R_2, D_1, and D_2 during the D/A converter's settling time. You should thus mount these components close to the ground plane, thereby minimizing their inductance.

R_3 and C_1 carry no current, so their inductance is of minor importance. You could insert them vertically to save space and to allow point 4 to more easily share a single-point ground with points 2, 3, and 5. In critical circuits, you must often trade the beneficial effects of lowered inductance for the loss of a single-point ground.

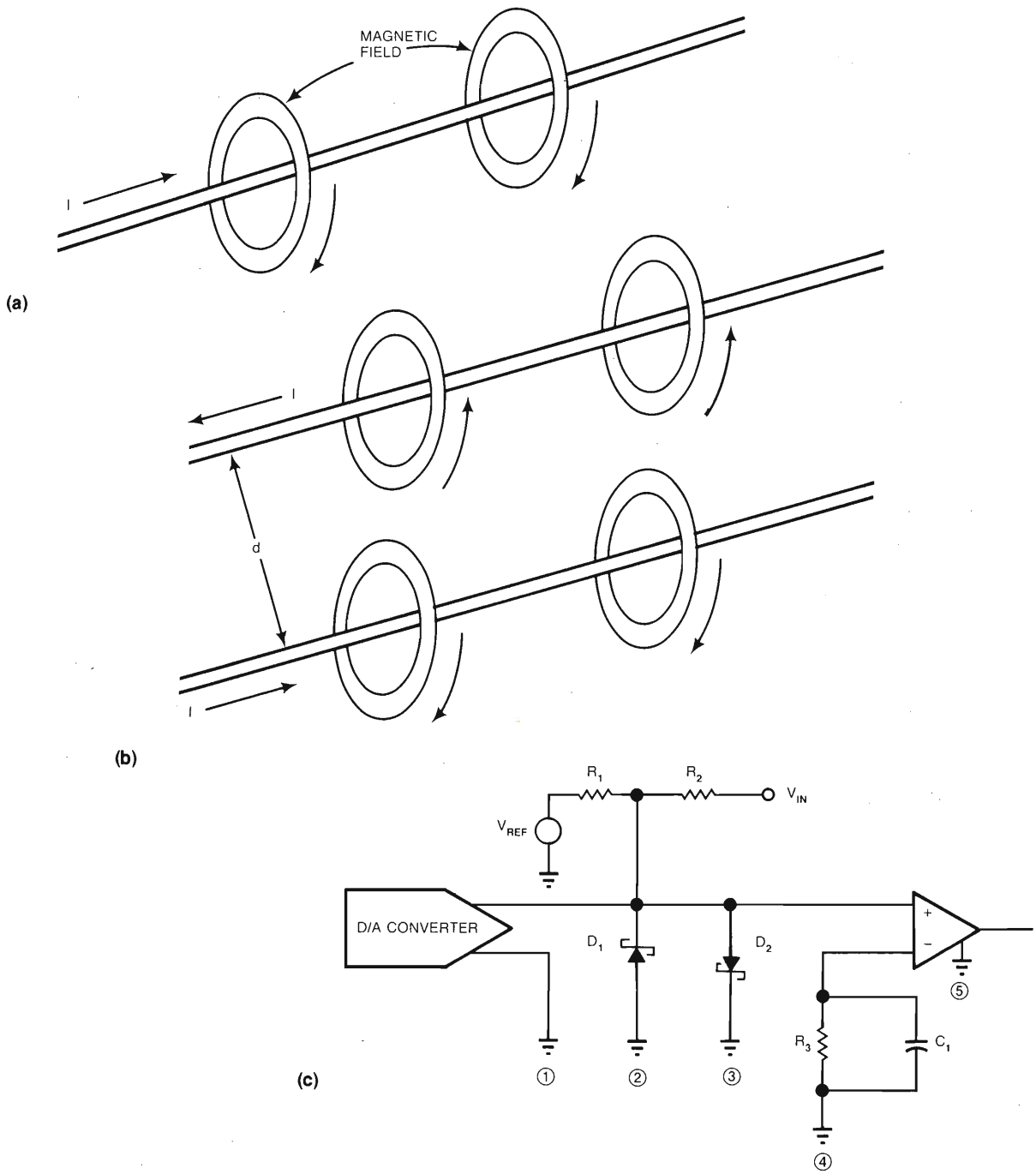
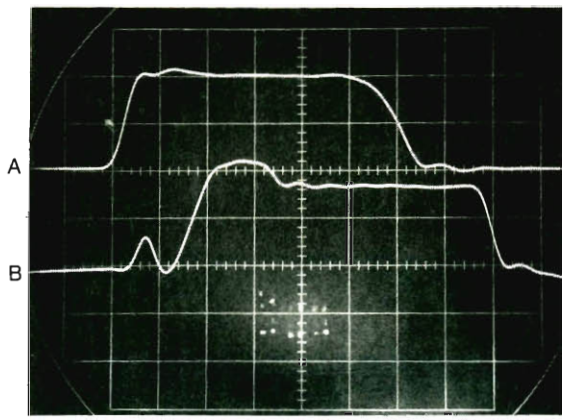


Fig A—Not a convenience, but a necessity: *Ground planes are essential in high-speed circuitry. They minimize inductance by cancelling the magnetic fields generated by currents in conductors. The diagrams in* **a** *and* **b** *show the fields and cancellation thereof. In the circuit example in* **c,** *it's important to provide a single-point ground for the components carrying fast-switching currents.*



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	20 nSEC/DIV
B	2V/DIV	20 nSEC/DIV

Fig 10—Grossly overdriving the LT1016's inputs *can result in output aberrations, as seen in trace B. Keep common-mode input voltages within spec-sheet limits at all times.*

ing undesired effects in the IC. The fix here is simple: *Keep the LT1016's ground connection as short as possible (typically ¼ in.), and run it directly to a low-impedance ground. Do not use sockets.*

To further illustrate the importance of using a low-impedance ground, **Fig 6** shows the effects of failing to use one. In this example, the output is clean except for chattering around the rising and falling edges. Here, the LT1016 operates without a ground plane (see **box,** "Understand the rules for ground planes"). You form a ground plane by placing a continuous conductive plane over the surface of the circuit board. The only breaks in this plane are for the circuits' necessary current paths.

The ground plane serves two functions. Because it's flat (ac currents travel along the surface of a conductor) and covers the entire area of the board, it provides access to a low-inductance ground point from anywhere on the board. Second, it minimizes the effects of stray capacitance in the circuit by referring the strays to ground. This stray neutralization breaks up unintended and harmful feedback paths. In short, *always use a ground plane with the LT1016.*

Effects of stray capacitance

The stray capacitance mentioned in the previous section can produce undesirable effects in comparator performance. Consider, for example, the fuzzy edges of the output waveform in **Fig 7a.** This condition appears similar to that of **Fig 6,** but the oscillation is more stubborn and persists well after the output switches low. The cause is stray capacitance from the comparator's outputs to its inputs. A 3-kΩ input-source impedance and 3-pF stray-capacitance feedback allowed this oscillation. The solution for this condition is not difficult: *Keep source impedances as low as possible (preferably ≤1 kΩ). Route output and input pins and components away from each other.*

As the operating speed of circuits increases, proper grounding becomes more important. It's crucial to minimize series inductance and resistance.

The opposite of stray-induced oscillations appears in **Fig 7b.** Here, the output response (trace B) badly lags the input (trace A). The lag arises from some combination of high source impedance and stray capacitance to ground at the input. The resulting RC network forces a lagging response at the input, resulting in an output delay. An RC combination of 2-kΩ source resistance and 5-pF capacitance to ground yields a 10-nsec time constant—the same as the LT1016's response time. Thus, *keep source impedances low and minimize stray capacitance from input to ground.*

Avoid heavy capacitive loading

Feedback and shunt strays are not the only capacitive offenders in a high-speed comparator's erratic operation. **Fig 8a** shows another capacitance-induced problem. Here, the output does not oscillate, but its transitions are discontinuous and relatively slow. The problem is a large output-load capacitance. Its genesis could be a cable, excessive output-lead length, or the input characteristics of the circuit following the LT1016. In most situations, heavy capacitive loading is undesirable; you can eliminate it by using a buffer stage. In a few circumstances, the loading might not affect overall circuit operation. *Consider the comparator's output-load characteristics and their potential effects on the circuit. If necessary, add a buffer between the output and the load.*

Another output-caused fault is shown in **Fig 8b.** The output transitions are initially clean but end in ringing. The key to the solution here is the ringing. The phenomenon arises because of an output lead that's too long. The lead, which appears as an unterminated transmission line at high frequencies, causes reflections. The transmission-line effect accounts for the ringing and the abrupt reversal of direction on the leading edge. When the comparator drives normal TTL circuits, the aberration might be acceptable; other loads, however, might not tolerate it. The direction reversal, for example, could cause trouble with a high-speed TTL load. The rule: *Keep output lead lengths short. When they're longer than a few inches, terminate the line with a resistor (typically between 200 and 500Ω).*

Another aspect of the LT1016's TTL outputs is that you must sometimes shift the levels of the output-voltage swing. In LT1016-based circuits, this task is not trivial; it's necessary to maintain very low delays in the

Beware of such stray-reactance problems as feedback or shunt capacitance and series inductance. Such unwanted circuit terms can cause ringing, oscillation, or worse.

level-shifting stage to obtain optimum performance. When you design level shifters, keep in mind that the comparator's output stage is a sink-source pair (**Fig 9a**) with a reasonable ability to drive capacitance (eg, feed-forward capacitors).

Fig 9b shows a noninverting voltage-gain stage with a 15V output. When the LT1016 switches, the 2N2369's base-emitter voltage reverses, causing the transistor to switch very rapidly. The 2N3866 emitter follower affords a low-impedance output; the Schottky diode aids the circuit's current-sinking capability. **Fig 9c** shows a very versatile stage. It offers a bipolar swing whose levels you can program by varying the output transistor's supplies.

The 3-nsec stage is ideal for driving FET-switch gates. Q_1, a gated current source, switches the Baker-clamped output transistor, Q_2. The heavy feed-forward capacitor from the LT1016 is the key to low delays; it provides Q_2's base with nearly ideal drive. This capacitor loads the LT1016's output (**Fig 9e,** trace A), but Q_2's switching is clean (trace B) and exhibits 3-nsec delay in its rising and falling edges.

The circuit in **Fig 9d** is similar to that in **Fig 9b,** except that a sink transistor replaces the Schottky diode. The two emitter followers drive a power MOSFET that switches 1A at 15V. Most of the 7- to 9-nsec delay in this stage occurs in the MOSFET and the 2N2369. *When designing level shifters, remember to use transistors with high switching speeds and high f_Ts.* To obtain results like the ones in these examples, you'll need switching times in the 2-nsec range and f_Ts approaching 1 GHz.

A final example of environment-induced maladies is shown in **Fig 10.** These waveforms are reminiscent of the input-RC-induced delay of **Fig 7b.** The output waveform initially responds to the input's leading edge,

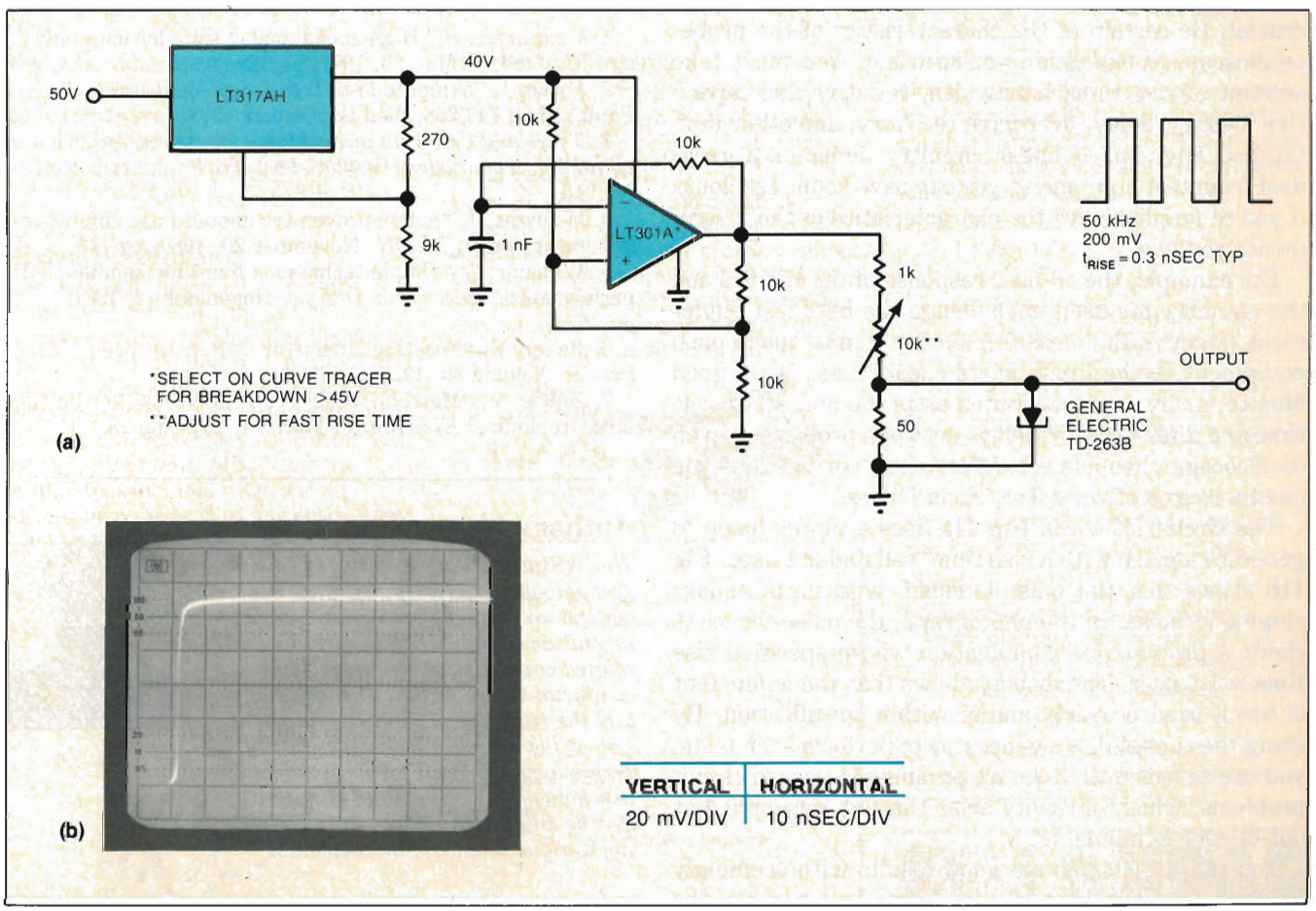


Fig 11—Be sure of your input pulses** when measuring the response of your equipment. The circuit in **a** uses a tunnel diode to generate very clean pulses with rise times much lower than 1 nsec **(b).

Respect a high-speed comparator's data sheet with regard to such parameters as common-mode input range and capacitive-load ability.

but then returns to zero before switching high again. When it does switch high, it slews slowly. Other odd characteristics include pronounced overshoot and pulse-top aberration. The fall time is also slow, and it's well delayed from the input. This behavior is certainly unusual for a TTL output.

All of these TTL-output anomalies are caused by the input pulse. Its 10V amplitude is well outside the 5V-powered LT1016's common-mode input range. Internal input clamps prevent such a pulse from damaging the comparator, but an overdrive of this magnitude invariably results in poor response. *Keep input signals within the LT1016's common-mode input range at all times.*

Verify equipment response

Although some of the examples described earlier dealt with probe-caused problems, oscilloscopes, too, can be troublesome. Your choice of oscilloscope is crucial. Be certain of the characteristics of the probe-oscilloscope combination you're using. You must take account of rise time, bandwidth, resistive and capacitive loading, delay, overdrive recovery, and other limitations. High-speed linear circuitry demands a great deal from test equipment; you can save countless hours if you're familiar with the characteristics of the instruments you use.

For example, the 10-nsec response of the LT1016 and the circuitry it's used in challenge the best test equipment. Many of the measurements you must make push equipment to the limits of its capabilities. It's a good idea to verify such attributes as probe and scope rise time and differences in delays between probes and even oscilloscope channels. To effect such verification, you need a source of very fast, clean pulses.

The circuit shown in **Fig 11a** uses a tunnel diode to generate a pulse with a rise time well under 1 nsec. **Fig 11b** shows that the pulse is clean, with no attendant ringing or noise. In the photograph, the pulse serves to check a probe-scope combination whose specified rise time is 1.4 nsec. The display shows that the equipment is being used properly and is within specification. By using the tunnel-diode generator to perform such tests, you can save countless hours pursuing supposed circuit problems, which in reality arise through misapplied or out-of-spec equipment.

You can, in fact, obtain good results with seemingly inadequate equipment if you know and respect the equipment's limitations. All the applications to appear in the two follow-on articles involve rise times and delays that correspond to frequencies that are greater than 100 or 200 MHz, but 90% of the development work was accomplished with a 50-MHz oscilloscope. Familiarity with equipment and thoughtful measurement techniques permit useful measurements that are seemingly beyond instrument capabilities.

A 50-MHz oscilloscope, for example, cannot track a 5-nsec rise-time pulse, but it can measure a 2-nsec delay between two such events. Using such techniques, you can often deduce the desired information. There are situations, though, where no amount of cleverness will work, and you must use the right equipment (eg, a faster oscilloscope). In general, *use equipment you trust and measurement techniques you understand. Keep asking questions and don't be satisfied until everything on the oscilloscope makes sense.* **EDN**

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Author's biography

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and -instrumentation design. He has served in related capacities at National Semiconductor Corp, Arthur D Little Inc, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. Jim is a former student of psychology at Wayne State University, and he enjoys tennis, art, and collecting antique scientific instruments.

Article Interest Quotient (Circle One)
High 473 Medium 474 Low 475

Fast comparator IC speeds converters and S/H amplifiers

This article, the second in a 3-part series, shows you how to use a fast comparator IC in V/F converters, A/D converters, sample-and-hold amplifiers, and track-and-hold amplifiers. The comparator realizes fast linear-circuit functions that are difficult or impossible to implement using previous techniques.

Jim Williams, *Linear Technology Corp*

The complementary, TTL-compatible outputs and the 10-nsec response time of the LT1016 comparator make the IC suitable for linear-circuit applications that demand high operating speeds. Once you have become familiar with the IC's basic attributes and some of the design precautions associated with its use, you can incorporate the comparator in a variety of circuits, from high-speed voltage/frequency (V/F) converters to sample-and-hold (S/H) and track-and-hold (T/H) circuits.

Part 1 of this series (EDN, June 13, 1985, pg 129) covered design guidelines for avoiding some of the problems associated with the high-speed circuitry that the LT1016 comparator would normally inhabit, as well as some essential precautions to take when performing tests on such circuitry. This article shows how you can exploit the full capabilities of the 10-nsec LT1016 comparator in applications requiring A/D and D/A conversion.

V/F converter is 10 times faster

Using the LT1016 comparator in combination with an LT1012 low-drift amplifier and support circuitry, you can build a V/F converter (**Fig 1a**) that delivers an output of 1 Hz to 10 MHz, with an overrange capability to 12 MHz (for an input of 12V). This dynamic range of seven decades (20 dB per decade for a total of 140 dB) is wider than that of any commercially available unit, and the 10-MHz full-scale frequency is 10 times faster than the upper limit of currently available monolithic V/F converters.

The main components of the converter are an integrating summing amplifier (Q_5, Q_6, IC_1, and C_2); a pulse generator (IC_2); a level-shifting charge dispenser (Q_1, Q_2, IC_5, and C_1); and supporting circuitry (IC_3 and IC_4) that stabilizes the summing integrator and prevents latch-up. Each time the circuit produces an output pulse, it feeds back a fixed quantity of charge (Q) to the summing node (Σ), where the resulting current is summed with the current provided by the input signal.

A high-speed comparator helps realize a V/F converter with a 7-decade dynamic range and a 10-MHz full-scale frequency.

The difference signal (integrated in capacitor C_2) that appears at the output of IC_1 causes the pulse generator to run at a frequency that pumps enough charge to offset the input signal and maintain the summing node at zero. Consequently, the circuit satisfies the equation $Q=CV$ such that the output frequency is linearly related to the input voltage.

Op amp reduces offset drift

For low-bias, high-speed operation, the monolithic input circuitry of IC_1 is turned off by connecting both input pins to the −15V rail. A pair of discrete FETs (Q_5 and Q_6) directly drives the output stages of IC_1. To reduce offset drift to 0.2 μV/°C, IC_3 (a precision op amp) measures the offset voltage at the inverting input (summing node) of the FET/IC combination, compares this offset to ground, and forces the noninverting input to maintain offset balance in the FET/IC combination. Note that IC_3 is configured as an integrator and responds only to dc and low-frequency signals.

When a positive voltage is applied to the input terminal, the output of IC_1 integrates in a negative direction (**Fig 1b,** trace A). During the formation of this ramp, the inverting output of IC_2 is low. A very-high-speed level shifter (see Part 1 of this series) consisting of Q_1 and Q_2 inverts the output of IC_2 and drives the zener reference bridge (IC_5). The positive output of this bridge charges C_1 to the value $V_Z+V_{BE(Q3)}$. The 1.2V diode string (D_1 and D_2) provides cancellation and temperature compensation for the diode drops in IC_5.

When the output of IC_1 crosses the zero level, the inverting output of IC_2 goes high and the collector of Q_2 (trace B) goes to −5V, thereby causing C_1 to dispense charge into the summing node via the base-emitter junction of Q_4. The amount of charge dispensed is a direct function of the voltage to which C_1 was charged during the integration cycle ($Q=CV$). The drop across the base-emitter junction of Q_4 compensates the $V_{BE(Q3)}$ term in the capacitor's charge equation. The current that flows through C_1 (trace C) reflects this charge-pumping action.

The removal of charge from the summing node causes the node to be driven negative very quickly (trace D). The 20-nsec negative-going transient at the bottom of the ramp (trace A) is a result of amplifier delay; the input signal feeds directly through C_1 and appears at the output terminal of IC_1. When the amplifier responds, its slew rate delays the process of regaining control of the summing node. The length of time during which Q_2's collector remains at −5V (trace B) depends upon how long it takes IC_1 to recover and upon the 5-pF/100Ω hysteresis network (R_3C_3) attached to IC_2. This time amounts to 60 nsec—sufficient for a complete discharge of C_1. At the end of this period, IC_2 changes state, Q_2's collector swings positive, and C_1 begins recharging to repeat the entire cycle.

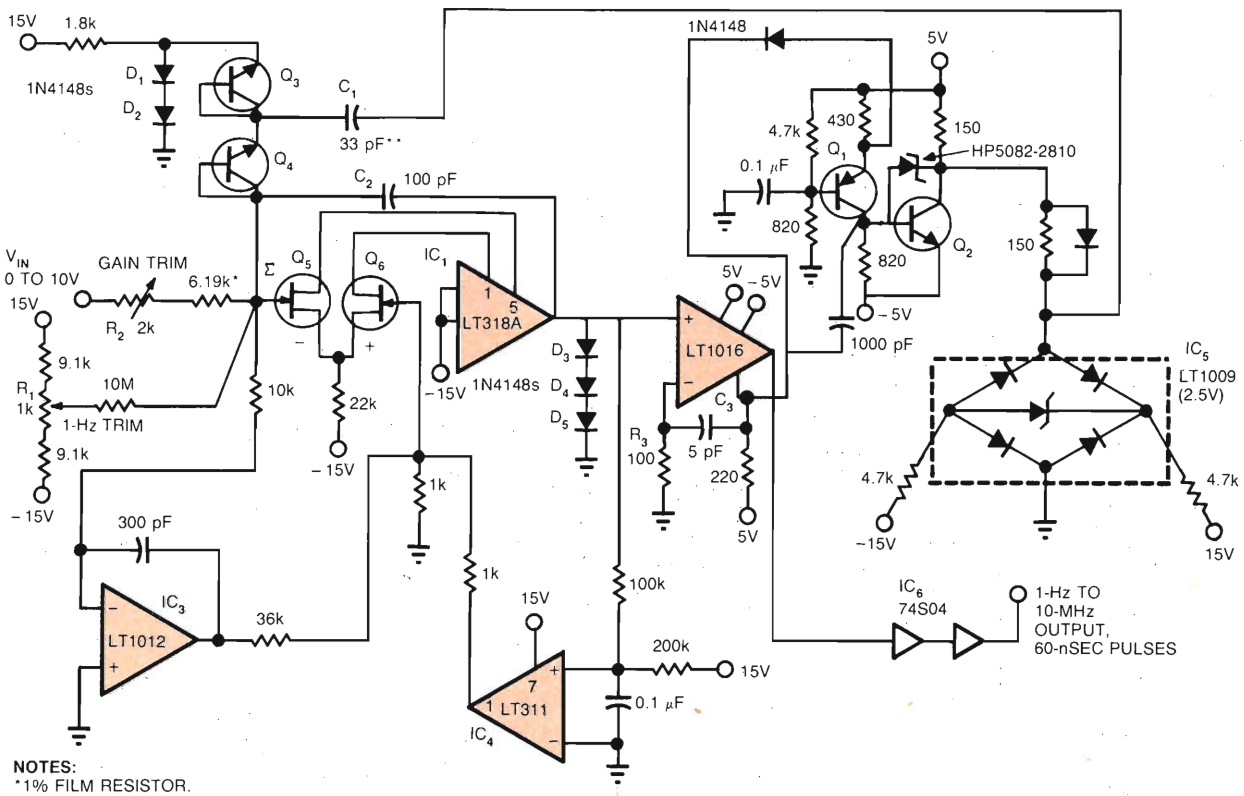
The frequency at which oscillation occurs is directly related to the current delivered by the voltage input to the summing node. Any given input current will require a corresponding oscillation frequency to hold the summing node at an average value of 0V. Maintaining the linearity of this relationship at megahertz frequencies places severe restrictions on circuit timing. The key to obtaining a full-scale operating frequency as high as 10 MHz is the ability to transmit information through the loop as quickly as possible. The discharge/reset sequence is particularly critical. An expanded view of this sequence is shown in **Fig 1c.**

Trace A represents the integrator's output; its falling ramp crosses the zero level at the first vertical graticule line (extreme left). A few nanoseconds later, the inverting output of IC_2 (trace B) begins to rise, driving the level shifter's output positive (trace C). Approximately 12 nsec after the integrator ramp crosses the zero level, Q_2's collector begins to swing negative. The summing node (trace D) begins to go negative 4 nsec later, as current is drawn from it through C_1. At the 25-nsec mark, the inverting output of IC_2 is fully positive, the collector of Q_2 is at −5V, and the summing node has been pulled to its negative extreme. At this point, IC_1 begins to take control; its output (trace A) begins to slew rapidly in the positive direction, restoring the summing point. At the 60-nsec mark, IC_1 is fully in control of the summing node and the integration ramp begins again.

Beware of latching conditions

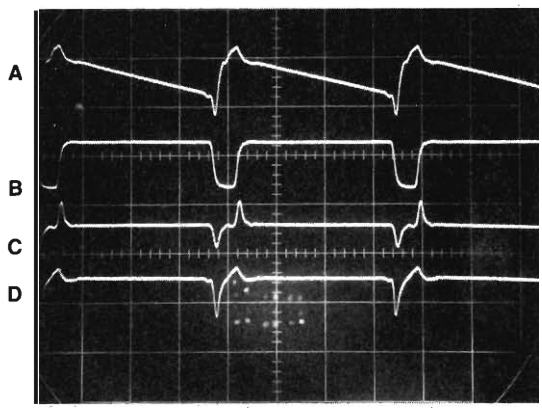
Start-up and overdrive conditions could force the output of IC_1 to go to the level of the negative rail and stay there, in which case the ac nature of the charge-dispensing loop would preclude normal operation and the circuit would latch. IC_4 provides a watchdog function to guard against latch-up. If the output of IC_1 falls too far below 0V, the output of IC_4 switches, forcing the input of FET Q_6 positive. This action in turn forces the output of IC_1 to slew in the positive direction to initiate normal operation. The diode chain (D_3 to D_5) prevents common-mode overdrive of IC_2. The two 74S04 inverters provide double buffering of the circuit's output.

To trim the V/F converter, first ground the input



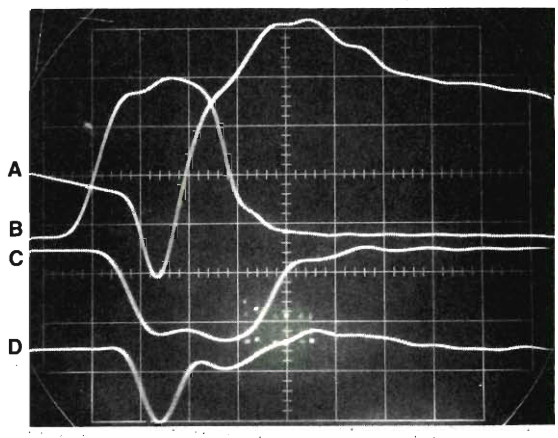
NOTES:
*1% FILM RESISTOR.
**POLYSTYRENE.
Q_3 AND Q_4 ARE 2N2369s.
Q_5 AND Q_6 ARE 2N4393s.
GROUND LATCH PIN OF IC_2.

(a)



TRACE	VERTICAL	HORIZONTAL
A	1V/DIV	100 nSEC/DIV
B	10V/DIV	100 nSEC/DIV
C	20 mA/DIV	100 nSEC/DIV
D	1V/DIV	100 nSEC/DIV

(b)



TRACE	VERTICAL	HORIZONTAL
A	0.2V/DIV (UNCALIBRATED)	10 nSEC/DIV
B	1V/DIV	10 nSEC/DIV
C	5V/DIV	10 nSEC/DIV
D	0.5V/DIV	10 nSEC/DIV

(c)

Fig 1—This wide-range V/F converter uses an integrator, *level shifter, and fast comparator* ***(a).*** *Transfer linearity is 0.06% over the full range from 1 Hz (0V input) to 10 MHz (10V input). Operation of the V/F converter* ***(b)*** *depends on the precise dispensing of charge through a capacitor. An expanded view of the critical discharge/reset sequence is shown in* ***c.***

Maintaining the linearity of the 10-MHz V/F converter at megahertz frequencies places severe restrictions on circuit timing.

terminal and adjust potentiometer R_1 for a 1-Hz output. Then remove the ground, apply 10V to the input terminal, and adjust potentiometer R_2 for an output of 10 MHz. The transfer linearity is 0.06%, full-scale drift is typically 50 ppm/°C, and the zero-point drift is approximately 0.2 μV/°C (0.2 Hz/°C).

Delays in the active elements included in the feedback path around the LT1016 determine the upper frequency limit of the V/F-converter circuit. The circuit shown in **Fig 2a** extends the frequency limit to 30 MHz by minimizing these delays while applying the appropriate corrections to retain good linearity and drift characteristics.

The components within the dashed line perform the V/F conversion in a manner similar to that of **Fig 1**'s circuit, except for the elimination of the level shifter and zener. Transistor Q_1 charges the 200-pF capacitor (C_1); the buffer consisting of transistors Q_2 and Q_3 unloads C_1. When the voltage at the inverting input of the LT1016 (IC_1) exceeds the voltage at the noninverting input, the output goes low, pulling charge out of C_1 via transistor Q_4 (which acts as a low-leakage diode). The 2.7-pF capacitor (C_2) connected from the output to the noninverting input of the LT1016 provides positive feedback, and the LT1016 oscillates at a frequency in the 1-Hz to 30-MHz range. The exact frequency depends upon the input voltage present.

Adjust for drift and linearity

Although this simple circuit is fast, its linearity is poor and drift exceeds 5000 ppm/°C. To correct these deficiencies without sacrificing speed, you have to add a quartz-locked, sampled-data loop that counts the number of pulses emitted by the LT1016 during a fixed interval, converts this information to an analog voltage, and compares this voltage to the signal input. This loop technique relies upon the stability of the time interval and the D/A conversion to achieve circuit stability. Frequent updating of the loop ensures long-term stability.

Traces A, B, and C in **Fig 2b** are the inverting input, output, and noninverting input, respectively, of the LT1016. Their similarity to the corresponding traces in **Fig 1c** reflects the similar operation of the two circuits. Trace D shows the crystal-controlled, 4-kHz clock pulse. During the low portion of the pulse, the gated output of the LT1016 appears at the output of IC_4 (trace E) and increments the counter chain consisting of IC_9 to IC_{11}. When the clock goes high, one section of the 74123 one-shot (IC_5) generates a pulse (trace F) that loads the 7475 latches (IC_6 to IC_8) with the number accumulated in the counters. The falling edge of this pulse triggers the second section of the 74123 to generate a pulse (trace G) that resets the counters to zero. At the next falling edge of the 4-kHz clock, the entire cycle repeats.

Loop resolution sets frequency smoothly

The D/A converter (IC_3) and the associated output amplifier (IC_{4A}) provide a voltage representation of the digital word contained in the 7475 latches. Amplifier IC_{4B} compares this voltage to the input signal, and the amplifier output drives the V/F converter. The feedback action of the stabilizing loop through the D/A converter corrects for any drift or nonlinearity produced by the V/F converter.

Although it's not obvious, the frequency-setting resolution of the loop is much greater than you'd expect the 12-bit quantization limit of the D/A converter to permit, because the converter's output signal behaves as if it were the output of a 4-kHz clocked-pulse-width modulator. The time constants of the loop integrate the modulated signal to a pure dc level, affording smooth, continuous frequency-setting capability. The practical limit on resolution depends upon the short-term frequency jitter of the LT1016; it's approximately 25 ppm of the reading.

Although this approach allows higher speeds than that of the 10-MHz V/F converter, there are some tradeoffs. The sampling action of the loop and the relatively long time constants limit the settling time of the circuit to approximately 100 msec min. Consequently, the 30-MHz circuit cannot trace rapidly varying inputs. Linearity is limited to 0.025% by D/A-converter characteristics, with a full-scale drift of 50 ppm/°C. The zero-point drift of 1 Hz/°C arises from the 0.3-μV/°C offset drift of IC_{4B}.

Fast 12-bit A/D converter

Turning now to a different application, you can use the high speed of the LT1016 to implement a very fast 12-bit A/D converter. The circuit **(Fig 3a)** uses a modified form of the successive-approximation technique, in which the 2504 successive-approximation register (SAR, IC_4), amplifier IC_2, and comparator IC_3 test each bit, beginning with the most significant, and produce a digital word representing the value of the input signal V_{IN}.

Because the 6012 D/A-converter chip (IC_1) is segmented and has a significantly shorter settling time for the lower nine bits than for the upper three bits, you

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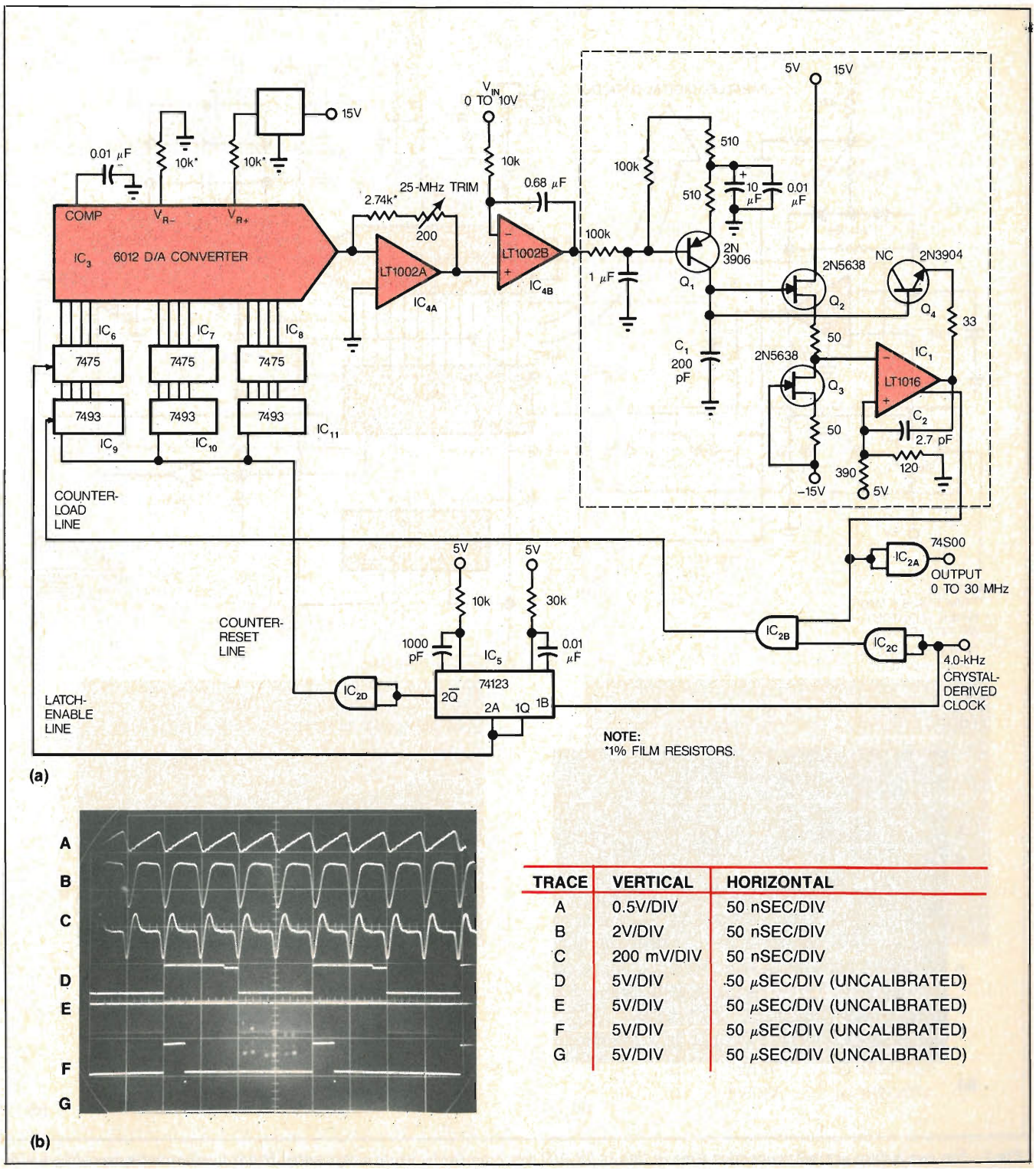
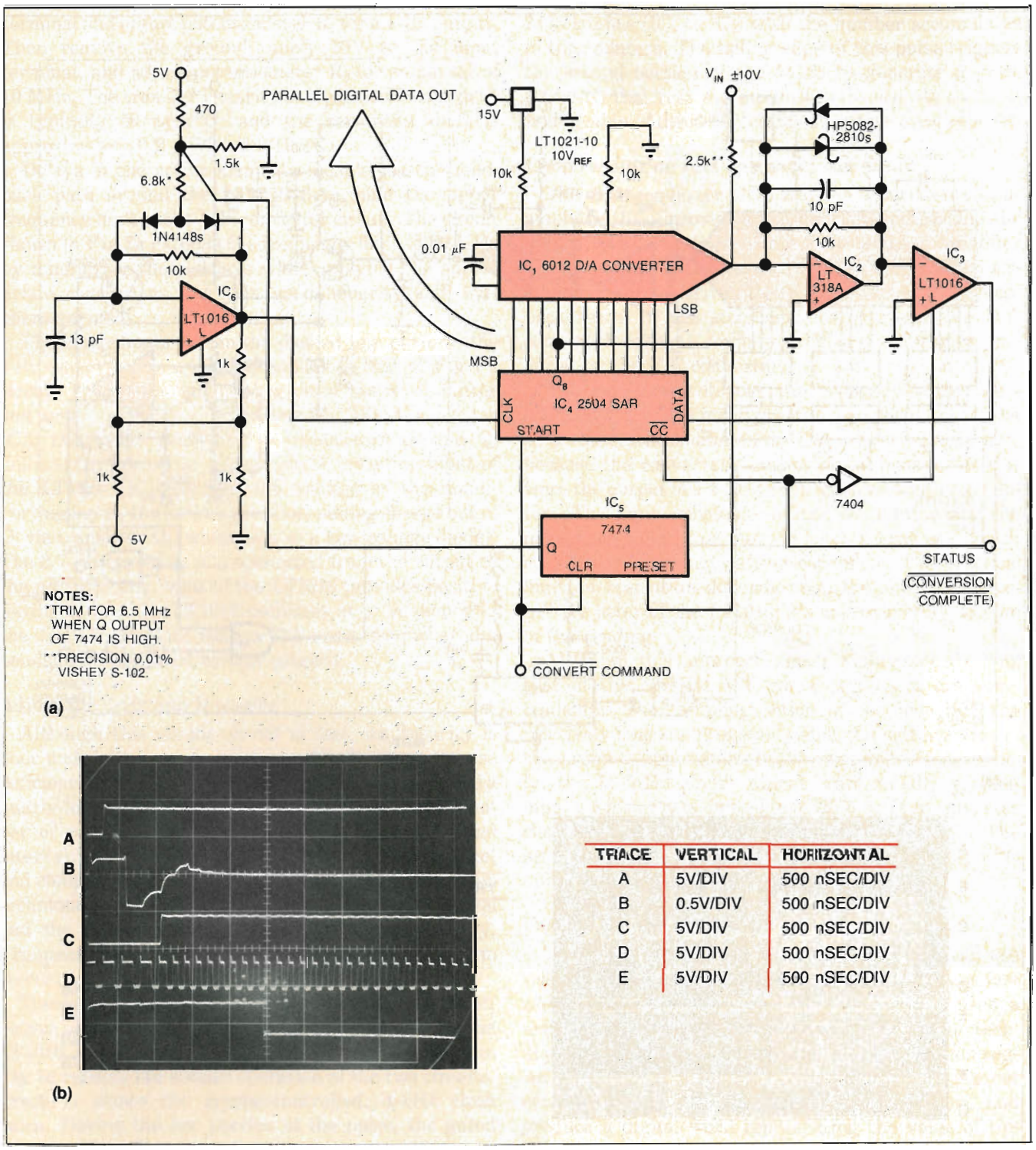


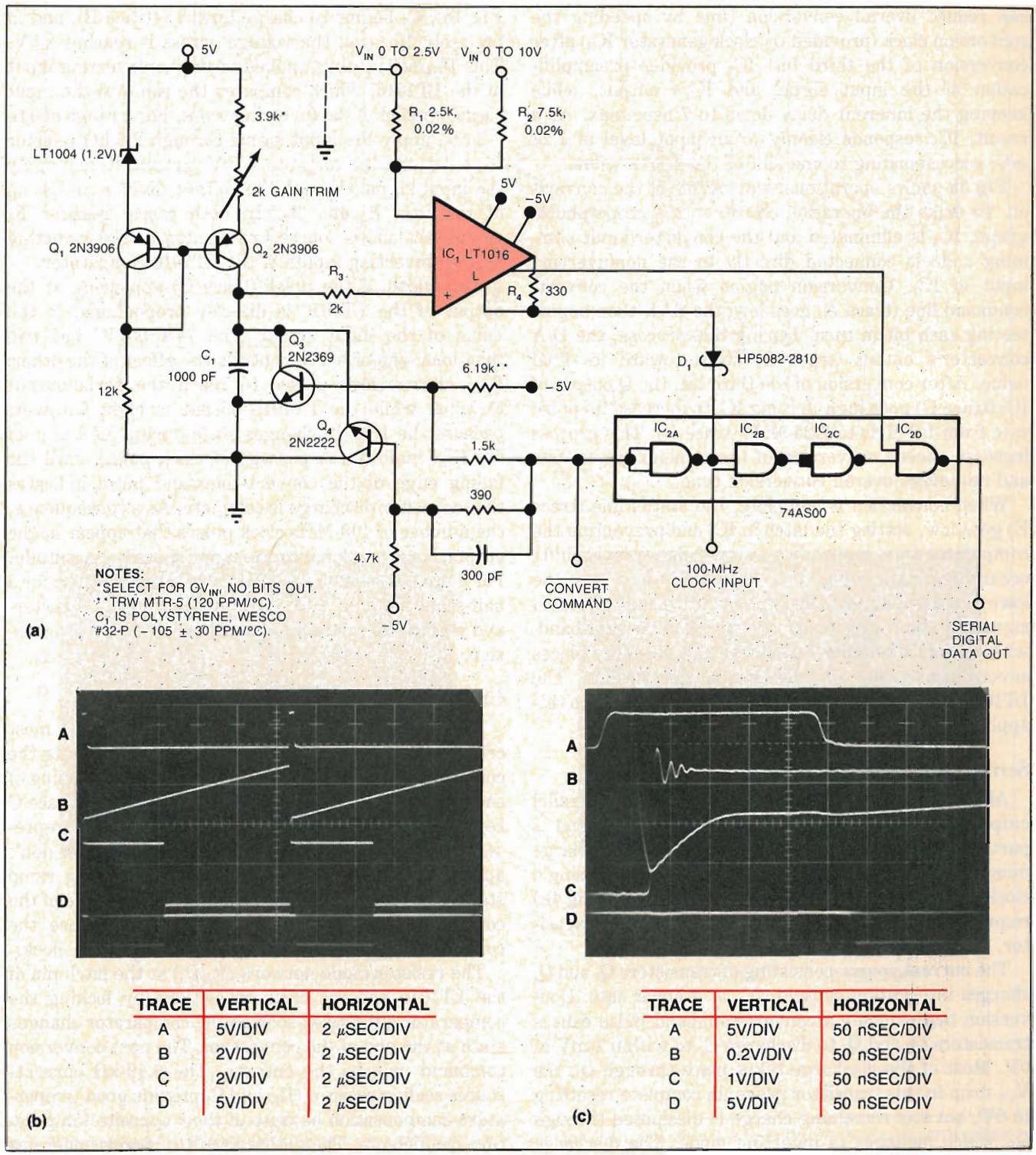
TRACE	VERTICAL	HORIZONTAL
A	0.5V/DIV	50 nSEC/DIV
B	2V/DIV	50 nSEC/DIV
C	200 mV/DIV	50 nSEC/DIV
D	5V/DIV	50 μSEC/DIV (UNCALIBRATED)
E	5V/DIV	50 μSEC/DIV (UNCALIBRATED)
F	5V/DIV	50 μSEC/DIV (UNCALIBRATED)
G	5V/DIV	50 μSEC/DIV (UNCALIBRATED)

Fig 2—This V/F converter (a) counts pulses generated *during a fixed interval. Deficiencies of the simplified converter are corrected with the aid of a D/A converter. The waveforms* ***(b)*** *show operational similarities between this circuit and that shown in* ***Fig 1a.***



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	500 nSEC/DIV
B	0.5V/DIV	500 nSEC/DIV
C	5V/DIV	500 nSEC/DIV
D	5V/DIV	500 nSEC/DIV
E	5V/DIV	500 nSEC/DIV

Fig 3—You can reduce overall conversion time *in this 12-bit A/D converter* ***(a)*** *by using a segmented D/A converter and by speeding up the clock after conversion of the three most significant bits is complete. Trace D* ***(b)*** *shows the clock rate accelerating from 4.2 MHz to 6.5 MHz after conversion of the first three bits.*



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	2 μSEC/DIV
B	2V/DIV	2 μSEC/DIV
C	2V/DIV	2 μSEC/DIV
D	5V/DIV	2 μSEC/DIV

TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	50 nSEC/DIV
B	0.2V/DIV	50 nSEC/DIV
C	1V/DIV	50 nSEC/DIV
D	5V/DIV	50 nSEC/DIV

Fig 4—You can use a serial A/D converter (a) *for applications in which a single clock serves many converters. Trace D* ***(b)*** *shows the gated 100-MHz pulse output of the serial converter. Trace A is the convert-command pulse. An expanded view of the critical region* ***(c)*** *shows the discharge of the capacitor (trace B). Gated output pulses (trace D) don't appear until linear charging of the capacitor begins.*

You can extend the V/F converter's frequency limit to 30 MHz by minimizing delays. Appropriate corrections can help retain good linearity and drift.

can reduce overall conversion time by speeding the conversion clock (provided by clock generator IC_6) after conversion of the third bit. IC_2 provides preamplification of the input signal and IC_1's output, while keeping the inherent delay down to 7 nsec max. As a result, IC_3 responds cleanly to an input level of 1.22 mV, corresponding to one-half of the LSB's value.

Fig 3b shows operational waveforms of the converter. To make the operation clearer in the scope photograph, IC_2 is eliminated and the converter/input summing node is connected directly to the noninverting input of IC_3. Conversion begins when the convert-command line (trace A) goes low; the SAR then begins testing each bit in turn. During this process, the D/A converter's output (trace B) steps toward its final value. After conversion of the third bit, the Q output of IC_5 (trace C) goes high, forcing IC_6 to increase its pulse rate from 4.2 MHz to 6.25 MHz (trace D). This process increase speeds conversion of the remaining nine bits and minimizes overall conversion time.

When conversion is complete, the status line (trace E) goes low, setting the latch in IC_3 and preventing the comparator from responding to any noise or level shifts occurring on the input line. During conversion of the lowest order bits, IC_3 must respond to millivolt-level signals without sacrificing speed; the high gain-bandwidth product required to achieve this response places severe constraints on the comparator design. The LT1016 is one of the very few comparators suited to this application.

Serial A/D converter needs few parts

Although most A/D converters generate a parallel output word, a serial converter is inexpensive and is particularly suited to applications that use a large number of converters that can all be served by a single clock generator. A simple serial A/D converter (**Fig 4a**) requires only a current source, an integrating capacitor, a comparator, and some gates.

The current source consisting of transistors Q_1 and Q_2 charges integrating capacitor C_1 at a linear rate. Conversion begins when a convert-command pulse causes transistors Q_3 and Q_4 to discharge C_1 to within 1 mV of 0V. Most of the discharge takes place through Q_1; the V_{CE} drop in this transistor prevents complete resetting to 0V, but any remaining charge is dissipated through Q_4, which switches in inverting mode. The discharge process takes 200 nsec, which is therefore the minimum acceptable width of the convert-command pulse.

On the falling edge of the command pulse (trace A, **Fig 4b**), C_1 begins to charge linearly (trace B), and in precisely 10 μsec, the voltage across it reaches 2.5V. This 10-μsec ramp is applied to the noninverting input of the LT1016, which compares the ramp to the input signal applied to the inverting input. For a range of 0 to −2.5V, apply the input signal through 2.5-kΩ resistor R_1; to extend the range to −10V, ground R_1 and apply the input signal through the voltage divider consisting of resistors R_2 and R_1. In both cases, resistor R_3 ensures balanced source impedances at the inverting and noninverting inputs of the LT1016 comparator.

The width of the pulse (trace C) appearing at the output of the LT1016 is directly proportional to the value of the input signal. The 74AS00 IC has two functions, one of which controls the effect of the other: IC_{2D} allows clock pulses to reach the serial-output terminal while the LT1016 output is high; however, because the LT1016 changes state during discharge of C_1, IC_{2A} inhibits the passage of clock pulses until the falling edge of the convert-command pulse indicates that capacitor discharge is complete. As a consequence, the number of 100-MHz clock pulses that appear at the output is proportional to the input signal's magnitude. For a full-scale input of −10V, 1024 pulses appear; for a half-scale input of −5V, 512 pulses appear. Quarter- and eighth-scale inputs, etc, follow the same progression.

Charging ramp initiates output pulses

Fig 4c furnishes an expanded view of the most critical part of the operation. Trace A represents the convert-command pulse. Trace B shows the resetting of the C_1 and the beginning of the charging ramp. Trace C represents the comparator's output. Trace D represents the gated serial output. Observe that pulses don't appear at the serial output until the charging ramp starts (just past midscreen, after the falling edge of the command pulse). Trace D shows jitter because the conversion command is not synchronized to the clock.

The resistor/diode network (R_4/D_1) at the latch pin of the LT1016 ensures clean transitions by locking the comparator outputs as soon as the comparator changes state at the end of the conversion. The next conversion command unlocks the outputs. The 6.19-kΩ current-source scaling resistor (R_5) and C_1 provide good temperature compensation because of their opposite temperature coefficients. The entire circuit typically maintains accuracy to ±1 LSB over the temperature range 0 to 70°F, with an additional uncertainty of ±1 LSB caused by the asynchronous relationship between the clock and

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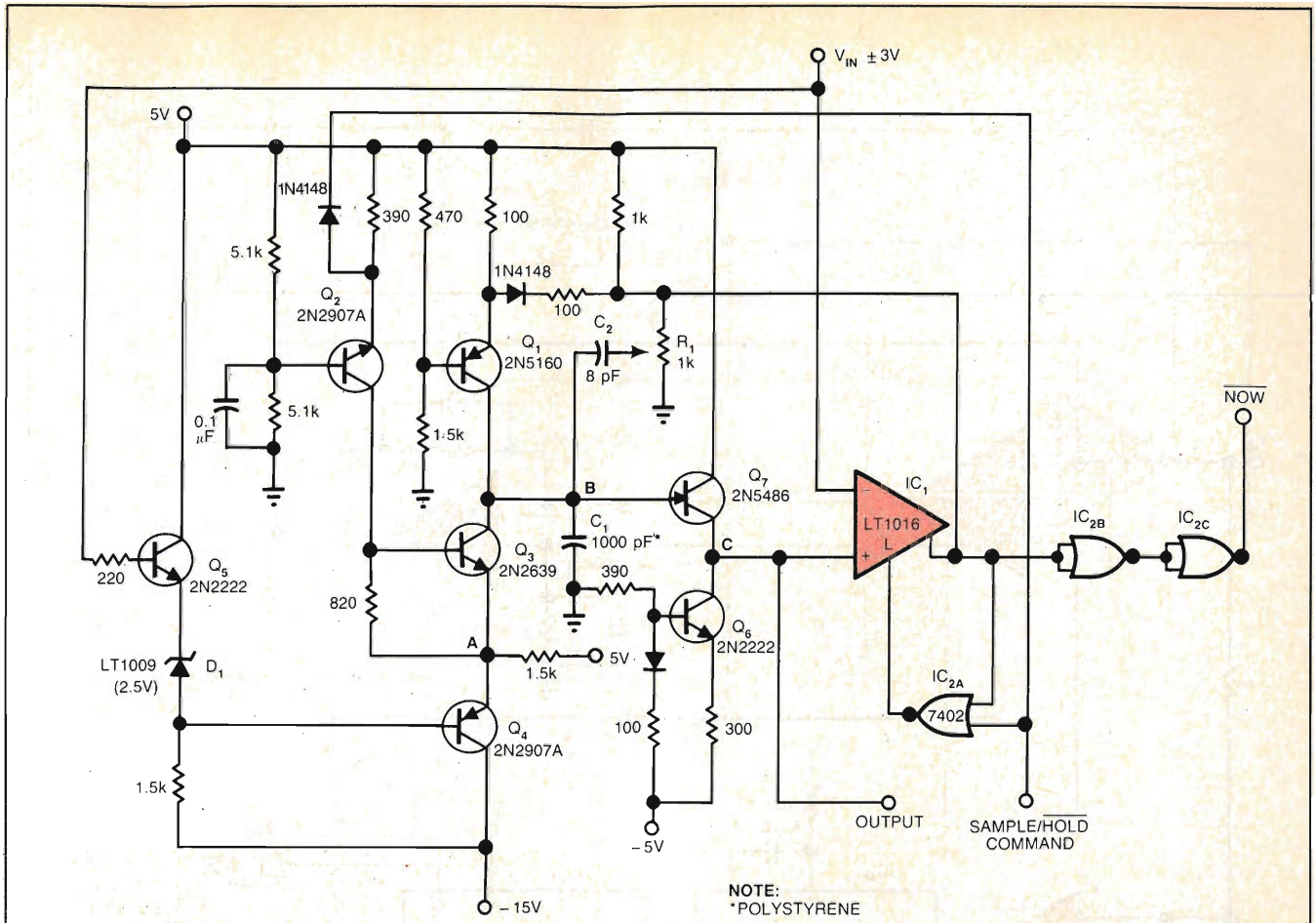
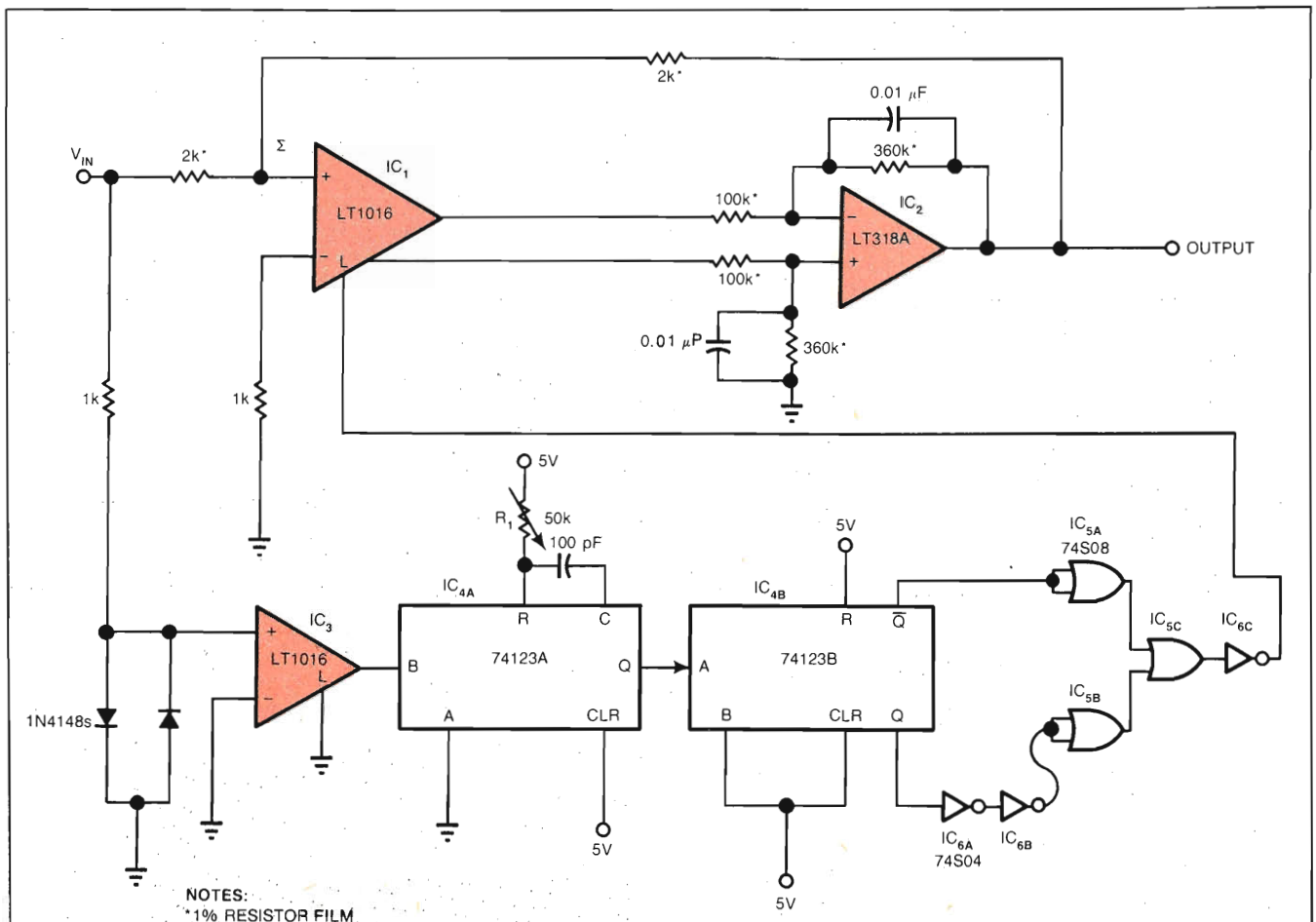
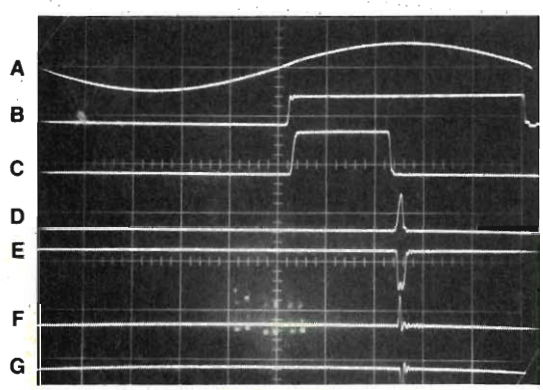


TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	500 nSEC/DIV
B	1V/DIV	500 nSEC/DIV
C	5V/DIV	500 nSEC/DIV
D	5V/DIV	20 nSEC/DIV
E	10 mV/DIV	20 nSEC/DIV
F	2 mA/DIV	20 nSEC/DIV
G	2V/DIV	20 nSEC/DIV

TRACE	VERTICAL	HORIZONTAL
A	2V/DIV	50 µSEC/DIV
B	2V/DIV	50 µSEC/DIV
C	1V/DIV	10 µSEC/DIV

Fig 5—This fast sample-and-hold circuit (a) *specs an acquisition time of less than 200 nsec. Internal delays allow the hold capacitor's voltage to exceed the input, but compensation brings the output to the correct value. Expanded traces E, F, and G* ***(b)*** *clarify sampling compensation. Trace E shows the charging ramp overshooting; trace F shows removal of surplus charge through the compensating network. Expanded trace C in* ***c*** *shows details of the sampling steps while the circuit samples a triangular wave. Trace A is the input signal; trace B is the sampled output signal on the same scale.*

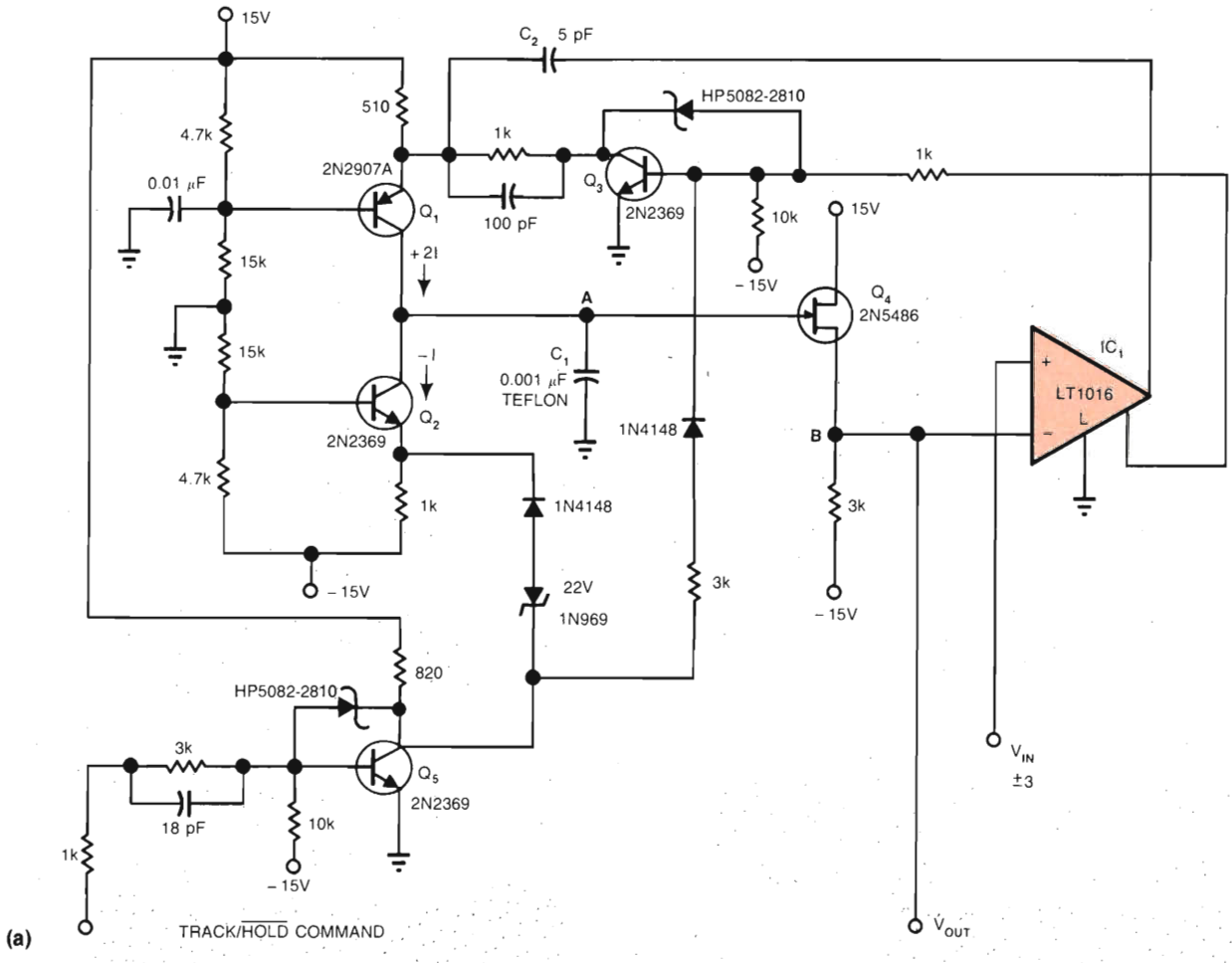




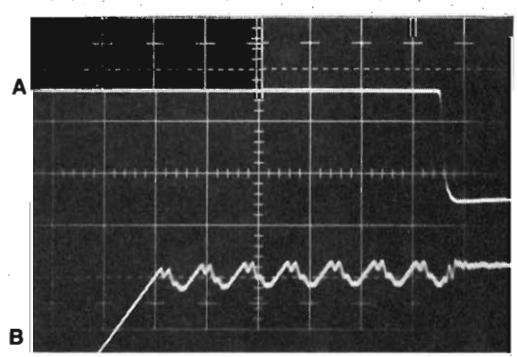
(b)

TRACE	VERTICAL	HORIZONTAL
A	20V/DIV	100 nSEC/DIV
B	5V/DIV	100 nSEC/DIV
C	5V/DIV	100 nSEC/DIV
D	5V/DIV	100 nSEC/DIV
E	5V/DIV	100 nSEC/DIV
F	5V/DIV	100 nSEC/DIV
G	5V/DIV	100 nSEC/DIV

Fig 6—You can cut sampling time to 10 nsec *when using this sample-and-hold circuit* ***(a)*** *to sample repetitive signals. The 10-nsec window can be positioned at any point on the input waveform. One-shots generate a delay period (trace C in* ***b****) and 30-nsec spikes (traces D and E), which are combined to form a 10-nsec spike (trace G) that performs the sampling.*

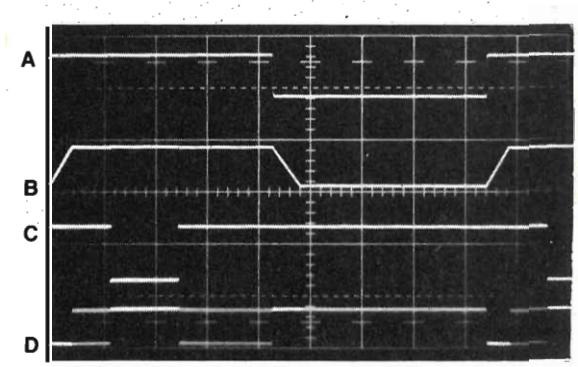


(a)



TRACE	VERTICAL	HORIZONTAL
A	2V/DIV	50 nSEC/DIV
B	20 mV/DIV	50 nSEC/DIV

(b)



TRACE	VERTICAL	HORIZONTAL
A	2V/DIV	10 μSEC/DIV
B	2V/DIV	10 μSEC/DIV
C	5V/DIV	10 μSEC/DIV
D	5V/DIV	10 μSEC/DIV

(c)

Fig 7—This track-and-hold circuit (a) tracks an input signal *within ±5 mV for 8-bit accuracy. The circuit has a settling time of less than 10 nsec. Trace B* ***(b)*** *shows output oscillation around the input level, with clean cutoff on return to hold mode. Trace B in* ***c*** *shows the circuit tracking a square wave (trace A). Note that comparator oscillation (trace D) stops cleanly when the track/hold line (trace C) goes low.*

The 30-MHz V/F converter achieves its high speed with a price. Circuit features limit the circuit's settling time to a minimum of approximately 100 msec.

the conversion sequence.

The high speed of the LT1016 comparator recommends its use in a fast S/H circuit like the one shown in **Fig 5a.** This circuit achieves an acquisition time of 200 nsec—well beyond the capability of monolithic S/H devices and matched only by hybrid and modular units in the $200 price range. The circuit also avoids FET switching errors, excessive amplifier settling times, and other problems associated with standard S/H design techniques.

Transistors Q_4 and Q_5 and diode D_1 form a wideband tracking amplifier that maintains point A at a potential that's always a fixed amount below the potential of the input terminal. When the sample command line (**Fig 5b,** trace A) goes high, transistor Q_2 conducts, thereby turning on transistor Q_3 and forcing capacitor C_1 to discharge (trace B) toward the potential of point A. Concurrently, the sample command enables the LT1016 by grounding the latch pin via TTL OR gate IC_{2A}. At that point, the inverting output (trace C) goes high. On the trailing edge of the sample command pulse, Q_2 and Q_3 turn off and current-source transistor Q_1 rapidly and linearly charges C_1.

The potential at point B is transferred to the noninverting input of the comparator through high-speed source follower Q_7, which is loaded by current-source transistor Q_6. When point C reaches the same potential as that of the input signal, the comparator changes state and its inverting output (trace C) goes low, thereby turning off Q_1 within approximately 2 nsec so that it ceases to charge C_1. The low state of the comparator output drives the latch pin high via IC_{2A} so that level changes and line noise on the input line cannot affect the potential stored in C_1.

Delays yield higher potential

Ideally, point C and the output terminal would now be at exactly the potential of the sampled input voltage. In practice, the turnoff time of Q_1 and delays in the comparator (amounting to 12 nsec) allow C_1 to charge to a potential slightly higher than that of the input. This error is compensated by removing a small quantity of charge from C_1, via delay-compensation capacitor C_2 and potentiometer R_1, when the comparator output goes low. Because the slope of the charging ramp is fixed, the error term is constant and the compensation, once adjusted, works over the entire input range of −3 to +3V.

Traces D through G are expanded to show the compensating action. When the comparator output (trace D) goes low, the charging ramp (trace E) slightly overshoots its final value. However, the discharge through the compensating network (trace F) is just enough to bring the ramp back to the correct value. Trace G represents the state of the $\overline{\text{Now}}$ line, which goes low two gate-delay time periods after the comparator delivers its output. At the end of this delay, the output line has settled after the correction transient and provides valid data. The total time from the falling edge of the sample command to the falling edge of the $\overline{\text{Now}}$ signal is never more than 200 nsec.

TABLE 1 — S/H CIRCUIT SPECIFICATIONS

ACQUISITION TIME	<200 nSEC
COMMON-MODE INPUT RANGE	±3V
DROOP	1 μV/μSEC
HOLD STEP (COMPENSATION OUT)	100 μV
HOLD STEP (COMPENSATION IN)	2 mV
HOLD SETTLING TIME	15 nSEC
FEEDTHROUGH REJECTION	>>100 dB
OUTPUT NOISE (IN HOLD)	3 nV/ √Hz AT 1 Hz

Fig 5c shows sampling of a bipolar, triangular waveform. Trace A represents the input signal and trace B the circuit output. Trace C, an expansion of trace B, shows slight smearing of the sampled pedestals because of the repetitive, asynchronous sampling of the triangle.

To calibrate the S/H circuit, ground the input line, repetitively pulse the sample-command line, and adjust compensation potentiometer R_1 to obtain 0V on the output line. After calibration, the circuit should meet the specifications listed in **Table 1.**

Cut sample time to 10 nsec

An even faster S/H circuit, which cuts acquisition time to 10 nsec, is shown in **Fig 6a.** You can use this circuit only with repetitive signals, however. An LT1016 comparator (IC_1) drives a differential integrator (IC_2) and accepts feedback from the integrator's output to the summing node. **Fig 6b** shows the action of the circuit when a 1-MHz sine wave (trace A) is applied to the input. A second LT1016 (IC_3) generates a zero-crossing signal (trace B), and one-shot IC_{4A} provides an adjustable delay (trace C) starting at the zero crossing.

At the end of the delay period, the Q output of one-shot IC_{4B} generates a 30-nsec pulse (trace D), which is fed into the logic network consisting of IC_5 and IC_6 along with the inverted signal from the $\overline{Q}$ output (trace

A fast 12-bit A/D converter incorporating the LT1016 uses a modified form of the successive-approximation technique.

F). At the end of the timing period, the $\overline{Q}$ output goes high and the Q output goes low. However, because of the gate delays in IC_{6A} and IC_{6B}, both inputs of IC_{5C} are high for a period of 10 nsec.

The resulting spike that appears at the output of IC_{5C} (trace F) is inverted and enables the latch of IC_1. Each time the spike occurs, IC_1 responds to the condition of the summing junction. After a number of input cycles, the output of IC_2 settles at a dc value that's the same as the level sampled during the period the comparator's latch is enabled. Delay-adjusting potentiometer R_1 allows positioning the 10-nsec sampling window at any point on the input sine wave.

Fast track-and-hold circuit

The last example of the use of the LT1016 in sampling and conversion applications is the fast T/H circuit shown in **Fig 7a.** The main functional elements are a switched current source (transistors Q_1 and Q_3); a current-sink (transistor Q_2); a FET source follower (Q_4); and the LT1016 comparator (IC_1).

To understand circuit operation, assume that the potential at point A is initially below that of the input terminal, and that the track/$\overline{\text{hold}}$ command line (**Fig 7b,** trace A) is at a logic-one TTL level (track mode). Under these conditions, Q_5 conducts, the noninverting output of IC_1 is positive, and the inverting output is low, thereby turning off Q_3 and allowing Q_1 to conduct. At this time, Q_2 is also operating, but at only half the current density of Q_1; the net effect, therefore, is to charge capacitor C_1 in a positive direction.

When the potential at point B reaches the value of the input signal, IC_1's outputs reverse their states. Q_3 turns on, thereby rapidly turning off Q_1; the turn-off is speeded by the action of capacitor C_2, which bypasses Q_3. Now, with the current source turned off, C_1 begins to discharge through Q_2 until the potential at point B falls below the input potential, at which point IC_1 changes state again. This process repeats at a 25-MHz rate, producing a controlled oscillation (trace B), 10 mV in amplitude, centered on the value of the input signal.

When the track/$\overline{\text{hold}}$ command line goes low (hold mode), Q_5 turns off, thereby turning off both Q_1 and Q_2. Oscillation ceases and the output terminal is maintained by Q_4 at a potential that corresponds to that of the input signal within ±5 mV. This 5-mV uncertainty, inherent in the circuit, limits accuracy to eight bits.

Fig 7c shows the action of the circuit when a square wave (trace A) is applied to the input terminal. Trace B represents the output signal, trace C the track/$\overline{\text{hold}}$ command signal, and trace D the comparator's output. Observe that oscillation stops cleanly when the track/$\overline{\text{hold}}$ line goes low. The circuit's parameters reflect a compromise between speed and accuracy: If the source and sink currents were to be increased, the output line would slew much more rapidly to keep up with changes in the input-signal level. However, the uncertainty of the output level, caused by the oscillating nature of the circuit, would also be proportionately increased. The component values specified in the schematic allow a 25-MHz update rate, which is adequate to track a relatively slow input signal within ±5 mV. Settling time is less than 10 nsec after switching to hold mode.

EDN

Author's biography

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in the design of analog circuits and instruments. He has served in related capacities at National Semiconductor Corp, Arthur D Little Inc, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. Jim is a former student of psychology at Wayne State University, and he enjoys tennis, art, and collecting antique scientific instruments.

Article Interest Quotient (Circle One)
High 479 Medium 480 Low 481

Fast comparator IC speeds VCOs and other circuits

This last part of a 3-part series describes how the fast LT1016 comparator improves the operation of a voltage-controlled sine-wave oscillator, an ac voltmeter, a fiber-optic receiver, a fast circuit breaker, and a counter. The speed of the comparator lets you run these circuits at higher frequencies than previously possible, and with less worry about distorting delays, accuracy, stability, and potential damage to associated parts.

Jim Williams, *Linear Technology Corp*

The LT1016 comparator sports complementary, TTL-compatible outputs and a 10-nsec response time, which can improve the performance of a variety of circuits. Mastery of a few design precautions (**Ref 1**) prepares you for designing the comparator into such circuits as V/F converters, A/D converters, sample-and-hold amplifiers, and track-and-hold amplifiers, as described in Part 2 of this series (**Ref 2**). This last installment describes a few more designs: a voltage-controlled sine-wave oscillator, an ac voltmeter, a fiber-optic receiver, a fast circuit breaker for semiconductor calibration, and a stable trigger circuit for a counter.

The V/F converters described in Part 2 have an output consisting of narrow pulses well suited to forming the input to counters and other digital equipment. However, there are many applications that require a voltage-controlled oscillator (VCO) with a sine-wave output. Such applications include audio test equipment and shaker tables for subjecting equipment to vibration tests.

Fig 1a shows a voltage-controlled sine-wave oscillator circuit with a frequency range of 1 Hz to 1 MHz for inputs of 0 to 10V. Voltage/frequency linearity is 0.25% over the whole range, and distortion is no more than 0.4%.

The principal functional elements of the circuit are a summing integrator (IC_2); a precision op amp (IC_4); a current source (Q_1) and a current sink (Q_2 and Q_3); a level shifter (Q_4 and Q_5); the LT1016 comparator (IC_3); and a wave shaper (IC_5 and IC_6).

Cycle generates triangular waveform

To understand the basic operation of the circuit, assume that Q_5 is conducting, and that its collector is at −15V (**Fig 1b**, trace A), thereby turning off Q_1. IC_1 inverts the positive control signal (V_{IN}) and then pulls a current (−I) from the summing node of integrator IC_2 through self-biased FETs Q_2 and Q_3 and resistor R_1. IC_4 provides dc stabilization of IC_2. IC_2's output (trace B) rises linearly until the noninverting input of IC_3 (trace C) crosses the 0V level. At that time, IC_3 changes state and its inverting output goes negative, thereby turning

The LT1016 suits many applications that require a voltage-controlled oscillator with a sine-wave output.

off Q_4 and Q_5. As a consequence, Q_5's collector goes to 15V and turns on Q_1.

Resistors R_2 and R_3 are scaled to produce a current (+2I), flowing into the summing node, that's exactly twice the absolute magnitude of the current flowing out of the node. The net current into the node thus becomes +I, and IC_2's output moves in a positive direction at exactly the same rate as it formerly moved in the negative direction. The positive movement continues until IC_3's input again crosses the 0V level, causing IC_3 to change state and thereby turn off Q_1 via the level shifter. The entire cycle then repeats, generating a triangular waveform at the output of IC_2. The repetition rate of this triangular wave is directly proportional to the magnitude of dc control signal V_{IN}.

The LT1009 diode bridge and diodes D_3 through D_6 provide a stable bipolar reference voltage, the polarity of which is always opposite to that of IC_3's output ramp. Schottky diodes D_1 and D_2 limit the signal appearing at the noninverting input of IC_3, thereby ensuring that the comparator recovers cleanly from any overdrive at IC_2's output.

Short delays minimize distortion

Trigonometric function generator IC_6, biased by op amp IC_5, converts the triangular wave appearing at the integrator's output to a sine wave. Distortion results, however, if the triangular wave's amplitude is not held constant. Possible causes of distortion are delays in the integrator's switching loop, which result in late turn-on and turn-off of Q_1, and gate-source transfer effects in Q_1. If turn-on/turn-off delays become excessive, triangle amplitude increases with frequency, so that sine-wave distortion also increases with frequency. Uncompensated gate-source transfer effects produce spikes at the upper and lower triangle peaks. These spikes also cause distortion.

The very high speed of the LT1016 comparator, together with careful design of the level shifter and the circuitry around Q_1, holds the total delay generated in the comparator, level shifter, and Q_1 down to 14 nsec. The feed-forward network consisting of capacitor C_3 and resistor R_4 also helps to minimize loop delays. Gate-source transfer effects in Q_1 are compensated by capacitor C_1. In addition, FETs Q_2 and Q_3 compensate the temperature-dependent on-resistance of Q_1 to maintain the +2I/−I relationship despite temperature variations. As the result of these precautionary measures, sine-wave distortion is no more than 0.4% over the entire frequency range of 1 Hz to 1 MHz, and at 200 kHz, it's typically less than 0.2%.

To calibrate the circuit, first apply a 10V input signal and adjust high-frequency symmetry potentiometer R_3 for a symmetrical triangular waveform at the output of IC_2 (the frequency should be approximately 1 MHz). Next, reduce the input signal to 100 μV and adjust low-frequency symmetry potentiometer R_5 for triangle symmetry. Then increase the input to 10V again and adjust frequency-trim potentiometer R_8 for an output frequency of 1 MHz. Finally, connect a distortion analyzer to the sine-wave output terminal of IC_6 and adjust distortion-trim potentiometers R_6 and R_7 for minimum distortion (trace E). Slight readjustment of the symmetry controls may also be necessary in order to achieve the best results over the whole frequency range. Don't forget to reduce the input signal to 100 μV when readjusting R_5 and to increase the input to 10V when readjusting R_3.

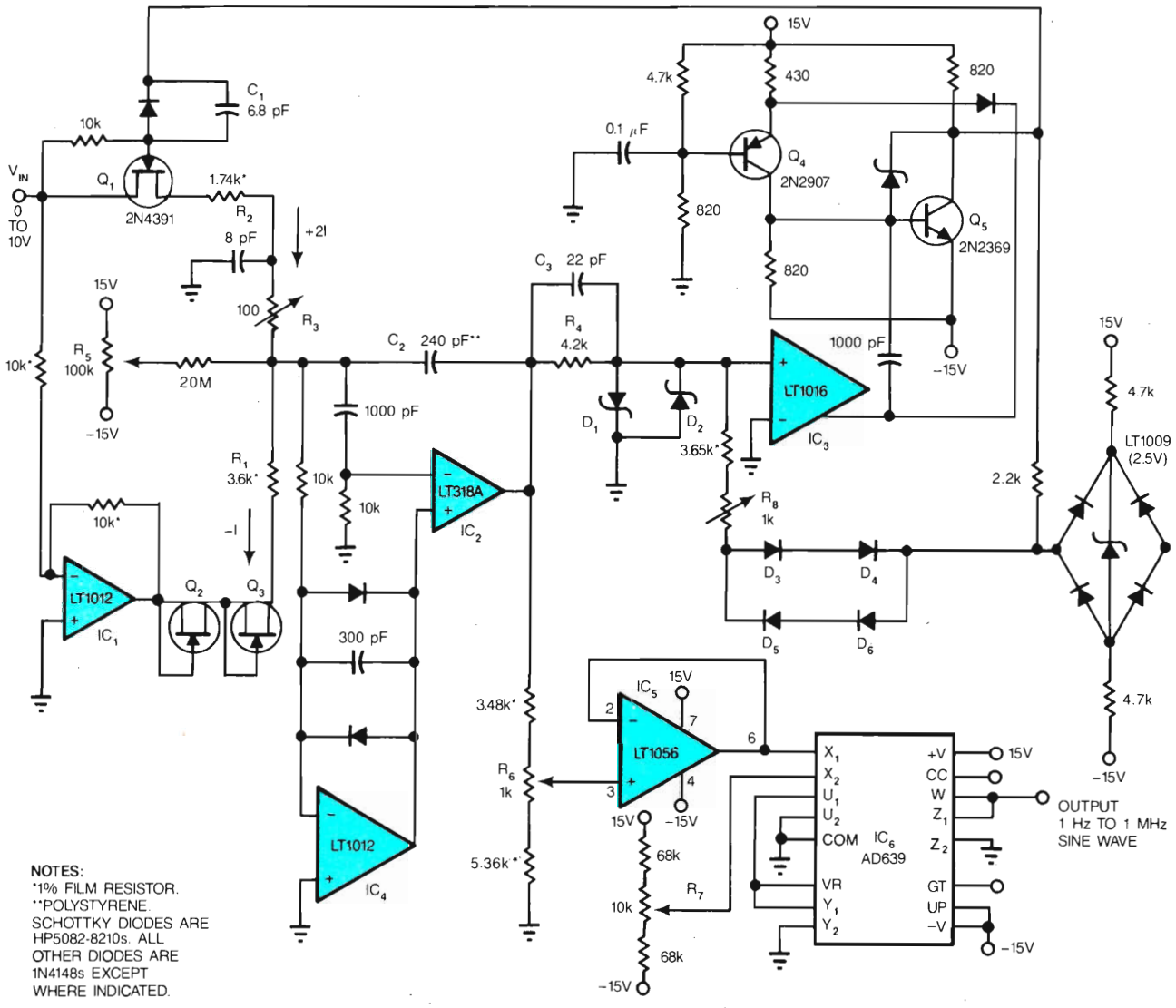
High-frequency precision voltmeter

The attributes of the LT1016 comparator inspire a new approach to the design of ac voltmeters. Previous precision-rectifier circuits relied on op amps to correct for voltage drops in the signal-rectifier diodes. Although that technique is satisfactory at low frequencies, bandwidth limitations in the op amps usually restrict the operation of such circuits to frequencies below 100 kHz. You can, however, use the LT1016 in the open-loop, synchronous rectifier configuration of **Fig 2a** to achieve high accuracy at frequencies as high as 2.5 MHz.

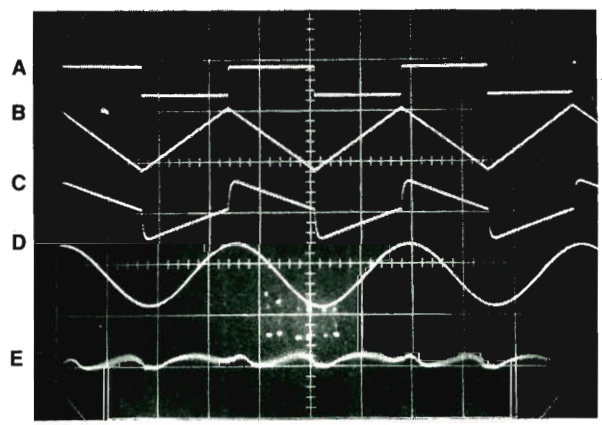
The main functional components of the circuit are a zero-crossing detector (IC_1); two level shifters with bipolar ±5V outputs and propagation delays of only 2 to 3 nsec; a Schottky-diode switching bridge (diodes D_1 through D_4); and a precision dc amplifier (IC_2).

The LT1016 (IC_1) changes state each time the input signal crosses the 0V level. Its complementary outputs drive the two level shifters that bias the switching bridge. Traces B and C (**Fig 2b**) show the switching voltages at points B and C, respectively, of the bridge. The input signal is applied to point A of the bridge. Because the comparator switches the bridge in synchrony with the input signal, a half-wave rectified sine wave appears at point D (trace D). IC_2 and the associated components generate a dc level corresponding to the true-rms value of the input signal.

The fast switching characteristic of the Schottky-diode bridge eliminates charge-pumping effects that would be present if a FET switch were used. Trace E,



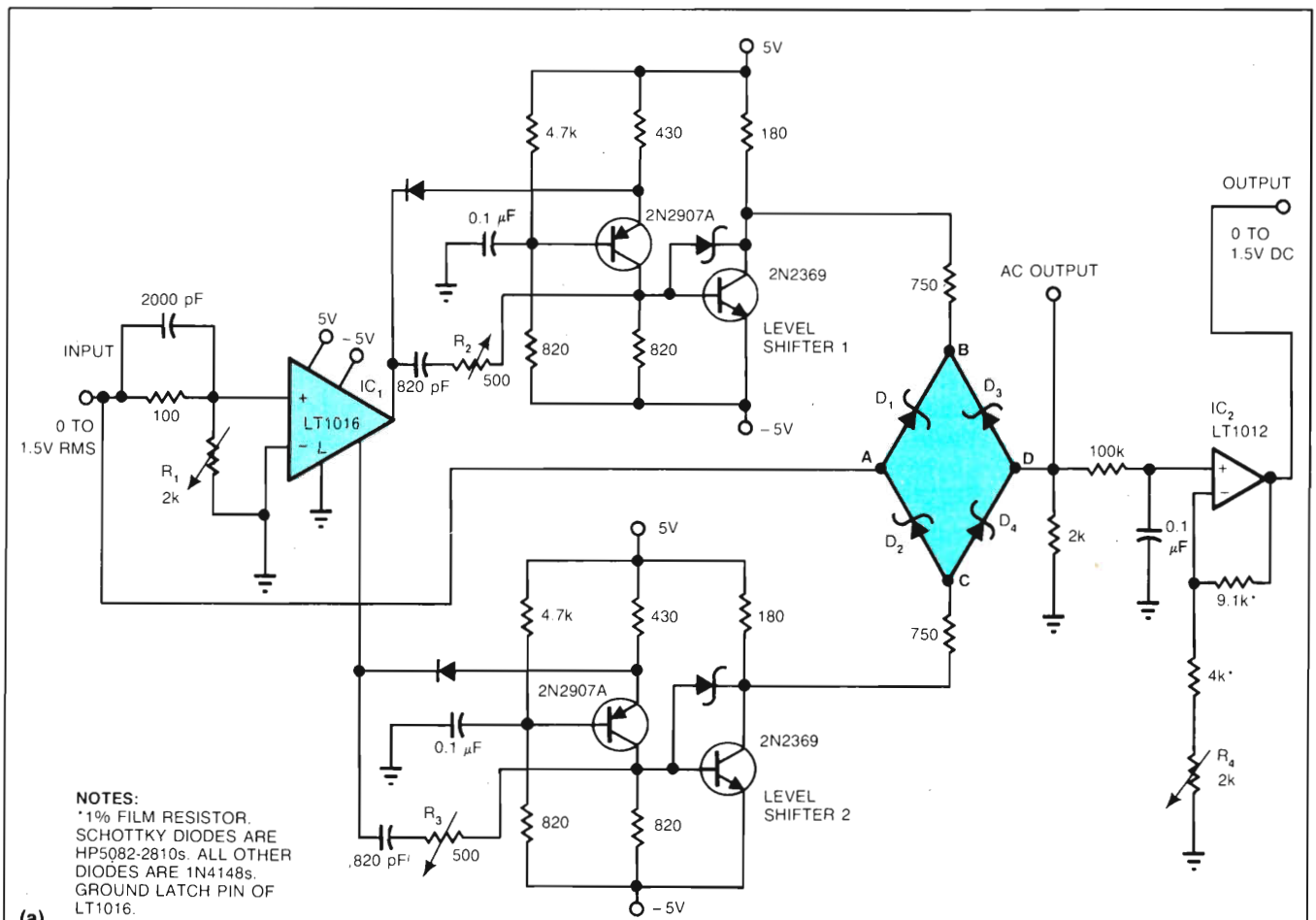
(a)

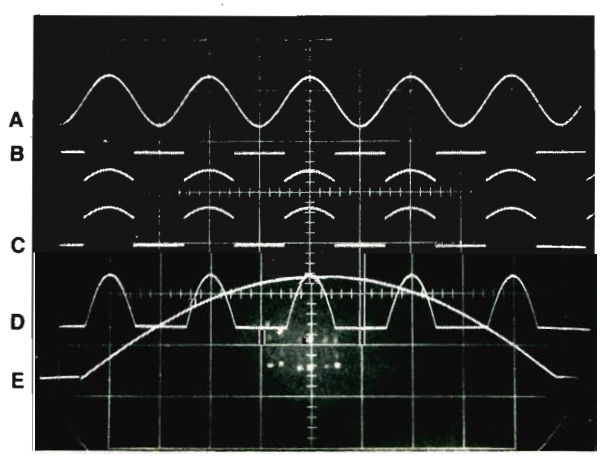


(b)

TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	500 nSEC/DIV
B	10V/DIV	500 nSEC/DIV
C	10V/DIV	500 nSEC/DIV
D	2V/DIV	500 nSEC/DIV
E	1V/DIV	50 nSEC/DIV (UNCALIBRATED)

Fig 1—You can use this sine-wave oscillator (a) *in applications requiring frequencies between 1 Hz and 1 MHz. You minimize sine-wave distortion (trace E in* ***b****) by maintaining the symmetry of the triangular waveform at the output of the integrator.*





(b)

TRACE	VERTICAL	HORIZONTAL
A	50V/DIV	500 nSEC/DIV
B	5V/DIV	500 nSEC/DIV
C	1V/DIV	500 nSEC/DIV
D	5V/DIV	500 nSEC/DIV
E	0.5V/DIV	500 nSEC/DIV

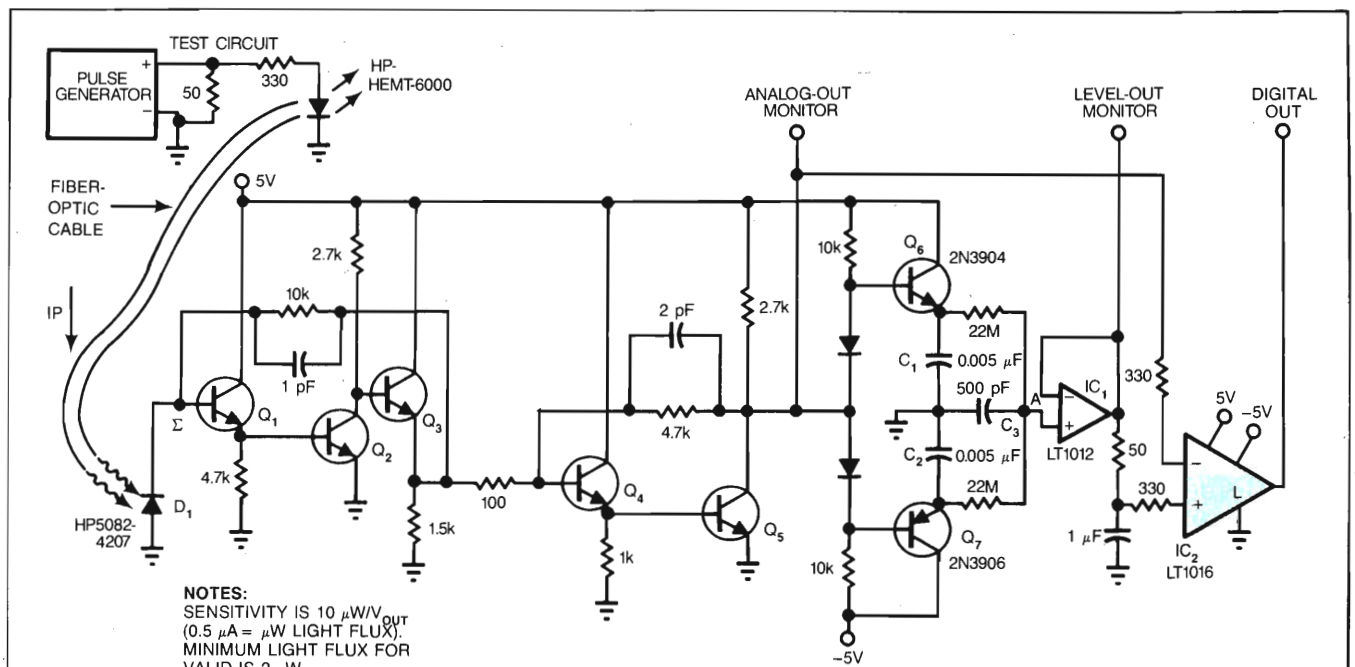
Fig 2—A fast comparator switches the diode bridge *at 0V crossings in this ac-voltmeter circuit* ***(a),*** *and thereby provides accurate rectification of the input signal. Clean switching signals (traces B and C in* ***b****) result in minimal disturbances in the rectified output (traces D and E). Trace A is the input; trace E is an expansion of the half-wave-rectified output.*

In the VCO circuit, the comparator helps hold sine-wave distortion to 0.4% over the 1-Hz to 1-MHz frequency range.

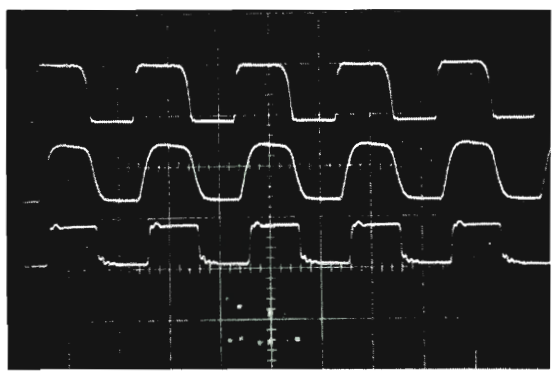
which is an expansion of trace D, shows that the waveform at the bridge is clean, with the exception of very small disturbances at the points where bridge switching occurs.

To calibrate the rectifier circuit, apply a sine-wave input signal with a frequency of 1 to 2 MHz and an amplitude of 1V p-p. First, connect an oscilloscope to points B and C and adjust delay-compensation potentiometer R_1 so that bridge switching occurs when the sine wave crosses the 0V level. This adjustment compensates for the small delays (11 to 12 nsec) contributed by the comparator and level shifters.

Next, adjust skew-trim potentiometers R_2 and R_3 for minimum aberration in the ac output signal at point C. Each of these potentiometers slightly shifts the phase of the output's rising edge from the associated level shifter. Optimum adjustment of the potentiometers keeps skew between the complementary switching sig-



(a)



(b)

TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	50 nSEC/DIV
B	2V/DIV (INVERTED)	50 nSEC/DIV
C	5V/DIV	50 nSEC/DIV

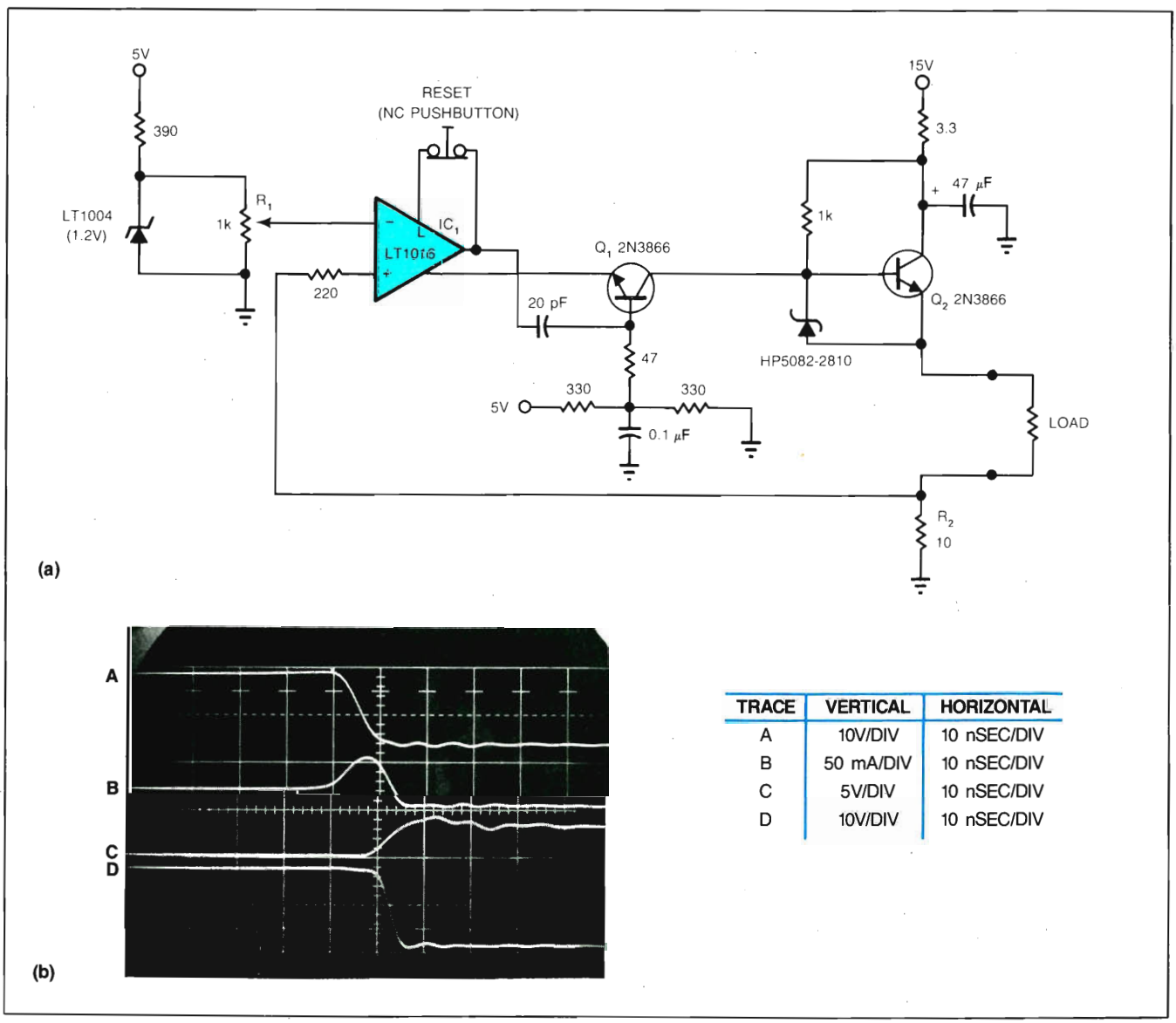
***Fig 3—This circuit (a) uses an adaptive threshold trigger** and the LT1016 to digitize fiber-optic signals at varying light levels and data rates as high as 10 MHz. Comparator transitions (trace C in **b**) line up with the midpoints of the analog-signal edges (trace B). Trace A is the test signal, monitored prior to transmission over the fiber-optic cable.*

The LT1016 surpasses the performance of op amps when used in ac voltmeters. The comparator achieves high accuracy at frequencies as high as 2.5 MHz.

nals to less than 2 nsec, thereby minimizing output disturbances caused by the switching operation. Finally, adjust gain potentiometer R_4 to obtain a dc output corresponding to the rms value of the input signal. When the circuit is correctly adjusted, a 100-mV sine-wave input will produce a clean output with a dc accuracy of better than 0.25% at frequencies as high as 2.5 MHz.

High data rates, and the light-level uncertainties resulting from the aging of components and other causes, present severe problems in the design of fiber-optic data receivers. The fiber-optic receiver circuit of **Fig 3a** features an adaptive threshold trigger that accommodates widely varying light intensities. The LT1016 accepts the adapted threshold as a switching threshold and enables operation at data rates as high as 10 MHz.

Two broadband amplifiers with feedback, one consisting of transistors Q_1 through Q_3, the other of transistors Q_4 and Q_5, amplify the signal detected by photodi-



TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	10 nSEC/DIV
B	50 mA/DIV	10 nSEC/DIV
C	5V/DIV	10 nSEC/DIV
D	10V/DIV	10 nSEC/DIV

Fig 4—The LT1016 comparator is the heart of this circuit breaker (a), *which features an adjustable current threshold. When load current (trace B in* ***b****) is forced past the current threshold, the comparator's output (trace C) reverses state, turning off Q_2 (trace D) within 12 nsec of the start of the overload condition.*

An adaptive threshold trigger handles varying light intensities in a fiber-optic receiver.

ode D_1. The amplified analog output appearing at Q_5's collector is applied to an output connector for monitoring purposes, to a bipolar peak-detector consisting of Q_6 and Q_7, and to the inverting input of the LT1016 (IC_2). The minimum potential of the amplified signal appears at Q_7's emitter and is stored in capacitor C_2; the maximum peak value of the signal appears at Q_6's emitter and is stored in capacitor C_1.

Combining these values through resistors R_1 and R_2 causes point A to assume a potential that's midway between the excursions of the signal, regardless of absolute amplitude. This signal-adaptive voltage, buffered by low-bias, unity-gain amplifier IC_1, sets the threshold level at the noninverting input of IC_2, and the amplified signal is applied to the inverting input. As a consequence, IC_2 will change state whenever the signal crosses the midpoint between the minimum and maximum signal levels, averaged over previous cycles.

Fig 3b shows waveforms representing the circuit's operation. Trace A is the output of a pulse generator set up for test purposes. This signal is applied to the receiver via the fiber-optic cable. Trace B represents the amplified analog output of the receiver, monitored at Q_5's collector. The broadband amplifier responds within 5 nsec, and its output reaches peak value within 25 nsec. Trace C is the digital output of the receiver, monitored at the output of the LT1016 comparator. **Fig 3b** shows that comparator transitions line up with the midpoints of the rising and falling edges of trace B, thus verifying the operation of the adaptive trigger circuit.

In the development and test phases of semiconductor design, calibration procedures or the introduction of probes can produce unexpected conditions or cause accidental short circuits that damage or destroy expensive components. The speed of the LT1016 comparator can be used to advantage in the construction of a circuit breaker (**Fig 4a**) that's three times faster and much less complex than its predecessors. The fast circuit breaker completes its function before an overload can cause damage.

Current-set potentiometer R_1 sets the comparator's threshold by applying a known portion of the reference voltage to the inverting input of the LT1016 (IC_1). The noninverting input is driven by the voltage drop across sensing resistor R_2, which is in series with the load. Under normal conditions, the voltage drop across R_2 is less than the threshold potential. The inverting output of IC_1 is high, shutting off Q_1 and thereby allowing Q_2 to supply current to the load.

When an overload occurs (in this case indicated by

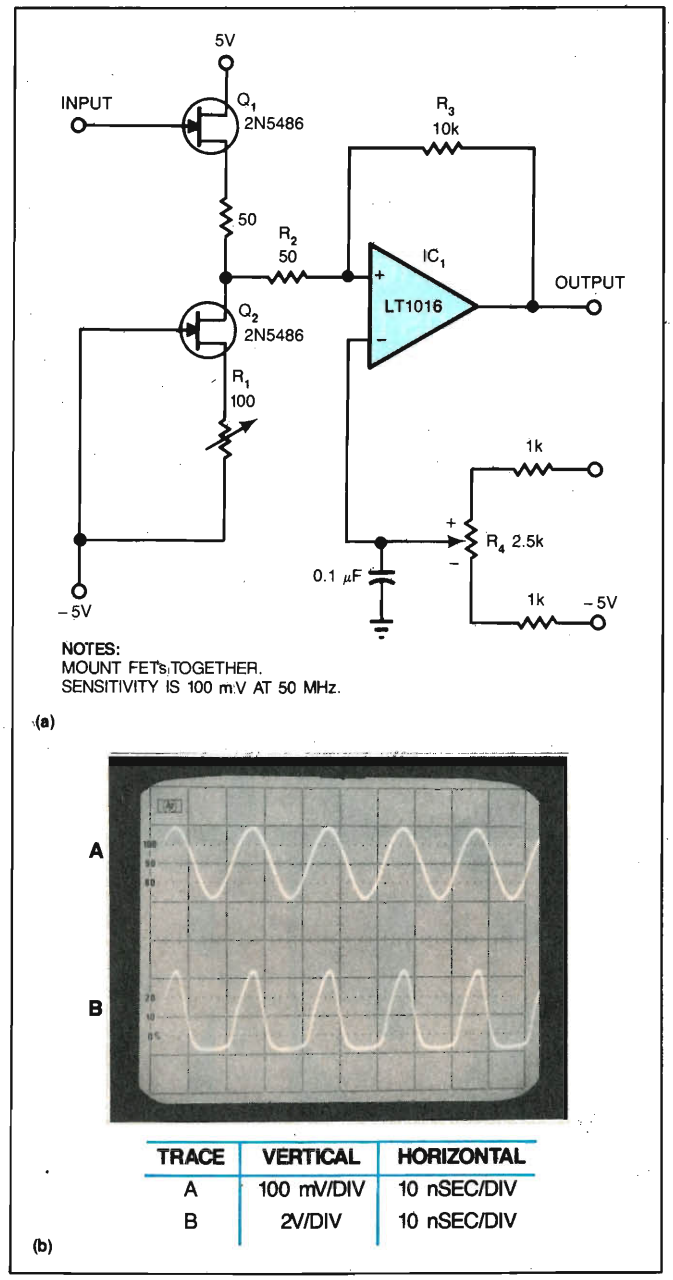


***Fig 5—This trigger circuit (a) specs 100-mV sensitivity** and provides sharp output pulses from complex input signals at frequencies from dc to 50 MHz. The circuit conditions a sine-wave input (trace A in **b**). The pulse output (trace B) is sharp enough to drive digital circuitry.*

the pulse of trace A, **Fig 4b**), current through R_2 (trace B) begins to rise, and when the resulting voltage across the resistor exceeds the threshold, IC_1 changes state. The inverting output goes low, turning on Q_1. The turn-on is speeded by feeding the positive-going pulse at the noninverting output (trace C) to Q_1's base. The resulting negative-going excursion of Q_1's collector turns off Q_2 within 5 nsec (trace D). The total delay from onset of overload to complete shutdown is just 12 nsec.

Feedback from the noninverting output of IC_1 through the normally closed reset switch to the latch pin maintains the LT1016 in the latched state. When the fault that caused the overload has been cleared, a momentary opening of the reset switch causes the

LT1016 to revert to its initial state, thereby restoring current to the load.

Counters and other digital instruments require a trigger circuit to generate clean, sharp pulses from complex waveforms. Schmitt-trigger ICs are satisfactory only at relatively low frequencies. Designing a stable trigger circuit to handle megahertz frequencies is not easy, and it often entails the use of many discrete components. However, the speed and stability of the LT1016 comparator allow you to build a very simple and stable trigger circuit with a sensitivity of 100 mV at 50 MHz.

FETs Q_1 and Q_2 (**Fig 5a**) act as a simple, high-speed buffer for the input signal. The LT1016 (IC_1) compares the buffered input signal to the threshold potential applied to its inverting input, and the comparator changes state whenever the buffered input signal crosses the threshold level. The feedback network consisting of resistors R_2 and R_3 provides hysteresis to eliminate chattering caused by noisy input signals.

Fig 5b illustrates the performance of the circuit: Trace A is a 50-MHz sine wave applied to the input, and trace B is the LT1016's output. To calibrate the circuit, ground the input terminal and adjust input-zeroing potentiometer R_1 for 0V, measured at the drain of Q_2. Then apply an input signal and adjust trigger-level potentiometer R_4 for the desired sensitivity. **EDN**

References

1. Williams, Jim, "Follow design rules for optimum use of fast comparator IC," *EDN*, June 13, 1985, pg 129.
2. Williams, Jim, "Fast comparator IC speeds converters and S/H amplifiers," *EDN*, June 20, 1985, pg 115.

Author's biography

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in the design of analog circuits and instruments. He has served in related capacities at National Semiconductor Corp, Arthur D Little Inc, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. Jim is a former student of psychology at Wayne State University, and he enjoys tennis, art, and collecting antique scientific instruments.

Article Interest Quotient (Circle One)
High 485 Medium 486 Low 487

Analog circuits operate from a 1.5V cell

In battery-powered equipment, it's often convenient to use one 1.5V cell. It's not easy, however, to design analog circuitry that performs well at such a low supply level. By using two ICs specifically conceived for low-voltage operation, you can configure several analog blocks that work from 1.3 to 1.5V rails.

Jim Williams, *Linear Technology Corp*

Two ICs that are specified for operation from one 1.5V supply allow you to design linear circuits that can work in battery-powered (for example, remote data-acquisition, medical, and power-monitoring) equipment that uses only one cell as a power source. The choice of a 1.5V supply eliminates most linear ICs as design candidates; however, the LM10 operational amplifier/reference and the LT1017/18 dual comparator are gain blocks specified for performance at low supply levels.

In addition to the limited availability of low-voltage linear ICs, the problem of 600-mV voltage drops in silicon transistors and diodes makes circuit design difficult. The voltage drop consumes a substantial portion of the available supply range. Furthermore, any circuit designed for 1.5V operation must function at the battery's end-of-life voltage, typically 1.3V (see **box,** "Components for 1.5V operation").

The design constraints are troublesome especially when you need such complex linear circuits as data converters and sample/hold amplifiers. However, by combining close attention to component characteristics and some unusual circuit-design methods, you can construct complex linear circuits as well as circuits for a crystal-controlled oscillator, a gain-of-101 amplifier, and a flyback switching regulator.

10-kHz V/F converter

For example, consider the 10-kHz V/F converter in **Fig 1a.** The 1.5V-powered circuit produces a 25-Hz to 10-kHz output for input voltages from 0 to 1V; transfer-function linearity over this range is 0.35%. Gain (full-scale) drift is 250 ppm/°C, and power-supply current consumption is approximately 800 μA.

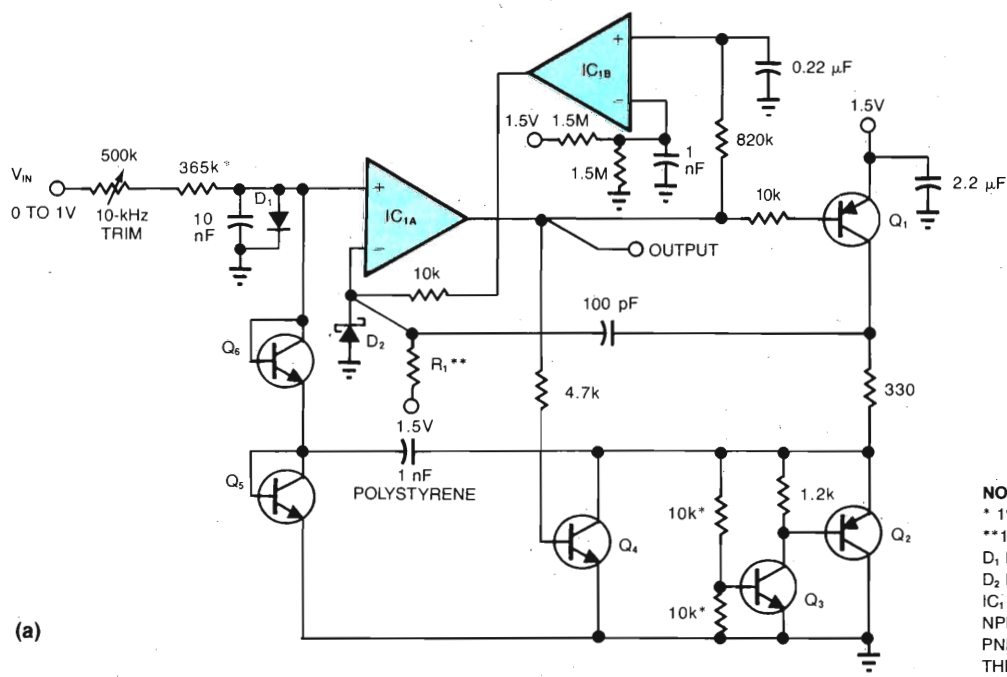
To understand circuit operation, assume IC_{1A}'s positive input is at a voltage level slightly below that of the negative input (IC_{1B} output is low). The input voltage initiates a positive-going ramp at IC_{1A}'s positive input (**Fig 1b,** trace A). IC_{1A}'s output (trace B) is low, and therefore turns on Q_1. Q_1's collector current drives the Q_2-Q_3 combination, and forces Q_2's collector to clamp at 1V.

The 1-nF capacitor charges to ground (the capacitor-current waveform is trace D) via Q_5. When the ramp at IC_{1A}'s positive input reaches a high enough level, IC_{1A}'s

Designing circuits for 1.5V single-cell operation requires a careful choice of components, as well as special design and adjustment techniques.

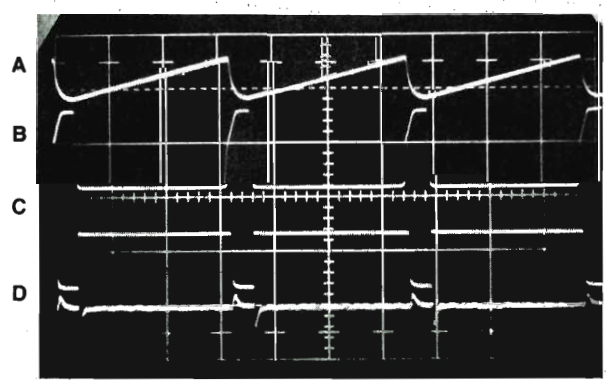
output goes high, cutting off Q_1, Q_2, and Q_3. Q_4 conducts, pulling current from IC_{1A}'s positive-input capacitor via Q_6. The current removal resets IC_{1A}'s positive-input ramp to a potential slightly below ground, thereby forcing IC_{1A}'s output low.

The 100-pF capacitor at Q_1's collector supplies positive ac feedback, thereby ensuring that IC_{1A}'s output remains positive long enough for a complete discharge of the 1-nF capacitor. The Schottky diode prevents voltage excursions that could drive IC_{1A}'s input to levels outside its common-mode limit. The feedback cuts off Q_4, then Q_1, Q_2, and Q_3 turn on and the entire cycle repeats. The oscillation frequency depends directly on the input-voltage-derived current. The junction temp-



(a)

NOTES:
* 1% FILM RESISTOR.
**1.5M TYP; TRIM FOR 25 Hz.
D_1 IS A 1N914.
D_2 IS AN HP5082-2810.
IC_1 IS AN LT1017.
NPNs ARE 2N3904.
PNPs ARE 2N3906.
THERMALLY COUPLE Q_3, Q_5, Q_6.



(b)

TRACE	VERTICAL	HORIZONTAL
A	20 mV/DIV	50 mSEC/DIV
B	1V/DIV	50 mSEC/DIV
C	1V/DIV	50 mSEC/DIV
D	400 µA/DIV	50 mSEC/DIV

Fig 1—A V/F converter powered by one 1.5V cell, *this circuit specs 0.35% linearity from 25 Hz to 10 kHz and consumes 800 µA from the battery. The circuit uses a dual comparator specified for low-voltage operation. You can trim the 25-Hz output by selecting a resistor; to trim the 10-kHz full-scale output, adjust a potentiometer.*

erature coefficients of Q_5 and Q_6 compensate the temperature coefficient of the Q_2-Q_3 1V clamp, minimizing overall temperature drift.

Circuit start-up conditions or overdrive can cause the circuit's ac-coupled feedback loop to latch. If this latch-up occurs, IC_{1A}'s output goes high. IC_{1B} detects this condition (via the 820-kΩ/0.22-μF lag network) and also goes high, lifting IC_{1A}'s negative input toward 1.5V. Because a diode clamps IC_{1A}'s positive input at 600 mV, the IC's output switches low, initiating normal circuit behavior.

To calibrate the V/F converter, apply 1 mV at the input and select the resistor connected to IC_{1A}'s negative input for a 25-Hz output. Then apply a 1V input

Components for 1.5V operation

Most commercially available linear ICs are not capable of 1.5V operation. Two that are capable are the LM10 and LT1017/1018. The first is an op-amp/reference pair that runs from rails as low as 1.1V; the second is a dual comparator that operates from voltages as low as 1.2V.

The LM10 provides good dc characteristics, although its slew rate is limited to 0.1V/μsec. The LT1017/1018 comparator specs microsecond-range response time, high gain, and good dc characteristics. Both devices consume little power.

Among the other components you'll use in low-voltage circuits are diodes, transistors, and the battery. Standard pn-junction diodes have a 600-mV voltage drop, an appreciable portion of the available supply range. At currents of less than 10 to 20 μA, the voltage drop decreases to about 450 mV. Schottky diodes exhibit only a 300-mV drop, although their reverse leakage is higher than that of standard diodes. Germanium diodes have the lowest drop (150 to 200 mV), even at relatively high currents. Often, though, the high reverse leakage of germanium devices precludes their use.

Silicon transistors have a 600-mV V_{BE} drop, but this figure decreases somewhat at very low base currents. The V_{CE} saturation drop of silicon transistors is well below 100 mV at reasonable currents; judicious device selection and use can reduce this figure to less than 25 mV.

Inverted-mode operation (collector and emitter interchanged) allows V_{CE} saturation losses at less than 1 mV, although beta in this mode is often less than 0.1, necessitating substantial base drive. Germanium transistors have two to three times lower V_{BE} and V_{CE} losses, although the devices' speed, leakage, and beta are generally not as good as those of silicon units.

Perhaps the most important component to consider is the battery. Many types of cells are available, and choosing the best one is a function of the application. Two common types are carbon-zinc and mercury. The first offers higher initial voltage, but mercury units have a much flatter discharge curve (**Fig A**) when currents are controlled.

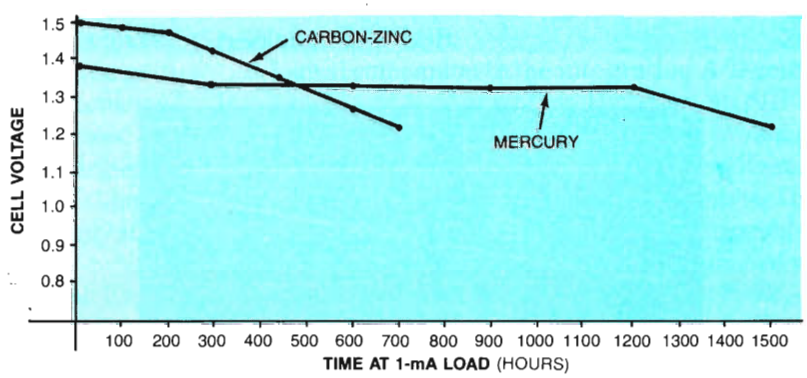


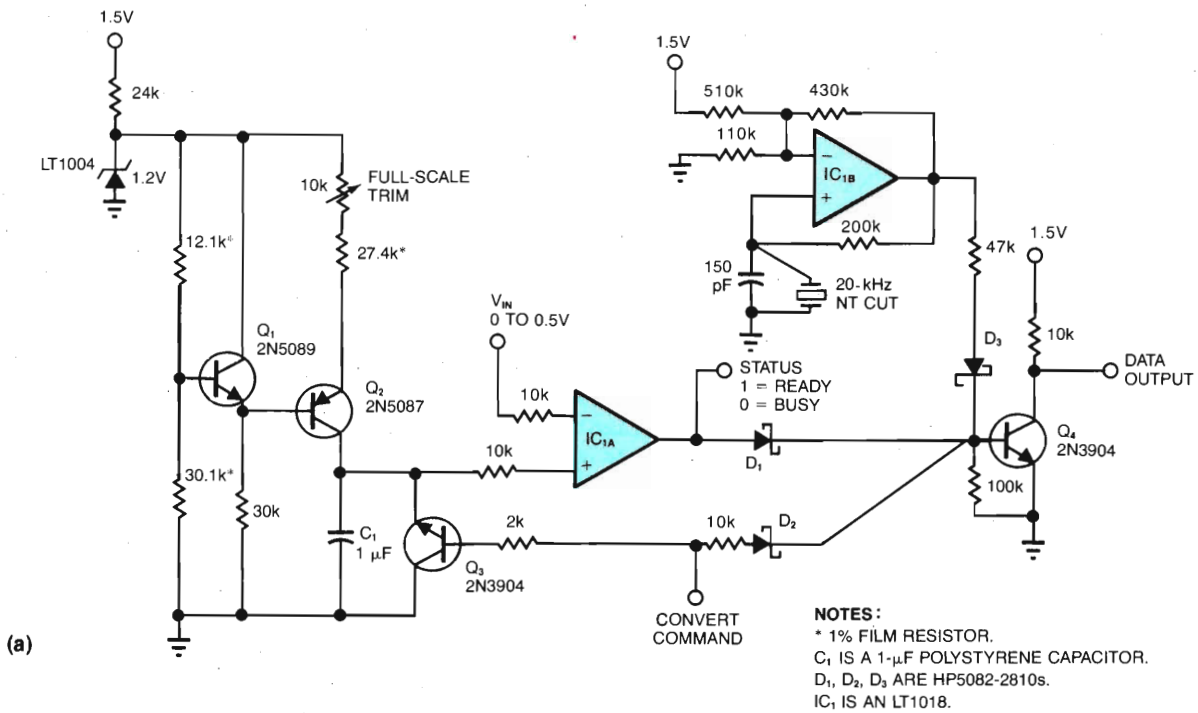
Fig A—Choose power sources carefully *when designing battery-powered systems. These curves show the disparate discharge characteristics of commonly used carbon-zinc and mercury cells. Although its initial voltage is clearly higher, the carbon-zinc cell exhibits a much steeper discharge curve than does the mercury cell. With a 1-mA load, the mercury cell overtakes the carbon-zinc unit after approximately 500 hours of operation.*

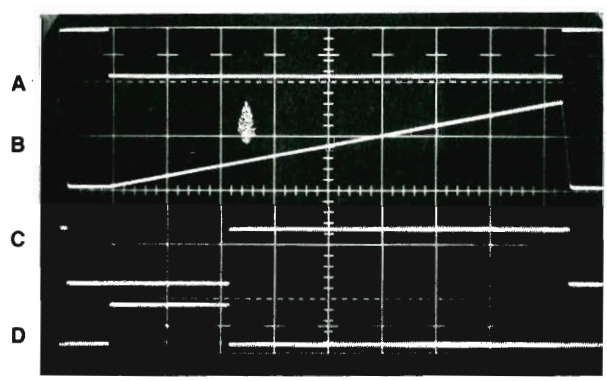
The physics of silicon semiconductors makes it difficult to design for 1.5V operation. Diode drops and saturation voltages consume much of the supply.

and trim the 500-kΩ potentiometer for a 10-kHz output.

The circuit in **Fig 2a** is another data-conversion configuration. This integrating A/D converter has a 60-msec conversion time, consumes 360 μA from its 1.5V supply, and maintains 10-bit accuracy over 15 to 35°C. A pulse applied to the convert-command line (**Fig 2b**, trace A) causes Q_3, operating in inverted mode (collector and emitter interchanged), to discharge the 1-μF capacitor (trace B).

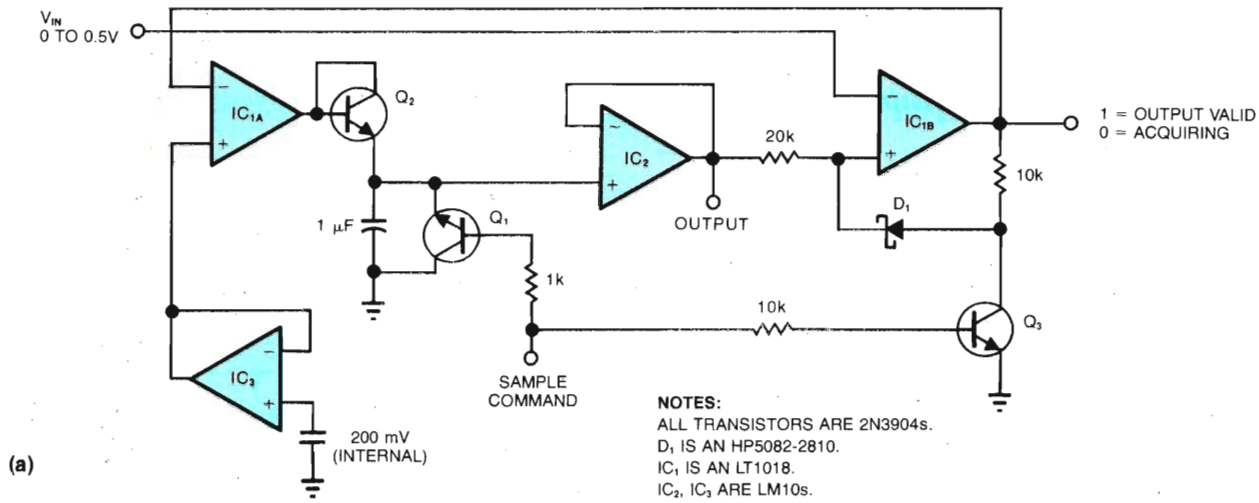
Simultaneously, the 10-kΩ/diode path biases Q_4, forc-



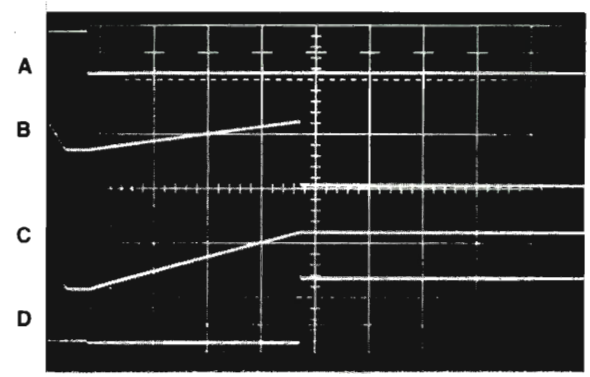


TRACE	VERTICAL	HORIZONTAL
A	2V/DIV	10 mSEC/DIV
B	0.5V/DIV	10 mSEC/DIV
C	1V/DIV	10 mSEC/DIV
D	2V/DIV	10 mSEC/DIV

***Fig 2—This 10-bit-accurate A/D converter** is ideal for battery-powered applications. It converts in 60 msec and maintains its accuracy over 15 to 35°C. The converter is an integrating type: The number of pulses appearing at the output is proportional to the input voltage.*



(a)



(b)

TRACE	VERTICAL	HORIZONTAL
A	2V/DIV	1 mSEC/DIV
B	1V/DIV	1 mSEC/DIV
C	0.5V/DIV	1 mSEC/DIV
D	1V/DIV	1 mSEC/DIV

Fig 3—Eliminating an S/H amplifier's FET switch *is one way to design a 1.5V-powered circuit. This S/H amplifier has 0.1% accuracy, making it suitable for systems with 10-bit resolution. The circuit acquires a signal in 4 msec max and specs 10-μV/msec droop. You can use the S/H unit as a companion for the low-voltage A/D converter in* ***Fig 2.***

ing the transistor's collector low (trace D). Q_3's inverted-mode switching results in a capacitor discharge to within 1 mV of ground. When the convert command goes low, Q_3 turns off, Q_4's collector voltage rises, and the LT1004-stabilized Q_1-Q_2 current source charges the 1-μF capacitor with a linear ramp. During the time the ramp's value is below that of the input voltage, IC_{1A}'s output is low (trace C).

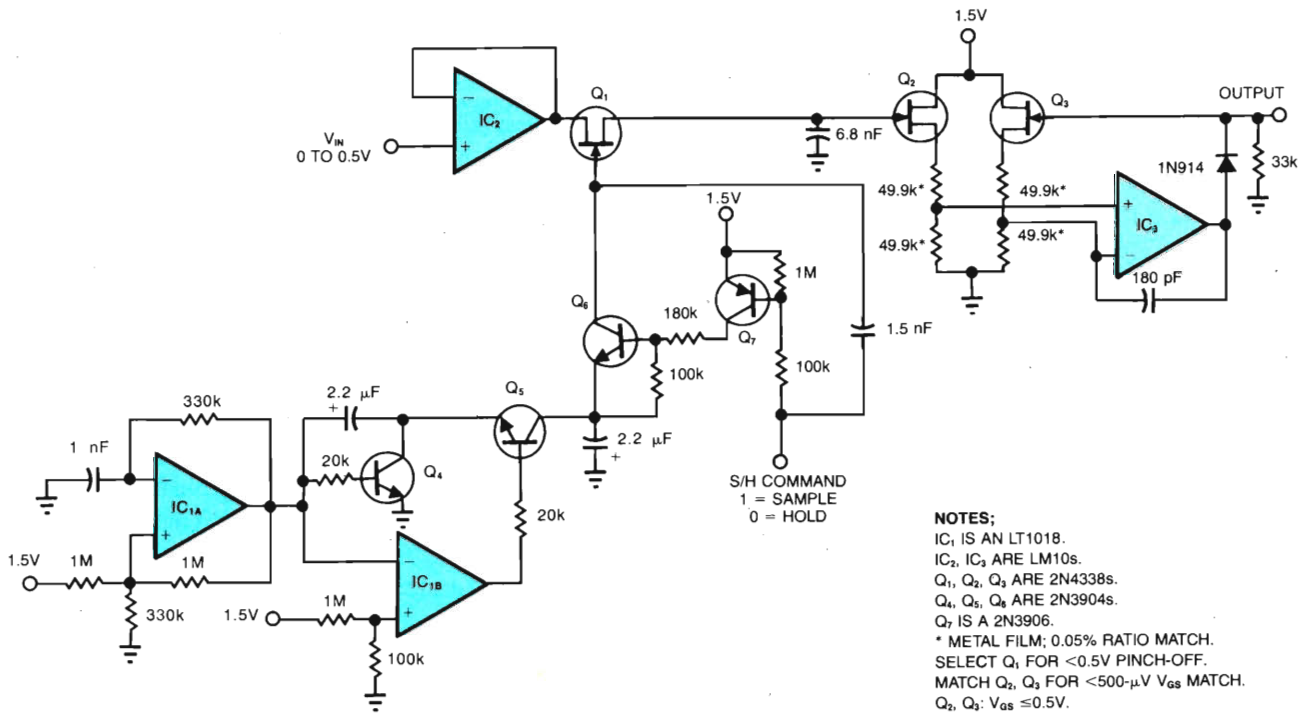
The low output at IC_{1A} allows pulses from IC_{1B}, a quartz-stabilized oscillator, to modulate Q_4. Output data appears at Q_4's collector (trace D). When the ramp crosses the input-voltage level, IC_{1A}'s output goes high and biases Q_4; output data then ceases. The number of pulses appearing at the output is directly proportional to the input voltage.

To calibrate the A/D converter, apply 0.5V to the input and trim the 10-kΩ potentiometer for exactly 1000 output pulses each time the convert-command line is pulsed. No zero trim is required; however, Q_3's inverted-mode, 1-mV saturation voltage limits zero resolution to 2 LSB.

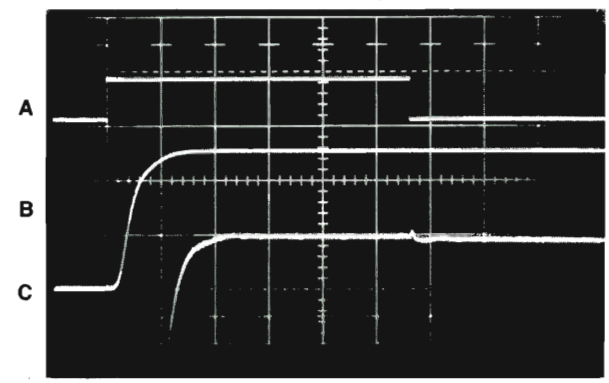
A logical companion to the integrating A/D converter is a sample-and-hold amplifier. However, an S/H amplifier is one of the most difficult circuits to design for 1.5V operation, primarily because FET switches with low enough pinch-off voltages are unavailable. The S/H circuit in **Fig 3a** circumvents the switch problem by eliminating the switch. Although it's an unusual way to implement an S/H amplifier, the switchless circuit requires no special components or trimming, it's easy to build, and it has a 4-msec acquisition time to a 0.1% error band.

When a sample command (**Fig 3b,** trace A) arrives, Q_1, operating in inverted mode, discharges the 1-μF capacitor (trace C). When the sample command's voltage drops, Q_1 turns off and IC_{1A}'s internal pull-up current source (trace B) charges the capacitor via Q_2, a transistor connected as a low-leakage diode. IC_2, a buffer for the capacitor's charging ramp, biases IC_{1B}'s positive input. When the ramp's potential crosses the

Single-cell-powered V/F and A/D converters are ideal for such remote-monitoring applications as medical, data-acquisition, and power-monitoring equipment.



NOTES;
IC_1 IS AN LT1018.
IC_2, IC_3 ARE LM10s.
Q_1, Q_2, Q_3 ARE 2N4338s.
Q_4, Q_5, Q_6 ARE 2N3904s.
Q_7 IS A 2N3906.
* METAL FILM; 0.05% RATIO MATCH.
SELECT Q_1 FOR <0.5V PINCH-OFF.
MATCH Q_2, Q_3 FOR <500-µV V_{GS} MATCH.
Q_2, Q_3: V_{GS} ≤0.5V.



(b)

TRACE	VERTICAL	HORIZONTAL
A	2V/DIV	50 µSEC/DIV
B	0.2V/DIV	50 µSEC/DIV
C	10 mV/DIV	50 µSEC/DIV

Fig 4—A charge-pump-driven FET switch *is the key to the operation of this S/H amplifier, which is speedier but more complex than the one in* ***Fig 3.*** *This S/H circuit also operates from one 1.5V cell, but it acquires a signal in 125 µsec as opposed to the 4 msec required of the* ***Fig 3*** *circuit. You must take special care, though, in selecting the FETs—pinch-off voltage and V_{GS} matching and absolute value are critical parameters.*

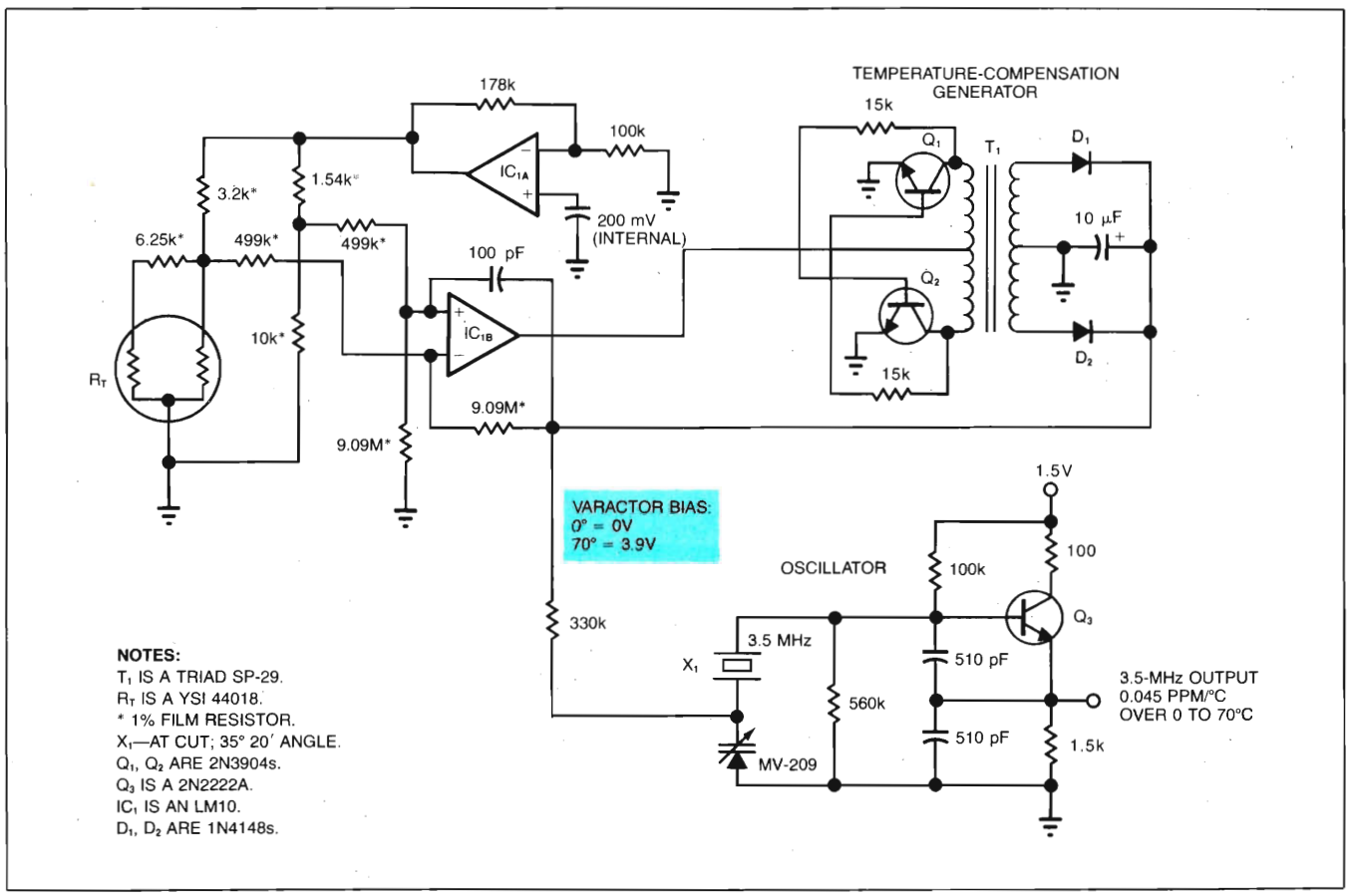


Fig 5—A drift-compensation scheme *stabilizes the output frequency of this crystal-controlled, 1.5V-powered oscillator. A thermistor in a bridge circuit provides a temperature-dependent signal; a self-exciting up converter scales the signal to a value adequate to bias the varactor that acts as a variable capacitor in series with the crystal. The compensation improves frequency stability by a factor of greater than 10.*

input voltage (applied to IC_{1B}'s negative input), IC_{1B}'s output goes high (trace D).

The high output forces IC_{1A}'s output low, and the 1-µF capacitor stops charging. Under these conditions, the circuit is in hold mode. The voltage on the capacitor is then the same as the input voltage, and the circuit's output appears at the output of IC_2. The 10-kΩ/diode path at IC_{1B} provides a latch that prevents input-voltage changes or noise from affecting the value stored in the 1-µF capacitor. When the next sample command arrives, Q_3 breaks the latch and circuit action repeats.

Acquisition time is proportional to the input voltage; a full-scale (0.5V) input requires 4 msec. Although faster acquisition is possible, the switching delay in shutting off IC_{1A}'s output will degrade accuracy. The circuit's primary features are its elimination of the FET-switch requirement and relative simplicity. The S/H amplifier's accuracy is 0.1%, droop specs at 10 µV/msec, and current consumption is 350 µA.

The circuit in **Fig 4,** a more conventional approach to the sample-hold function than the **Fig 3** circuit, is significantly faster, but it's also more complex and it has special construction requirements. Q_1 serves as the sample-hold switch, and Q_6 and Q_7 provide a level shift to drive Q_1's gate. To minimize power consumption, a 1500-pF feed-forward path provides fast gate switching without resorting to high operating currents in Q_6 and Q_7.

IC_{1A}, a simple square-wave oscillator, drives Q_4. IC_{1B} inverts IC_{1A}'s output and biases Q_5. Q_4 and Q_5 serve as synchronous switches and pump charge to the 2.2-µF capacitor at Q_5's collector, resulting in a negative voltage on the capacitor. Q_1's low pinch-off voltage is obtained at the expense of on-resistance. The typical 1.5- to 2-kΩ on-resistance mandates that the circuit's hold capacitor be small to obtain fast acquisition.

Magnetic components—transformers and inductors—make it possible to design circuits that deliver outputs beyond the limits imposed by the 1.5V supply.

The low capacitance dictates a low-bias-current output amplifier; otherwise, droop rate suffers. Q_2, Q_3, and IC_3 meet the low-bias-current need. Q_2 and Q_3 are configured as source followers; the resistors serve as level shifters to keep IC_3's inputs inside the LM10's common-mode range. By setting the LM10's output voltage well above ground, IC_3's output diode ensures clean dynamic performance for voltages close to 0V. The 180-pF capacitor compensates the composite amplifier.

You must take several precautions to use this circuit. To ensure proper turn-off, select Q_1, already an extremely low-pinch-off device, for a pinch-off voltage below 500 mV. Next, any V_{GS} mismatch between Q_2 and Q_3 will contribute to offset error; therefore, you must select these devices for V_{GS} matching within 500 μV. Also, V_{GS} for Q_2 and Q_3 must be less than 500 mV, otherwise IC_3 can encounter common-mode limitations for circuit inputs near full scale. Finally, mismatches in the level-shift resistors contribute gain errors. To maintain 0.1% circuit accuracy, the ratio match must be within 0.05%.

The preceding precautions taken, the circuit performs well for a 1.5V-powered sample-and-hold amplifier. Acquisition time is 125 μsec to a 0.1% error band, and the droop rate is 10 μV/msec. Current drain is less than 700 μA. **Fig 4b** shows the circuit acquiring a full-scale input. Trace A is the sample-hold command and trace B is the circuit's output. Trace C, an expanded-amplitude version of trace B, shows details of the output waveform. Acquisition takes place within 125 μsec, and sample-hold offset is within 1 mV.

A stable 1.5V oscillator

In addition to S/H amplifiers, you can use the LM10 to build a temperature-stable crystal oscillator. Many systems require a clock source, and crystal oscillators that run from 1.5V are relatively easy to construct. However, if your system needs good stability over temperature, the design task becomes more difficult. You could use a crystal oven, but this approach leads to excessive power consumption. An alternate method provides open-loop, correcting bias to the oscillator; the bias value is determined by absolute temperature.

The correcting bias cancels the oscillator's predictable and repeatable thermal drift. The simplest way to implement such a scheme is to vary the crystal's resonance point slightly by means of a variable shunt or series impedance. Varactor diodes, whose capacitance varies with reverse voltage, commonly fulfill this variable-impedance role. Unfortunately, these diodes require volts of reverse bias to generate significant capacitance shifts, so direct 1.5V-powered operation is impossible.

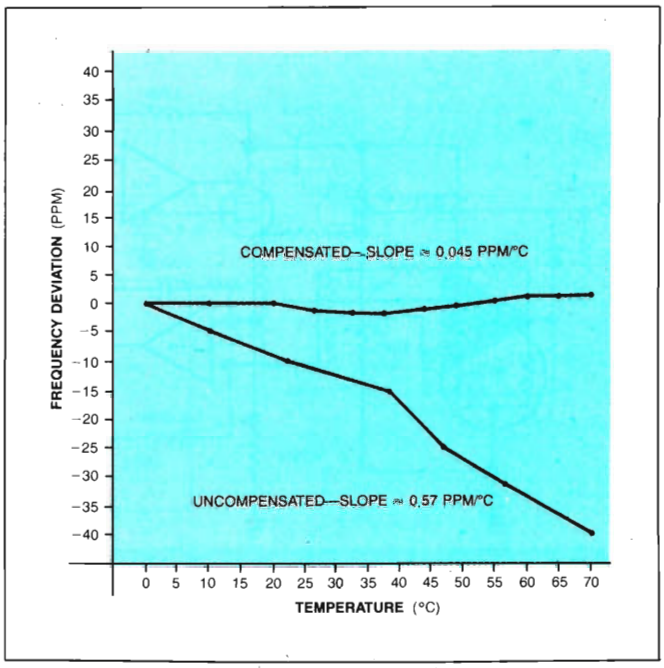


Fig 6—The benefits of oscillator-drift compensation *are evident in these curves, showing the temperature stability of the circuit in* ***Fig 5.*** *The compensated oscillator's output frequency exhibits a temperature-drift slope of approximately 0.045 ppm/°C over 0 to 70°C, vs an uncompensated circuit's 0.57 ppm/°C. The slight irregularities in the compensated circuit's temperature function arise from basic nonlinearities in the oscillator's drift characteristic.*

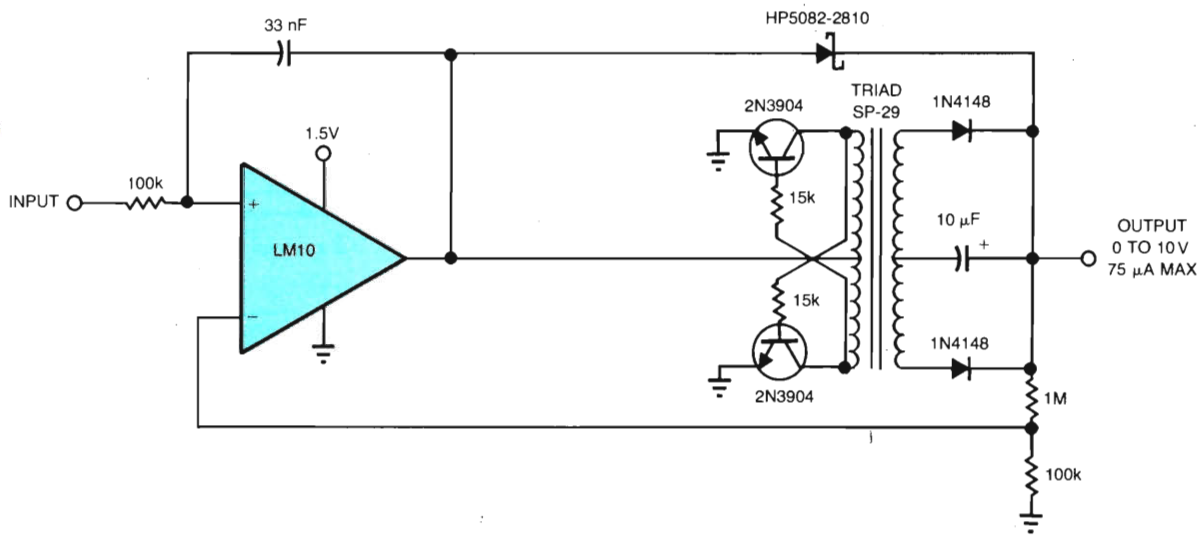
The circuit in **Fig 5** accomplishes the temperature-compensation function. The transistor and associated components form a Colpitts oscillator that runs from the 1.5V supply. The varactor diode, in series with the crystal, tunes the oscillator's frequency as the diode's dc bias varies. The remaining circuitry generates an ambient-temperature-dependent dc bias.

The thermistor network and IC_{1B} produce a temperature-dependent signal that corrects for the thermal drift of the specified crystal type. The 1.5V-powered LM10 op amp could not normally provide the output levels required to bias the varactor. Here, however, a self-exciting, switch-mode up converter (T_1 and associated components) forms part of the LM10's feedback loop. The LM10 drives the switching converter's input so it generates as much output voltage as is required to close the loop.

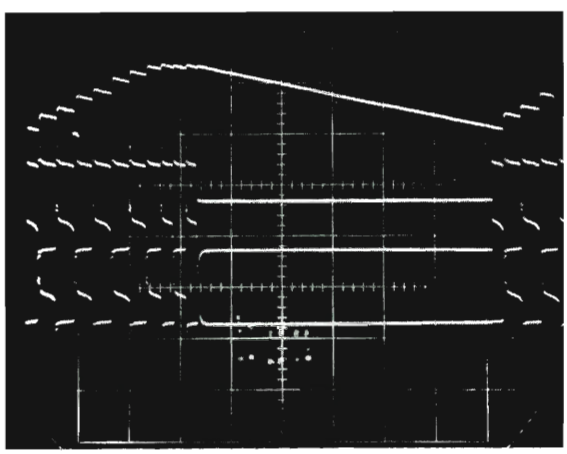
The thermistor-bridge network and the amplifier's

feedback resistor are scaled to produce appropriate temperature-dependent varactor bias. IC_{1A}, the LM10's reference portion, stabilizes the temperature network against 1.5V-supply variations. **Fig 6** plots compensated vs uncompensated oscillator drift. The compensation improves drift performance by a factor of greater than 10. Residual aberrance in the compensated curve results from the first-order linear fit that the circuit applies to the oscillator's nonlinear drift characteristic. Current drain is less than 850 μA.

By borrowing from the method used by the **Fig 5** circuit to generate high-voltage outputs, you can effect an interface between 1.5V-powered circuitry and higher-voltage systems. Such an interface could be used, for example, in 1.5V-driven, remote data-acquisition equipment that feeds a line-powered data-gathering



(a)

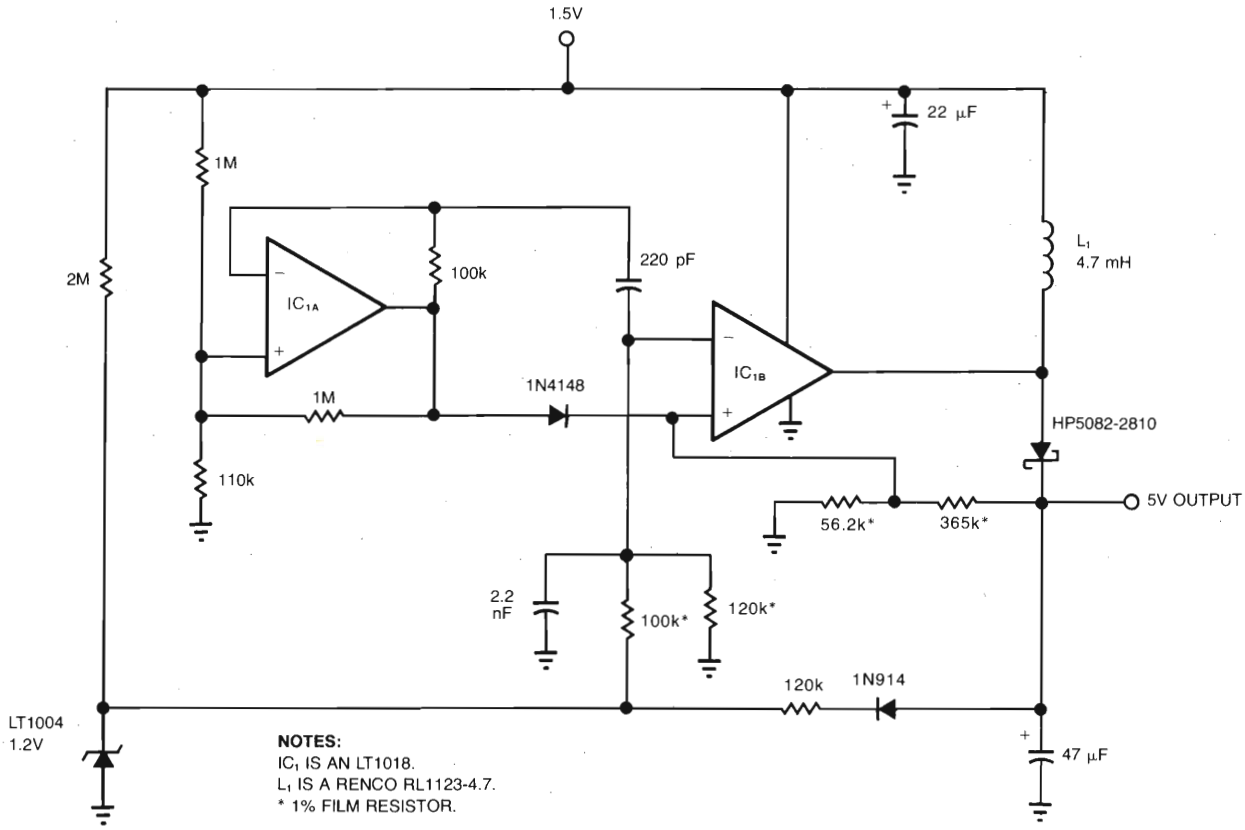


TRACE	VERTICAL	HORIZONTAL
A	10 mV/DIV (AC COUPLED)	10 mSEC/DIV
B	2V/DIV	10 mSEC/DIV
C	5V/DIV	10 mSEC/DIV
D	5V/DIV	10 mSEC/DIV

(b)

Fig 7—A 0 to 10V output with one 1.5V cell *is possible in this gain-of-101 amplifier because of the self-exciting up converter at the output. The op amp provides the converter's transformer with enough energy to close the feedback loop; the 1-MΩ/100-kΩ divider sets the gain. The Schottky diode bypasses the up converter for low-level signals not needing the converter's step-up action.*

Many circuits work in logic-driven systems, but no commercially available logic, μP, or memory family will operate from 1.5V.



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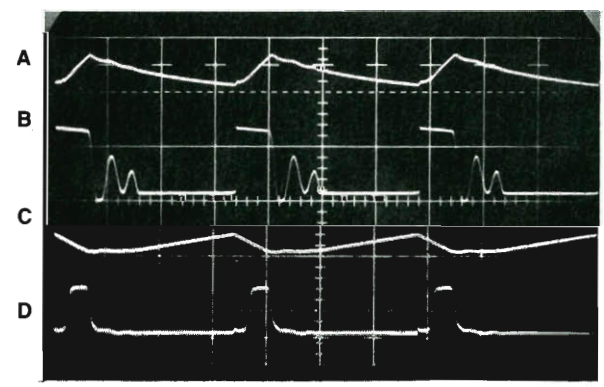


TRACE	VERTICAL	HORIZONTAL
A	0.5V/DIV	10 μSEC/DIV
B	5V/DIV	10 μSEC/DIV
C	20 mA/DIV	10 μSEC/DIV
D	0.5V/DIV	10 μSEC/DIV

(b)

Fig 8—Power 5V logic blocks from a 1.5V cell *with the flyback switching regulator in* ***a****. Energy from the output inductor charges the 47-μF capacitor; the circuit derives its reference from the 1.2V LT1004. The series diode-resistor combination from the output to the LT1004 provides immunity from variations in the 1.5V supply, and thereby aids line regulation.*

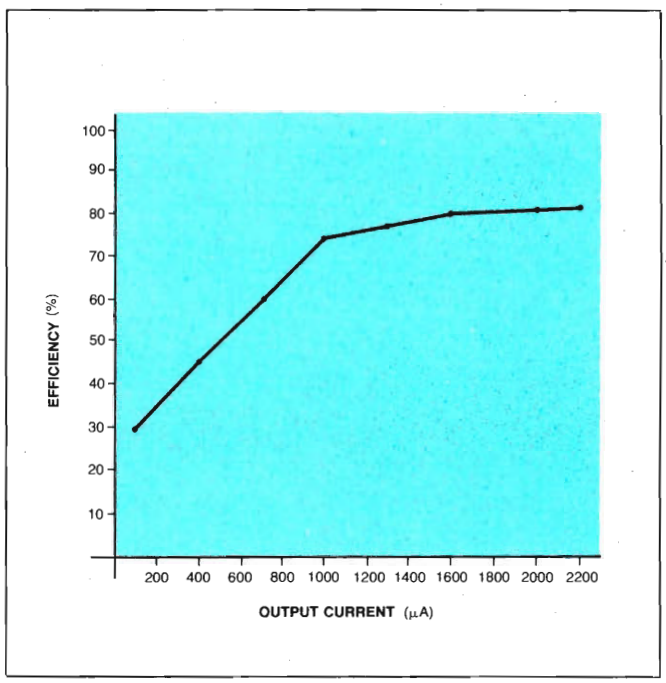


Fig 9—The efficiency of Fig 8's 5V regulator *is a function of load current. Fixed losses in the regulator are responsible for low efficiency at low currents; with higher currents, the figure reaches 80%.*

point. Although the battery-powered portion can provide local processing of signals with 1.5V-powered circuitry, it's useful to address the high-level monitoring instrumentation at higher voltages.

The 1.5V-powered amplifier in **Fig 7** provides 0 to 10V outputs and load currents as high as 75 μA. The LM10 drives the self-exciting up converter with enough energy to close the feedback loop. In this case, the amplifier is configured with a gain of 101, although other gain values are easy to realize. The sole restriction to the circuit's operation is to not exceed the 1.5V-powered LM10's common-mode input range.

The Schottky diode bypasses the up converter for low-voltage inputs, aiding output-noise performance. Overlap between the up converter's turn-on threshold and the diode's forward threshold ensures clean, dynamic behavior at the transition point. To increase efficiency, the 33-nF capacitor provides positive ac feedback, forcing the LM10's output to provide pulse-width modulation to the up converter.

Fig 7b gives details of the circuit's operation. The output (trace A) decays until the LM10 switches (trace B), thereby starting the up converter. The two transistors' collectors (traces C and D) alternately drive the transformer until the output voltage rises to a high enough level to shut off the LM10's output. The sequence repeats; the repetition rate depends on the output voltage and loading conditions.

Single-cell 5V regulator

Although many of the circuits described earlier work in logic-driven systems, no commercially available logic, microprocessor, or memory family will operate from 1.5V. Therefore, it's necessary to devise a way to drive standard logic blocks from a 1.5V battery. The simplest way to do this is to use a switching regulator designed for 1.5V-input operation. **Fig** 8's flyback configuration, originated by RJ Widlar (LT1017/18 Notes, Linear Technology Corp memorandum, 1984), delivers a 5V output.

IC_{1A} serves as an oscillator that provides a ramp (**Fig 8b,** trace A) at IC_{1B}'s dc-biased negative input. IC_{1B} compares a divided version of the output with a reference point derived from the LT1004. The ramp signal, summed with the reference point, causes IC_{1B}'s output to undergo width modulation (trace B). During the time IC_{1B}'s output is low, current builds in its output inductor (trace C).

When the ramp at IC_{1B}'s input reaches a low enough level, IC_{1B}'s output goes high, and the inductor discharges into the 47-μF capacitor. The diode from IC_{1A}'s output to IC_{1B}'s positive input supplies a pulse (trace D) on each oscillator cycle, thereby ensuring loop start-up. The 120-kΩ/diode path from the output bootstraps the LT1004's bias, thus aiding overall regulation. **Fig 9** plots regulator efficiency. Because of fixed losses in the regulator, small loads produce the lowest efficiency; however, the circuit exhibits 80% efficiency for loads greater than 1500 μA. **EDN**

Author's biography

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and -instrumentation design. He has served in related capacities at National Semiconductor Corp, Arthur D Little Inc, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art, and collecting antique scientific instruments.

Article Interest Quotient (Circle One)
High 479 Medium 480 Low 481

Test your analog-design IQ Part 2

Midterm break is over; it's time to test your skill with 25 entirely new linear-design challenges, some of which have deliberately planted bugs. Designed with more recent ICs than those in Part 1, these circuits reflect modern-day speed and stability problems.

Jim Williams, *Linear Technology Corp*

Pit your wits against analog gremlins in this quiz, a continuation of the test that appeared in EDN's Nov 28, 1985, issue. (Part 1 is an updated version of the quiz that appeared in the October 5, 1979, issue of EDN.) These new circuits incorporate more recent semiconductor devices, many of which were unavailable in 1979. The circuits demonstrate the enhanced speeds and stability possible with today's devices.

Ready? Begin!

1. **Fig 1** shows a motor-speed control circuit that uses the motor's back EMF as the speed signal. IC_1, configured as an oscillator, drives the Q_1-Q_3 pair, thereby providing pulsed excitation to the motor. The 4016 switch and associated components form a synchronously updated servo amplifier. The speed signal, sampled between Q_3's output pulses, is stored in the 0.047-μF capacitor. IC_2's output, a dc signal, closes the loop at IC_1's noninverting input. IC_1 responds by varying its duty cycle to control motor speed. What are the func-

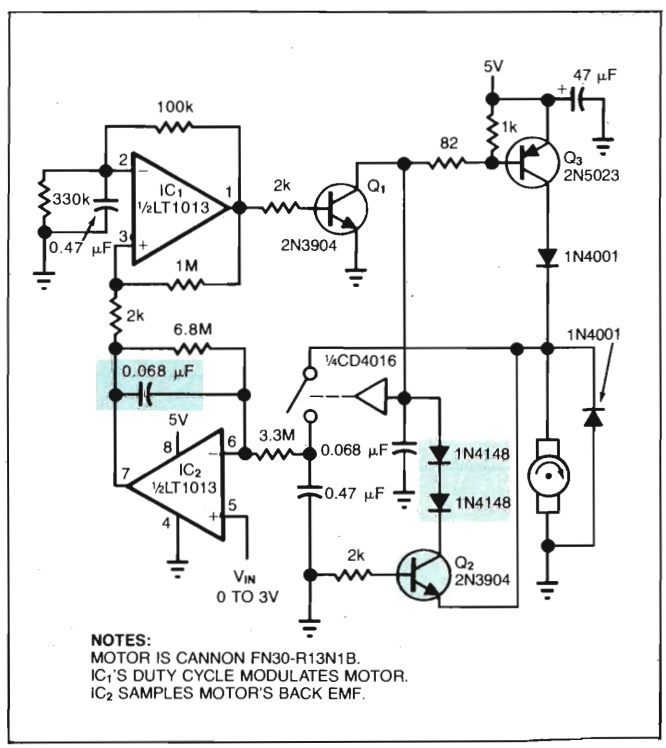


***Fig 1—Q_2, the 0.068-μF capacitor, and the 1N4148 diodes** in this motor-speed control circuit play a vital role. What is that role?*

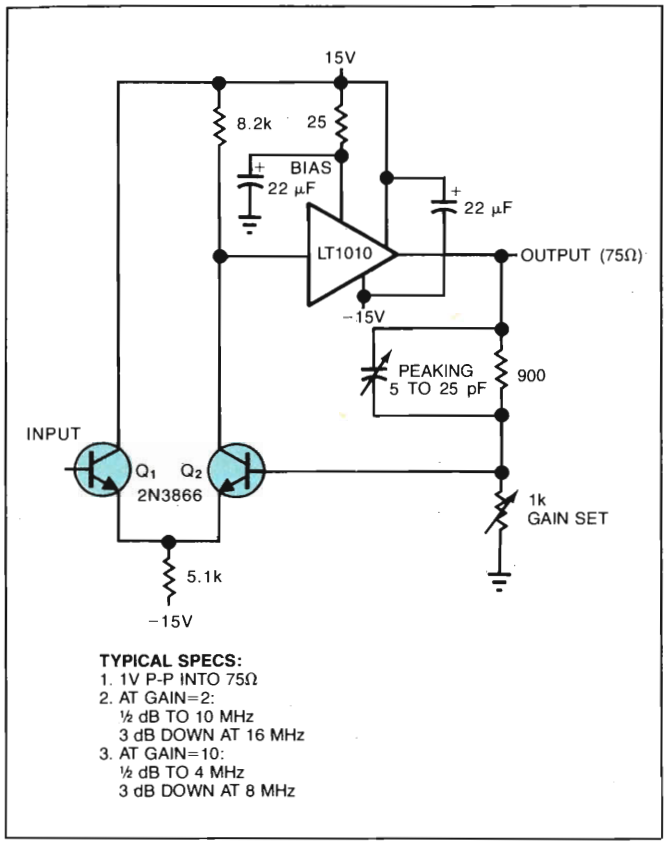


Fig 2—Eliminate the output offset *caused by V_{BE} mismatch in the input transistors in this video amplifier.*

tions of Q_2, the 0.068-µF capacitor, and the 1N4148 diodes?

2. The circuit in **Fig 2** is a video amplifier. Although the dc response of video amplifiers is generally not crucial, it's a good idea to minimize offset in the amplifier's output. A mismatch in the V_{BE}s of the discrete input transistors can generate such output offset voltages, particularly at high gains. Suggest a simple way to solve the problem.

3. **Fig 3** shows a quartz-stabilized V/F converter. It operates by clocking the LTC1043 charge pump in such a way as to force the voltage at IC_1's summing junction to 0V. IC_1's output ramp sets the flip-flop, and the IC_2 quartz-controlled oscillator resets it. The flip-flop's resultant Q_1 output controls the charge pump. The LM199-IC_3 combination serves as a reference. The circuit's schematic diagram contains two errors. Find them.

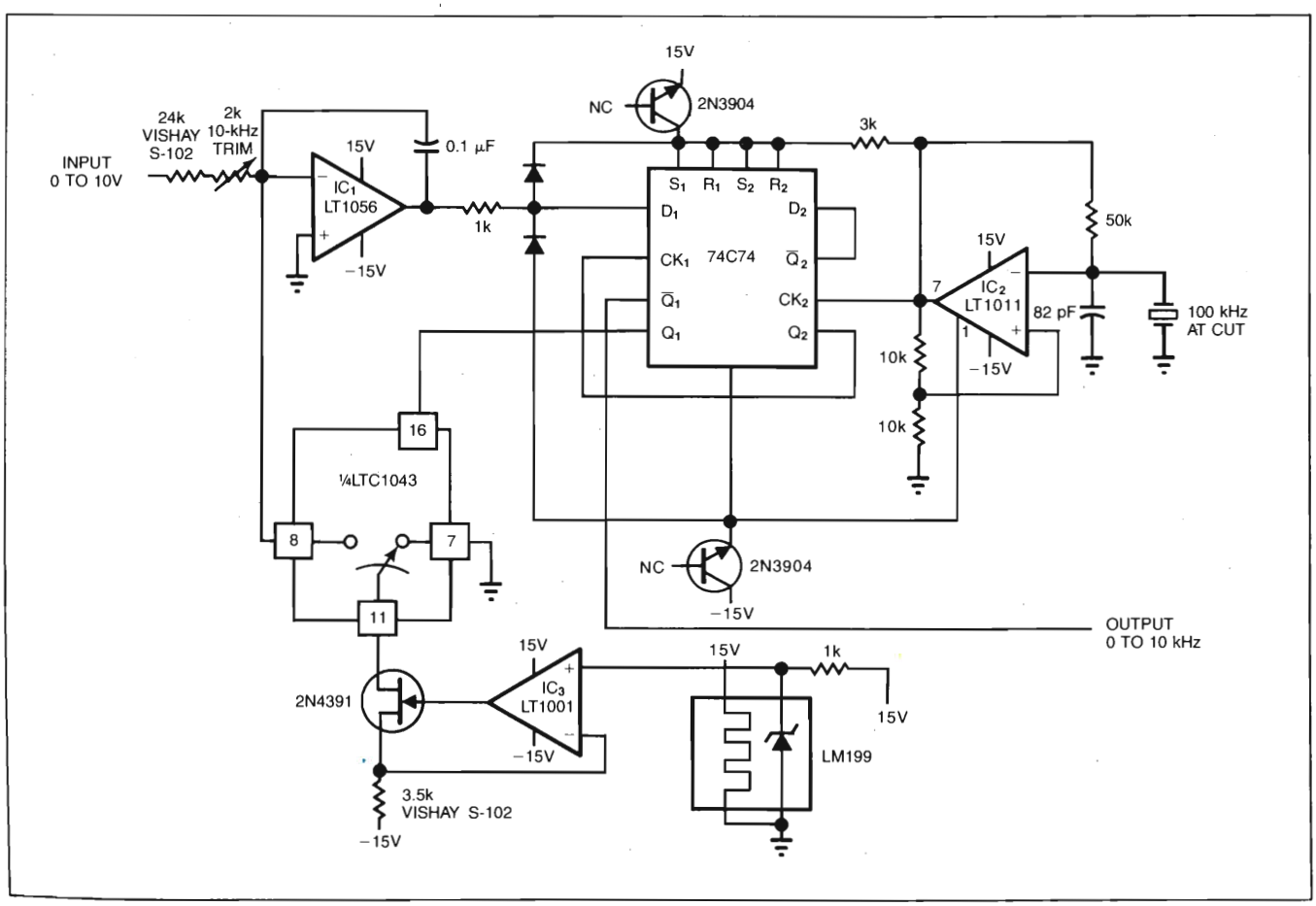


Fig 3—This quartz-stabilized V/F converter won't work. *Can you find and correct the two connection errors that prevent this circuit from functioning properly?*

You must sometimes use subtle circuit tricks to stabilize or protect linear circuitry.

4. Something is missing from the circuit in **Fig 4.** What is it?

5. **Fig 5** shows a fast level shifter that converts the LT1016's TTL outputs to +5, −10V levels for FET-gate drive. With the addition of two components, the circuit will switch in the 3- to 4-nsec range. Add the necessary components.

6. The crystal-oscillator circuit in **Fig 6** functions well with AT-cut crystals designed to operate at approximately 10 MHz or below. With higher-frequency crystals, however, the circuit often provides multiples of the intended frequency. Devise a simple solution to the problem and explain why your solution works.

7. The circuit in **Fig 7** is a simple voltage reference. The inverted-mode transistor serves as a first-order, temperature-compensated zener diode, and the op amp provides scaled buffering. The 5-nF capacitor filters noise. Most voltage references of this type work, but some exhibit output noise. There is a very evil gremlin in this circuit. What is it?

8. **Fig 8** gives the schematic diagram of a μA733 video amplifier. The configuration of the input stage

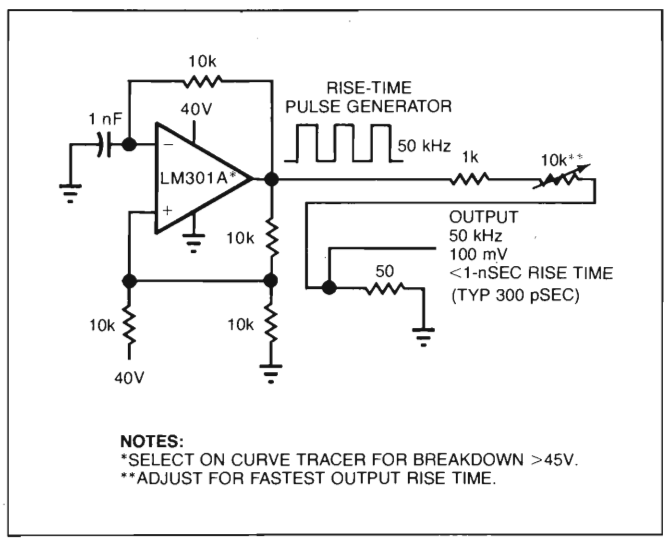


Fig 4—Something is missing *from this pulse-generation circuit. What is it?*

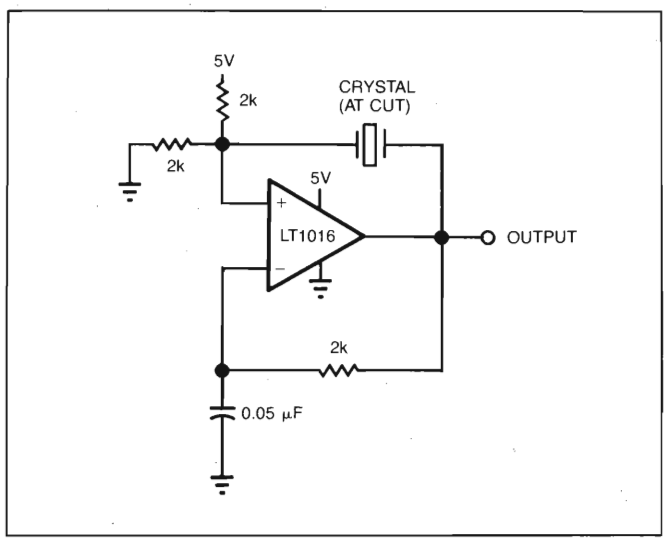


Fig 6—Eliminate the 10-MHz high-frequency limitation *inherent in this crystal-oscillator circuit.*

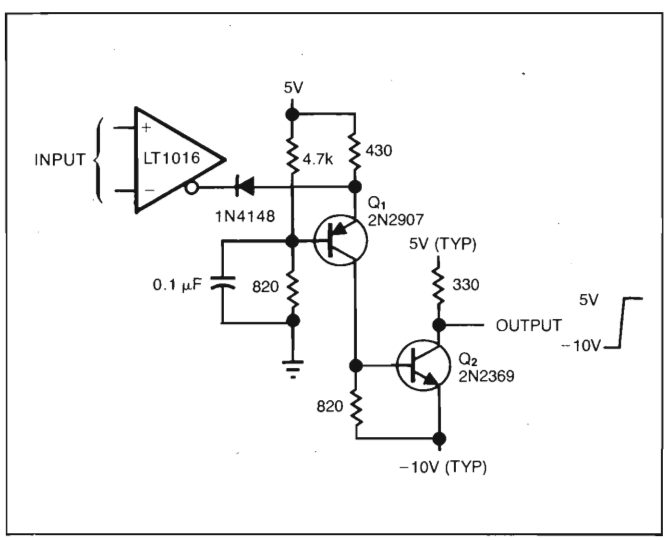


Fig 5—By adding two components, *you can make this level shifter switch in only 3 to 4 nsec.*

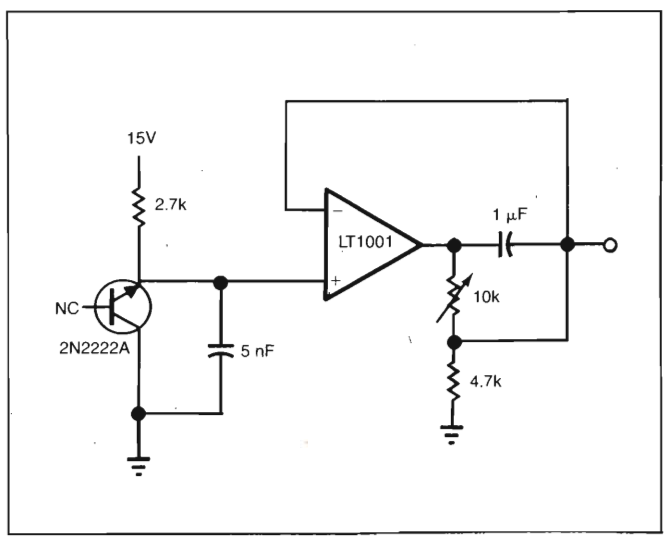


Fig 7—A mischievous gremlin lurks *in this simple voltage-reference configuration. Find the gremlin and eliminate it.*

In linear-circuit design, adding a few components often makes the difference between smooth performance and erratic, unpredictable operation.

suggests an application other than high-frequency amplification. Using only the user-accessible pins, sketch the application circuit. (Hint: You may ground the V+, V−, and output lines.)

9. Once you've determined the potential alternate use for the 733 in question 8, discuss the reasons why the reconfigured circuit might not work well.

10. **Fig 9** shows a transistor that has suffered emitter-base breakdown. Predict the voltage at the collector and describe the mechanism that's responsible for the existence of this voltage level.

11. The 1.5V-powered A/D converter in **Fig 10** is designed to operate over 25 to 35°C. The dual-transistor current source produces a ramp, which IC_1 com-

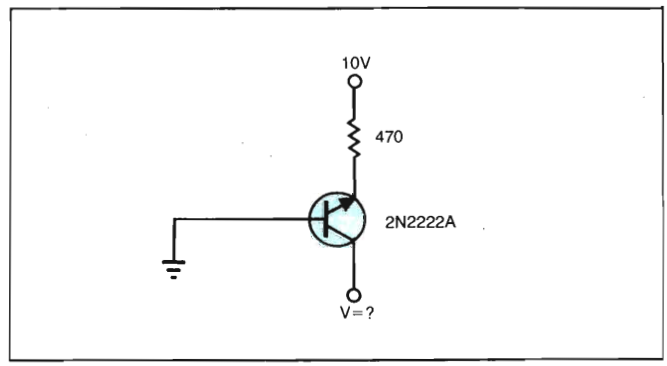


Fig 9—Test your knowledge of transistor trivia. *Under the condition of base-emitter breakdown, what's the collector voltage in this circuit configuration?*

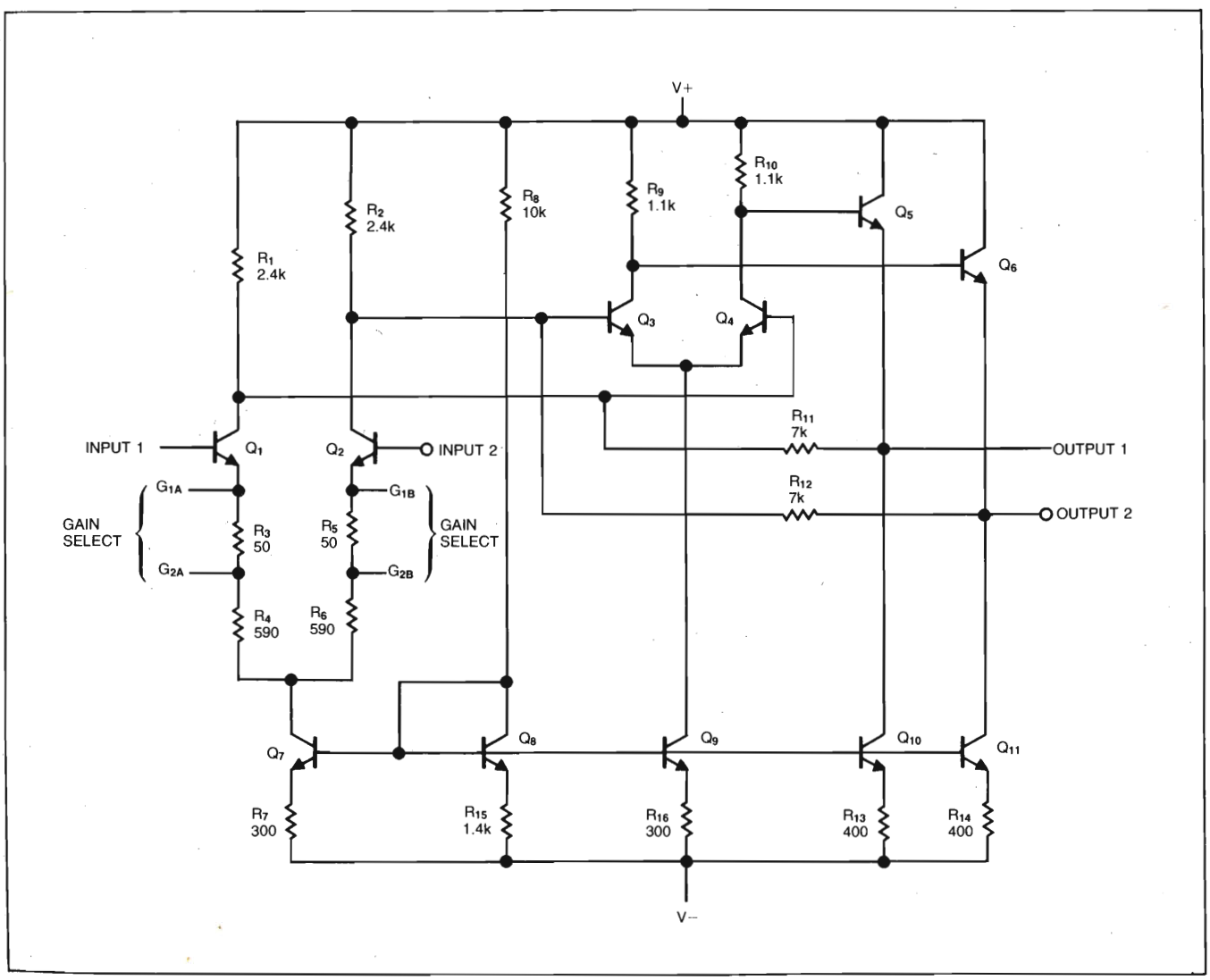


Fig 8—Find an unorthodox application *for this monolithic video amplifier. You may ground any pins you like.*

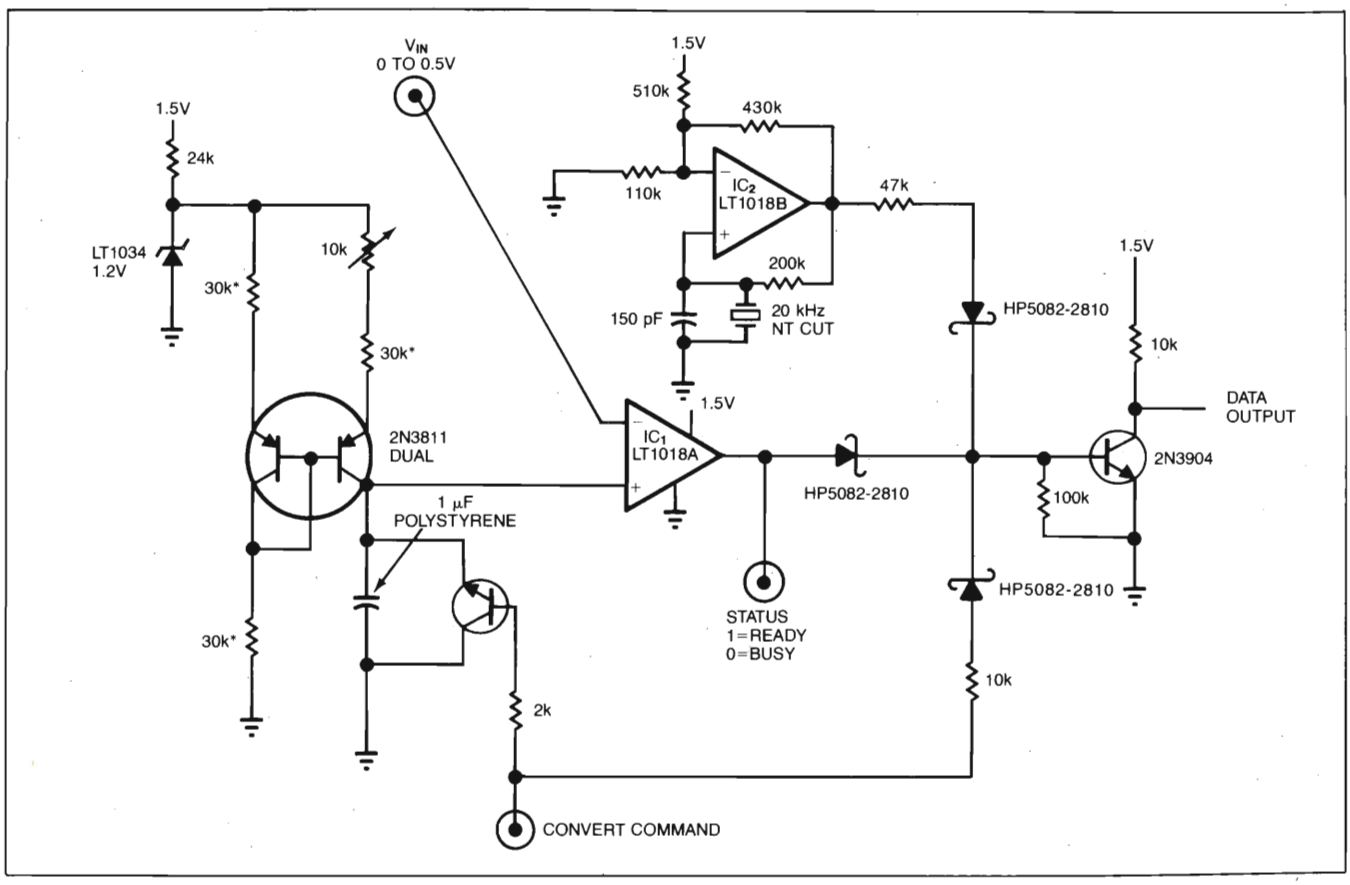


Fig 10—Sharpen your drift-reduction skills *with this 10-bit A/D converter. Find and eliminate the principal contributor to gain drift.*

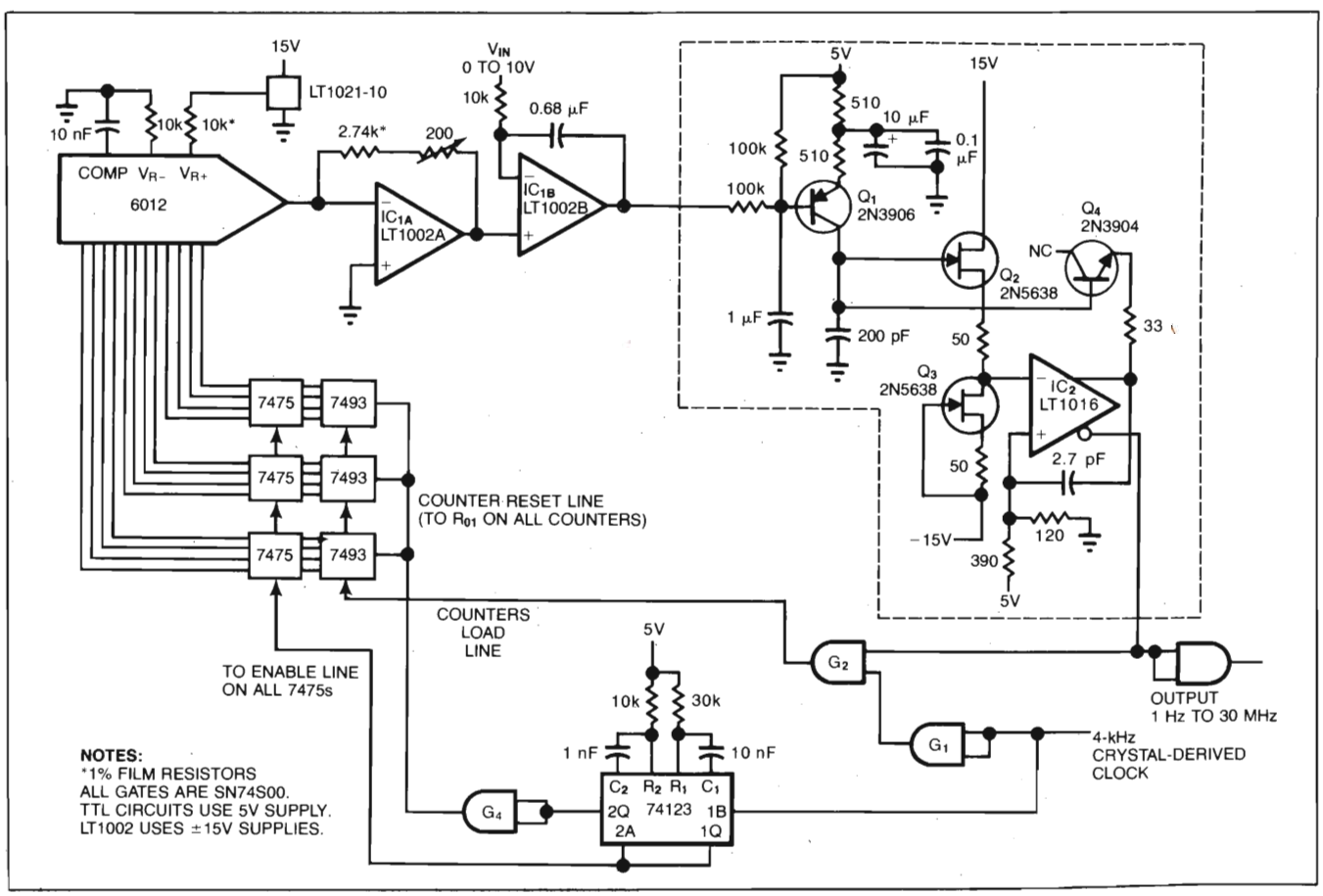


Fig 11—What's the limiting factor on frequency resolution *in this V/F converter, and what's the finest input-induced frequency change possible?*

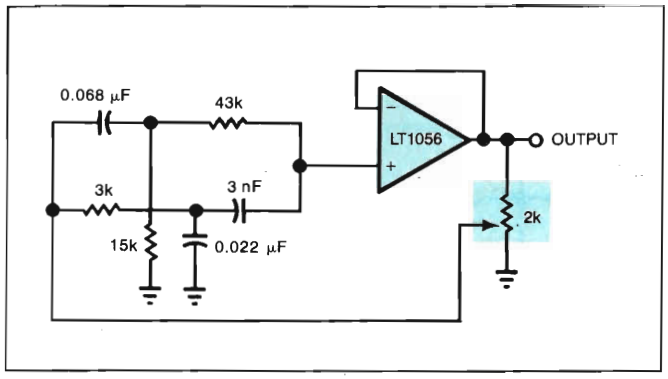


*Fig 12—**Predict the output** of this unity-gain voltage follower, and discuss the role of the potentiometer.*

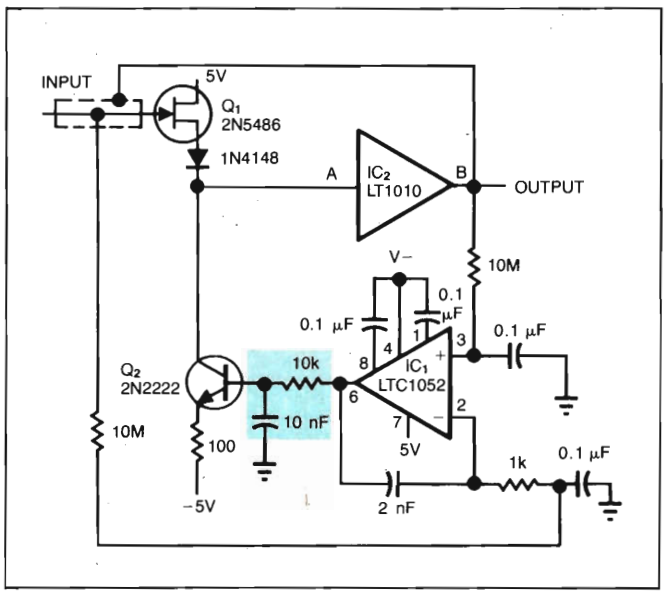


*Fig 13—**What's the role of the RC network** in this fast, dc-stabilized FET buffer?*

pares with the input voltage. IC_1's output status and the convert command gate IC_2's output pulses to the output. The circuit takes 16 msec to perform a full-scale conversion and draws 360 µA. It also has a large gain drift. Find the main source of this drift and correct it.

12. The broken lines in **Fig 11** enclose a crude V/F converter that operates over a 1-Hz to 30-MHz range. Although this simple circuit is fast, its linearity is poor and drift exceeds 5000 ppm/°C. The remaining components form a quartz-locked, sampled-data loop that corrects the deficiencies. The loop works by counting the number of pulses at the LT1016's output during a fixed interval and by then converting this pulse count to a voltage (with the aid of the D/A converter). This voltage is compared with the circuit's input voltage by an amplifier that drives the LT1016 V/F converter.

This closed-loop technique relies on the stability of the time interval and the digital-to-voltage conversion to achieve circuit stability. Frequent updating of the loop ensures long-term stability. What are the frequency-resolution limitations of this circuit, and why do they compromise resolution? What governs the smallest possible input-related frequency change increment?

13. The circuit in **Fig 12** is a unity-gain follower connected to a network of resistors and capacitors.

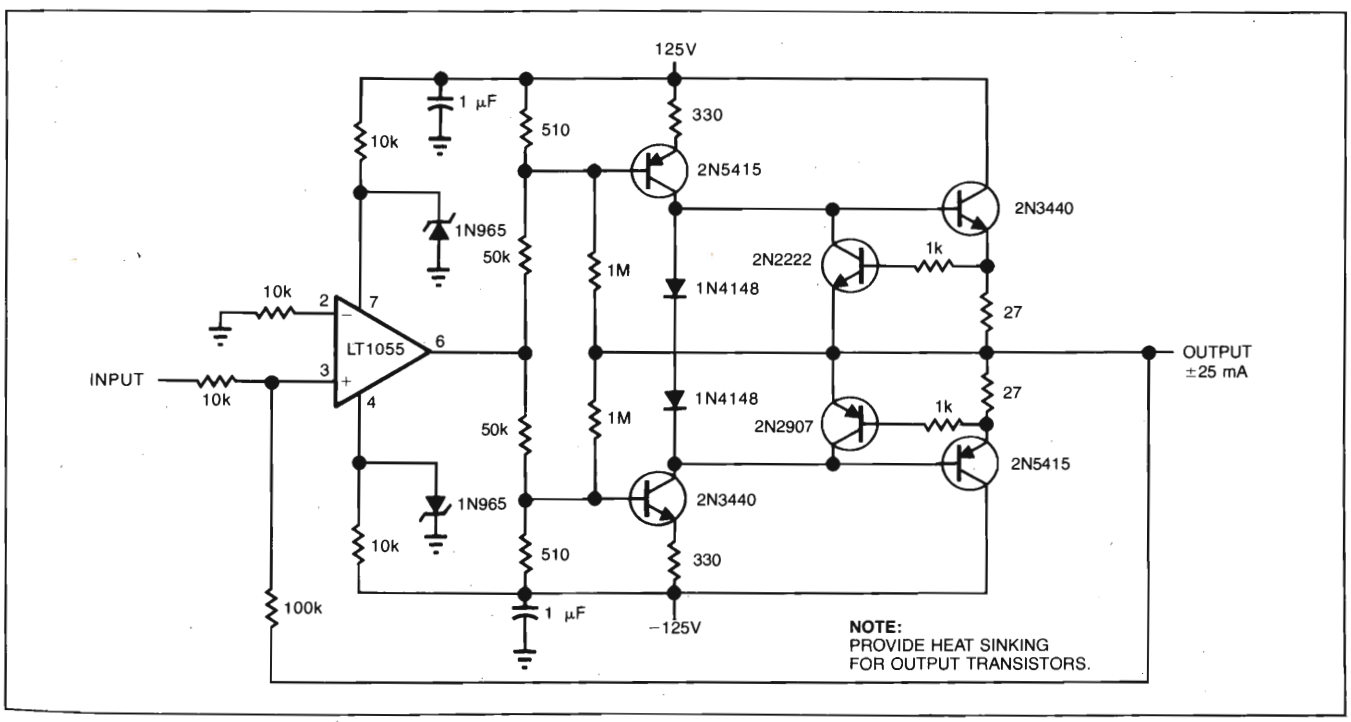


*Fig 14—**Add compensation** to this 240V p-p, FET-input operational amplifier. What are the limitations on the circuit's high-frequency response?*

Stable dc characteristics and extended high-frequency performance aren't necessarily mutually exclusive. Clever stabilization tricks let you obtain both.

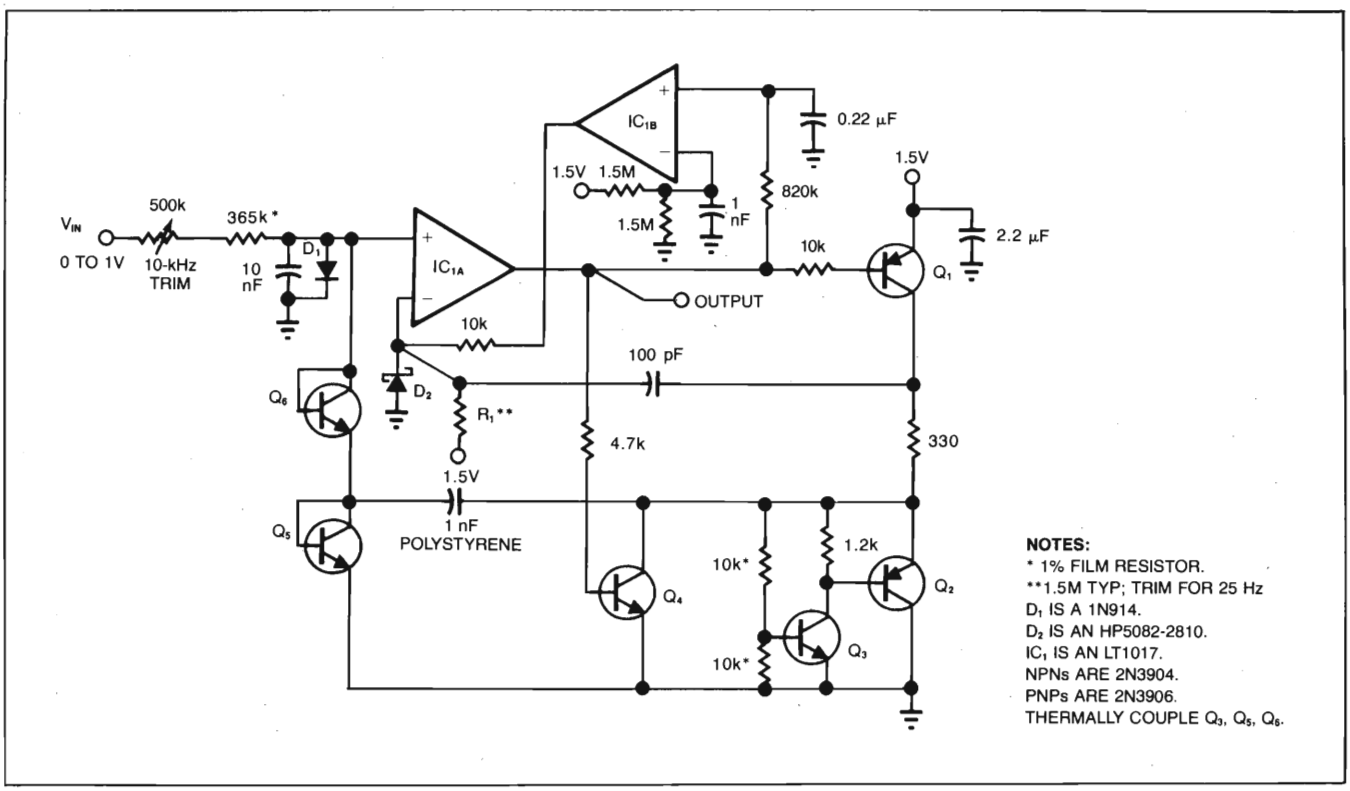


Fig 15—What's the approximate gain drift *in this V/F-converter circuit, and what are the primary contributors to the drift figure?*

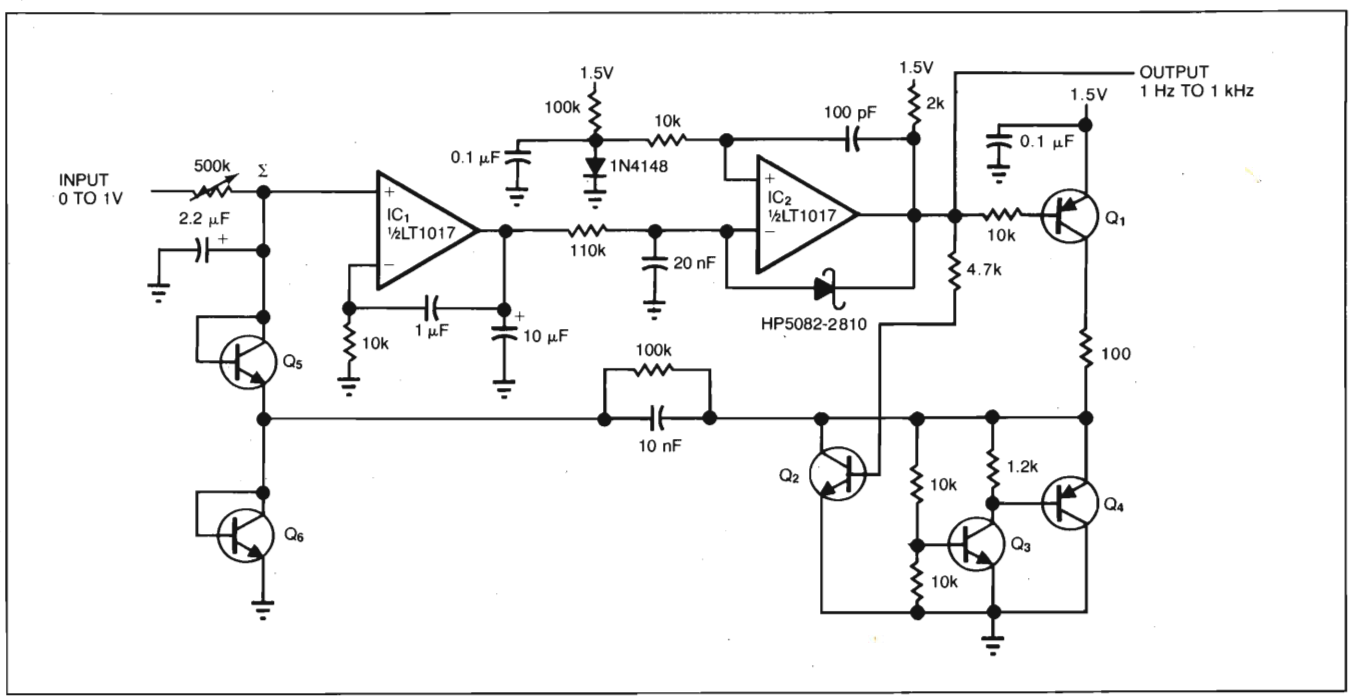


Fig 16—What's the secret *of this 1.5V-powered V/F converter's low current consumption, and what tradeoffs do you have to make to achieve such low consumption?*

It takes imagination and creativity to design linear circuitry that exploits the high speed and precision of modern linear ICs.

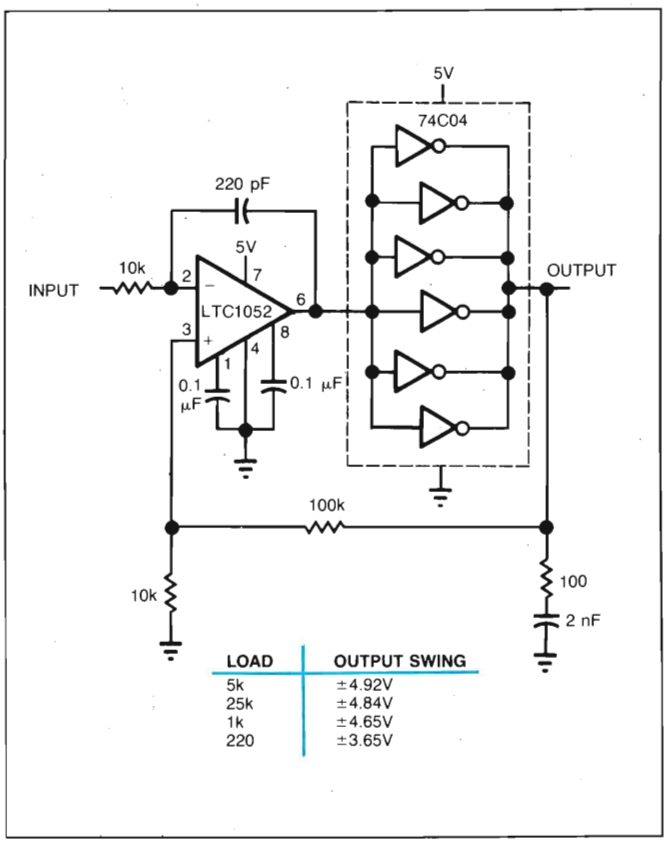


Fig 17—What are the power-supply constraints *in this CMOS-output, chopper-stabilized operational amplifier?*

What would you expect to see at the amplifier's output? What does the 2-kΩ potentiometer do?

14. **Fig 13** shows a fast, dc-stabilized, low-capacitance FET buffer. The FET, configured as a source follower, drives the LT1010 buffer. The LTC1052 chopper-stabilized amplifier compares the dc voltages at the input and output of the LT1010, and it forces (via Q_2) the FET's channel current to control circuit offset. What is the function of the 10-kΩ/10-nF RC combination?

15. The circuit in **Fig 14** has a ±120V-swing output stage connected to an input stage that uses an LT1055 FET op amp. The LT1055 has a 5-MHz gain-bandwidth product. Frequency compensation for this circuit is not shown. Put it in. What limits this circuit's high-frequency response?

16. The 1.5V-powered charge-pump V/F converter in **Fig 15** operates to 10 kHz. Which transistors must you thermally couple in order to obtain the best overall temperature coefficient in this circuit? Discuss the primary sources of gain drift in this configuration and estimate the gain temperature coefficient.

17. **Fig 16** shows another 1.5V-powered V/F converter. This circuit provides a 1-kHz full-scale output. It draws only 125 μA of supply current—almost seven times less than does the circuit in **Fig 15.** What makes this reduction possible? What tradeoffs does the current reduction entail?

18. CMOS inverters serve as an output stage for the

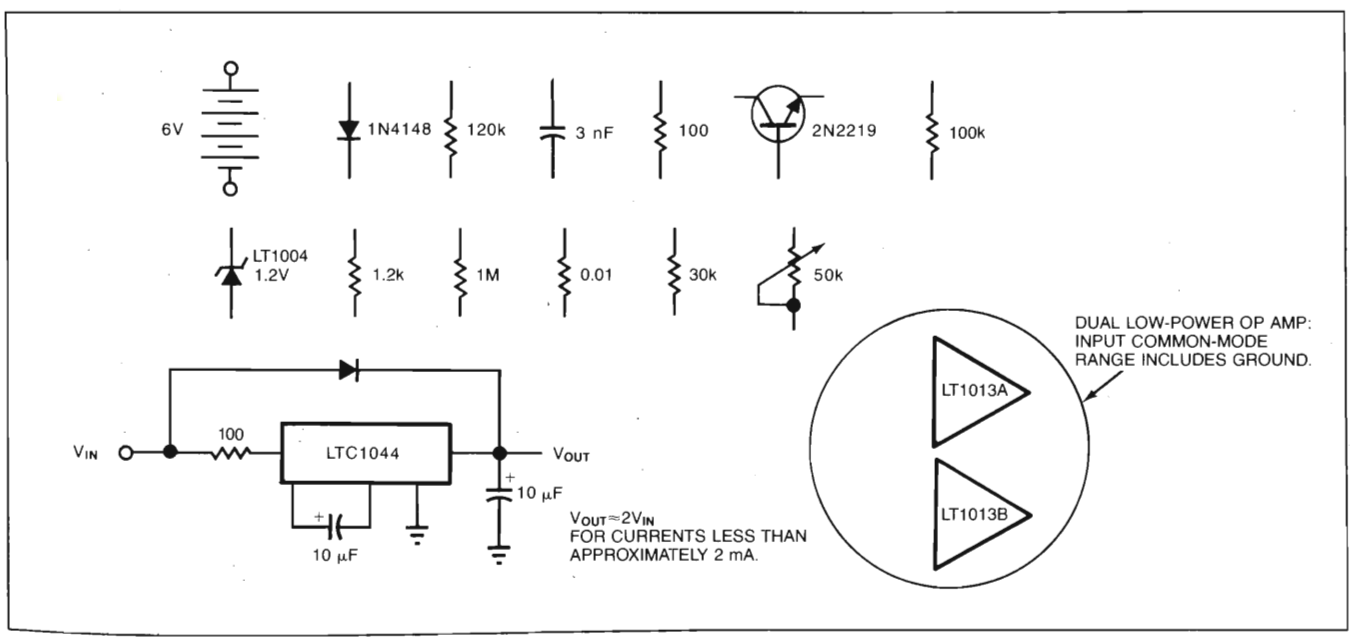


Fig 18—Use these building blocks *to design a low-dropout, 5V regulator. Be sure to include short-circuit current limiting.*

LTC1052 chopper-stabilized op amp in **Fig 17.** The damper network prevents oscillation, and the circuit works well as shown. Discuss power-supply restrictions —what supply voltages can you use in this circuit, and what voltages must you not use? Why?

19. Almost all low-dropout voltage regulators use pnp pass transistors. PNP-based designs provide low dropout, but they often have poor dynamic performance and relatively high quiescent currents. Using the components shown in **Fig 18,** construct a low-dropout, 5V regulator that operates from the 6V battery and provides 100-mA output. Include short-circuit limiting.

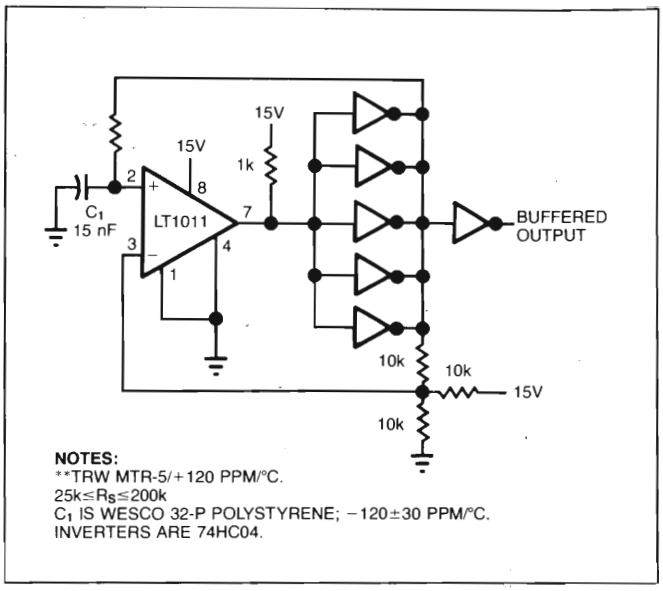


Fig 20—Analyze this RC oscillator. *Discuss the role of the CMOS inverters, the influence of comparator characteristics, the temperature-drift performance, and the influence of operating frequency on drift.*

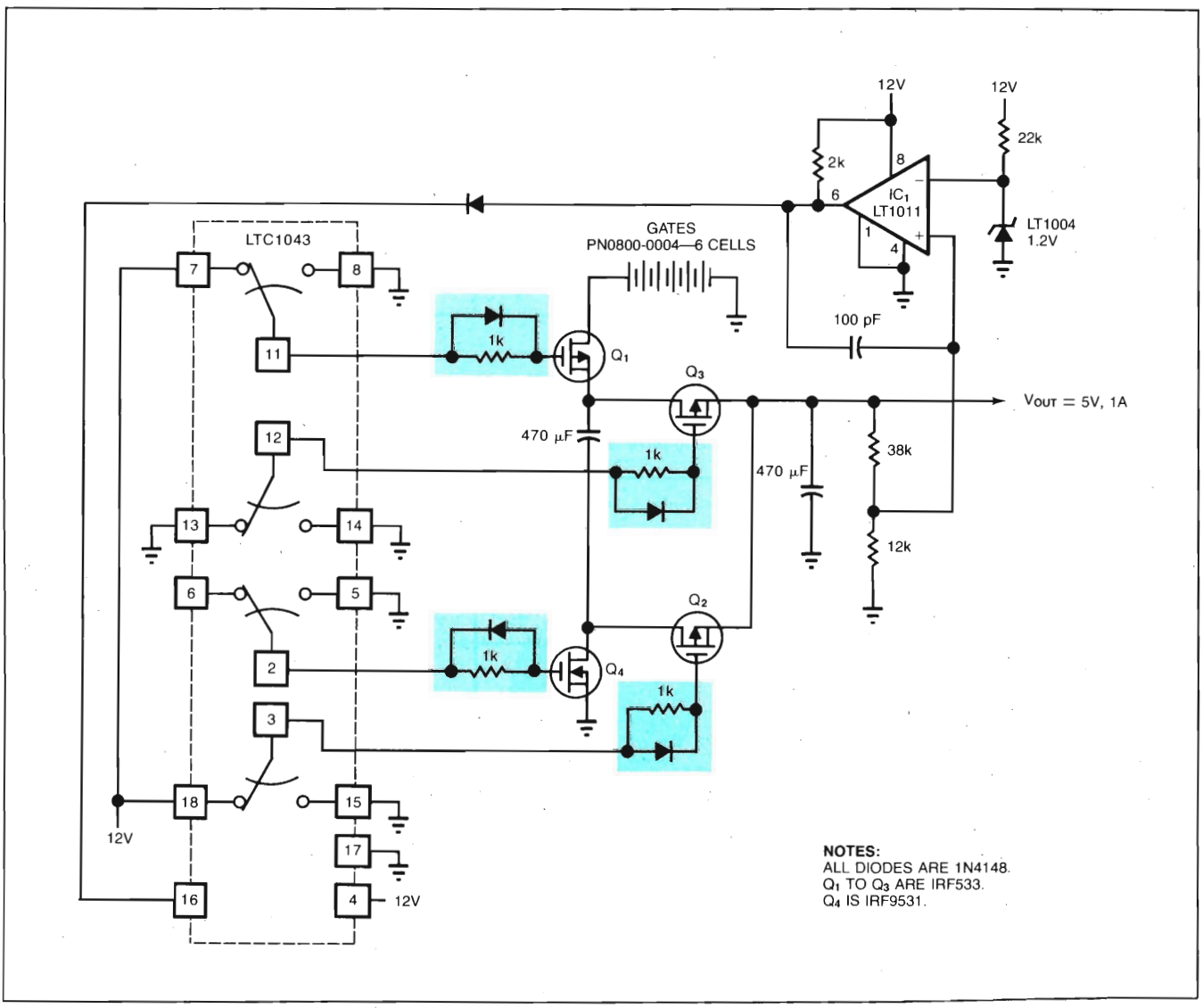


Fig 19—Discuss the roles of the diode-resistor networks *in this switched-capacitor voltage inverter. Why are the networks present, and how do they function?*

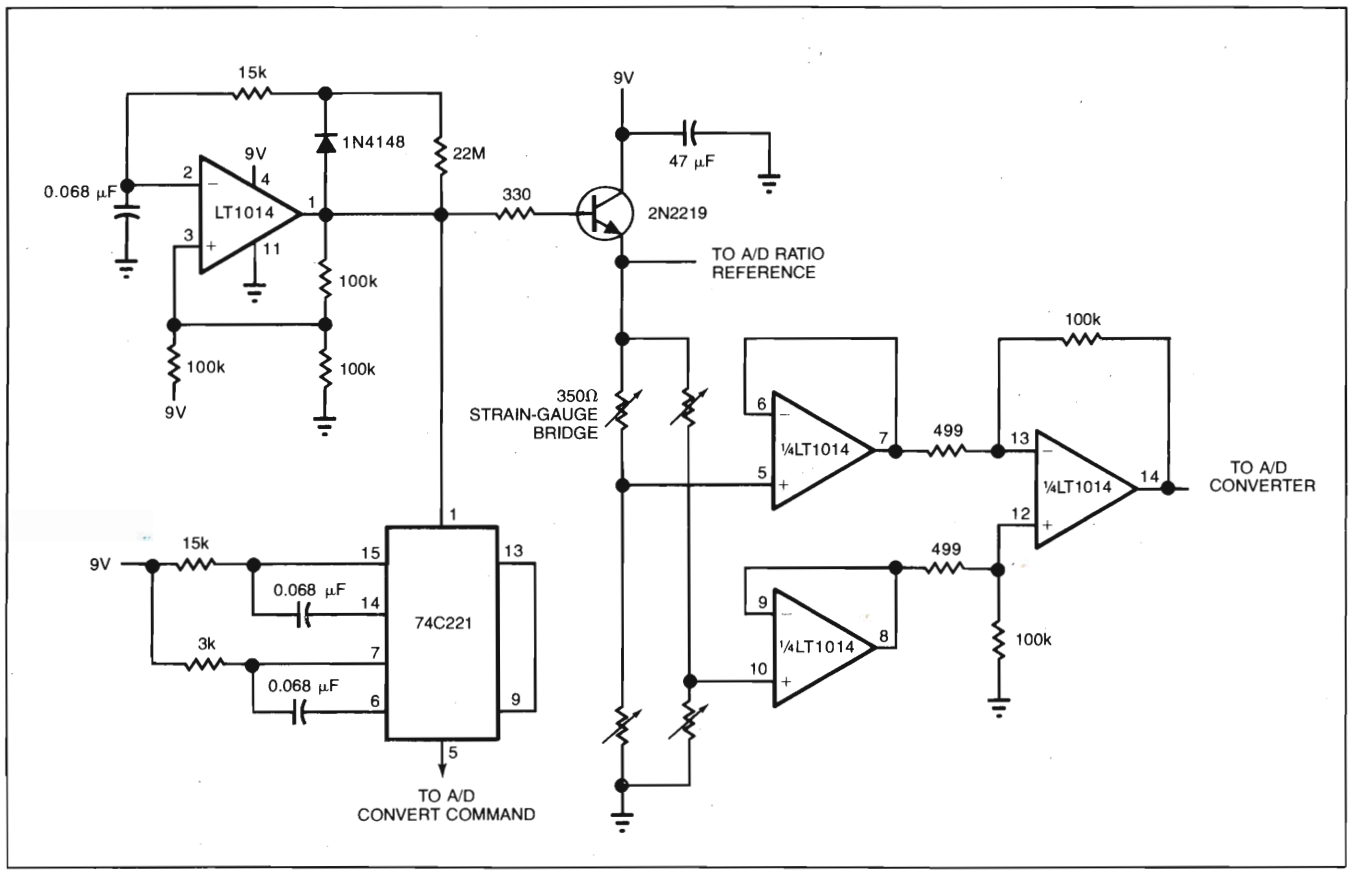


Fig 21—Can you find the subtle gremlin *that degrades long-term accuracy in this sampled-operation strain-gauge signal conditioner?*

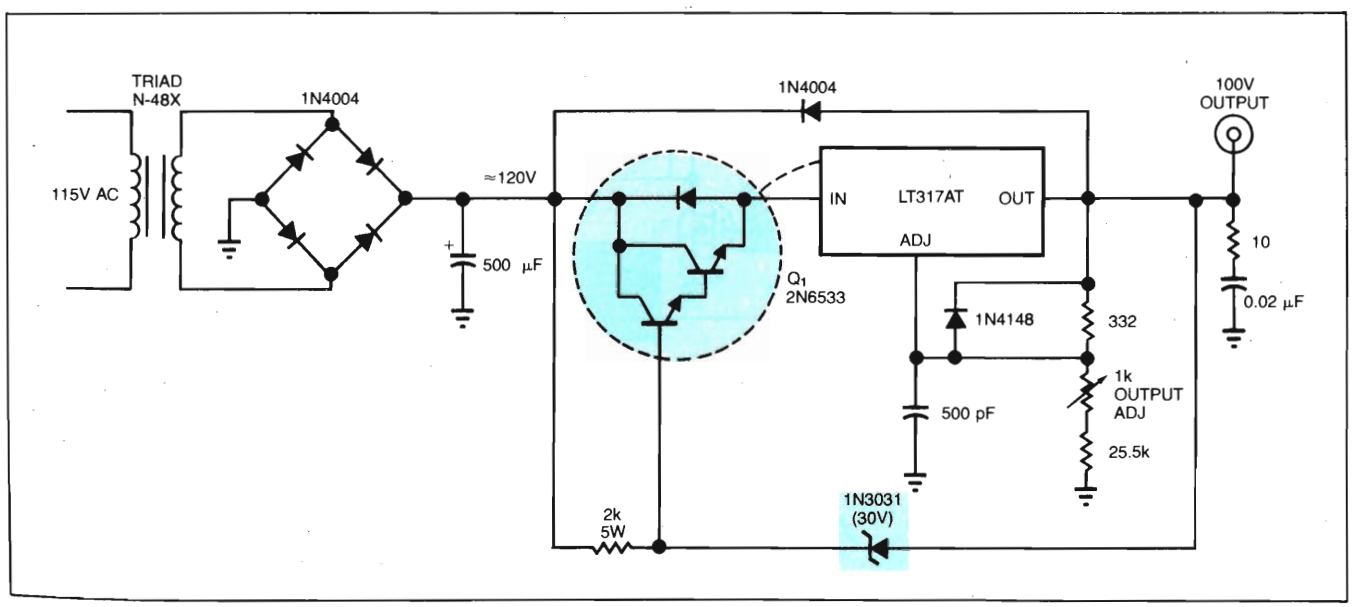


Fig 22—Discuss the roles of the transistor and the zener diode *in this high-voltage regulator. What characteristics must Q_1 have, and how does the transformer type you choose influence your selection of Q_1?*

Incorrect circuit configurations or poor choices of component values can render the best analog components worthless.

20. **Fig 19** shows a large-scale, switched-capacitor voltage converter. The self-clocked LTC1043 provides opposite-phase drive to the MOSFETs. The FETs are arranged so that the 470-μF capacitors are alternately placed in series and in parallel. When they're in series, the capacitors are charged; when you place them in parallel, they discharge into the load. IC_1 truncates the cycle, allowing the output to achieve a regulated 5V level. What do the diode/1-kΩ combinations do, and why?

21. The circuit in **Fig 20** is a low-drift RC oscillator. What do the CMOS inverters contribute? What effects do the comparator's characteristics have? Estimate the oscillator's drift performance. As the oscillator's operating frequency increases, what should happen to the drift, and why?

22. **Fig 21** shows a sampled-operation, strain-gauge signal conditioner. A low-frequency oscillator drives the strain bridge via the 2N2219, and the 3-op-amp instrumentation amplifier extracts the difference signal. The 74C221 one-shot multivibrator generates a delayed pulse that triggers a monitoring A/D converter. The low-frequency sampling yields low-power operation: Current drain is typically 650 μA. A subtle mechanism in this circuit, however, can degrade accuracy over time. What causes the accuracy degradation, and how can you correct the problem?

23. The circuit in **Fig 22** is a high-voltage regulator. What is the function of the 30V zener diode? For the regulator to work properly, what characteristics must Q_1 have? How does the transformer you select influence the type of transistor you select for Q_1?

24. The LM669 autozero IC in **Fig 23** continuously corrects offset drift in the LM11. It effects the correction by monitoring the LM11's summing-junction voltage, comparing this voltage with 0V, and then driving

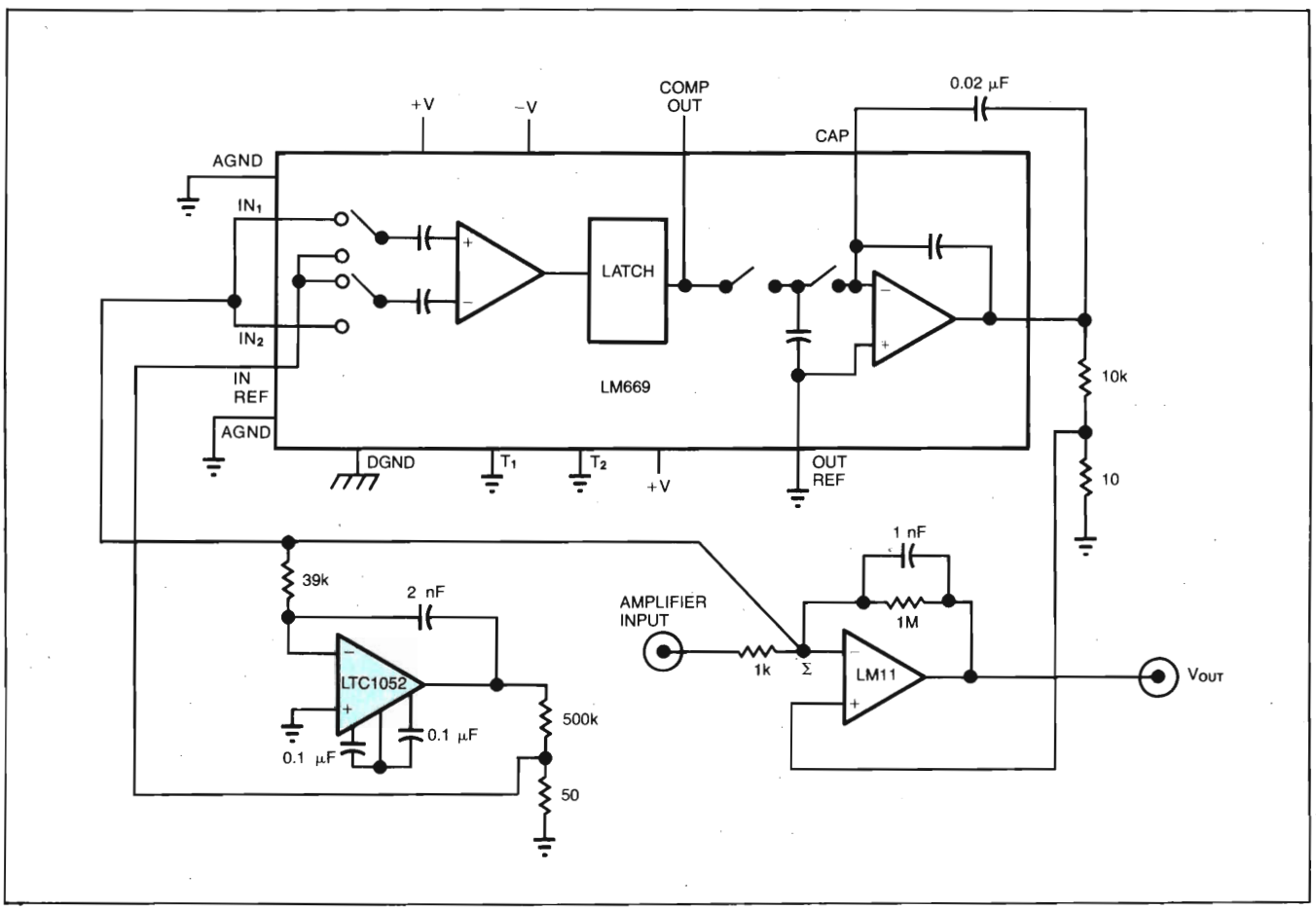


Fig 23—Perform simplification and power-reduction surgery *on this autozeroing circuit. What is the role of the LTC1052 chopper-stabilized operational amplifier?*

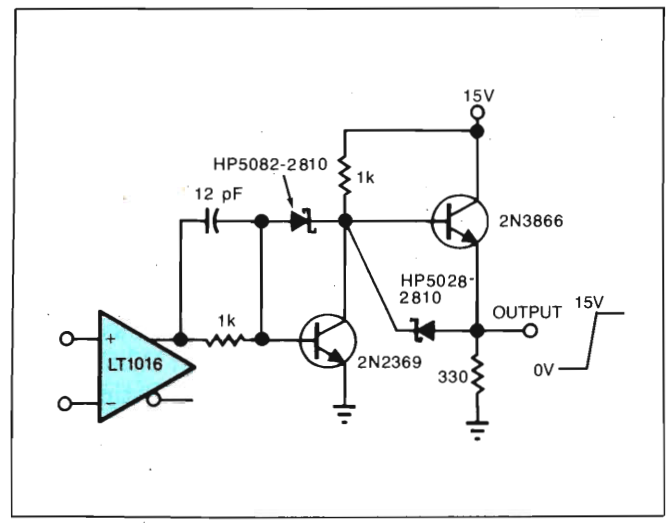


Fig 24—Halve the delay time *in the level-shifting circuit at the output of the LT1016 TTL-output comparator.*

the noninverting input to null the offset. The LM669 has a maximum error of 25 μV. What is the LTC1052 chopper-stabilized amplifier doing in the circuit? How could you simplify the circuit? How might you obtain power savings?

25. **Fig 24** shows a level shifter for a fast TTL-output comparator. The level shifter's delay is approximately 8 nsec. Show a simple way to cut this delay in half.

Score yourself

After you've answered the 25 questions, compare your responses with the ones presented on page 155. Note that, as in Part 1, the answers to Part 2 are sometimes incomplete, and they sometimes pose additional questions for your reflection. Finally, be sure to circle the appropriate number in the Article Interest Quotient. Your response will count heavily in the author's decision to work on another analog-IQ quiz, or to give in and study ones and zeros (heaven forbid!). **EDN**

Article Interest Quotient (Circle One)
High 476 Medium 477 Low 478

Build your own A/D converter for optimum performance

When you're faced with the task of solving an A/D-conversion problem, you can choose from a variety of off-the-shelf parts. In terms of performance, however, it might be better to build than to buy. By following some design guidelines, you can build your own high-speed 12-bit A/D converter.

Jim Williams, *Linear Technology Corp*

To economically achieve the best speed in an A/D converter, consider designing the part rather than buying it. Although you can choose from a variety of monolithic, hybrid, and modular SAR-based (successive-approximation-register-based) devices (the most popular technique employed in A/D-converter designs), such off-the-shelf solutions are generally either slower or more expensive than you'd prefer.

At the 12-bit conversion level, for example, the fastest monolithic devices spec conversion times of approximately 10 μsec. Modular and hybrid 12-bit converters can achieve 2-μsec conversion times, but such devices are expensive. By designing your own 12-bit A/D converter, you can build a device that solves both the conversion-speed and the cost problems.

Fig 1a shows a simple 12-bit, 12-μsec SAR converter. You'll find it easier to design faster converters if you understand this circuit's performance limitations. In **Fig 1b,** a clock signal (trace A) is applied to the 2504 SAR. On the rising edge of the start pulse (trace B), the SAR-D/A-converter combination begins to test each bit, starting with the MSB. Signal status at the LT1011's positive input (trace C) reflects this action. As shown, this waveform's voltage sequentially converges toward 0V as the SAR, D/A converter, and comparator provide servo control for the node.

The conversion-complete (CC) line (trace D) goes low after conversion of the LSB to signal the end of the sequence. The 7475 latch prevents the comparator from responding to input noise once the conversion is complete. This latch is reset at the next CC command.

Understanding some inherent limitations

When it comes to conversion speed, the D/A converter and the comparator are the major limiting factors in this circuit. For a worst-case, full-scale step, most bipolar D/A converters spec settling times of 150 to 200 nsec. In addition, the comparator's delay time comes into play. The clamp diodes limit excursions to speed comparator response, and the 820Ω resistor, which is

Successive-approximation A/D converters start with the MSB and work towards the LSB as they make each under/over decision.

connected to ground, shunts the D/A converter's output capacitance to speed comparator-D/A-converter node settling. Although this shunt degrades the voltage level per LSB available to the comparator, the LT1011's high gain compensates for that degradation.

In general, the circuit shown in **Fig 1a** is a fairly typical 12-bit SAR converter that features low cost and adequate speed. To realize higher conversion speeds, you'll need more sophisticated circuitry.

The circuit in **Fig 2a** uses a clock-modulation scheme to improve conversion speed. In this design, a 2-speed oscillator drives the clock terminal, CP. **Fig 2b** details circuit performance. A convert-command pulse (trace A) initiates the SAR routine. The pulse sets the 7474 flip-flop's $\overline{Q}$ output (trace C) high, which turns on Q_1. The 47- and 33-pF capacitors (part of oscillator IC_1's timing network) are now in parallel. IC_1's output pulses (trace B) drive the SAR's CP terminal.

The flip-flop resets after conversion of the third MSB (trace C). Q_1 turns off, and the clock oscillator increases its frequency (trace B). The higher clock frequency reduces dwell time per bit at the comparator-D/A-

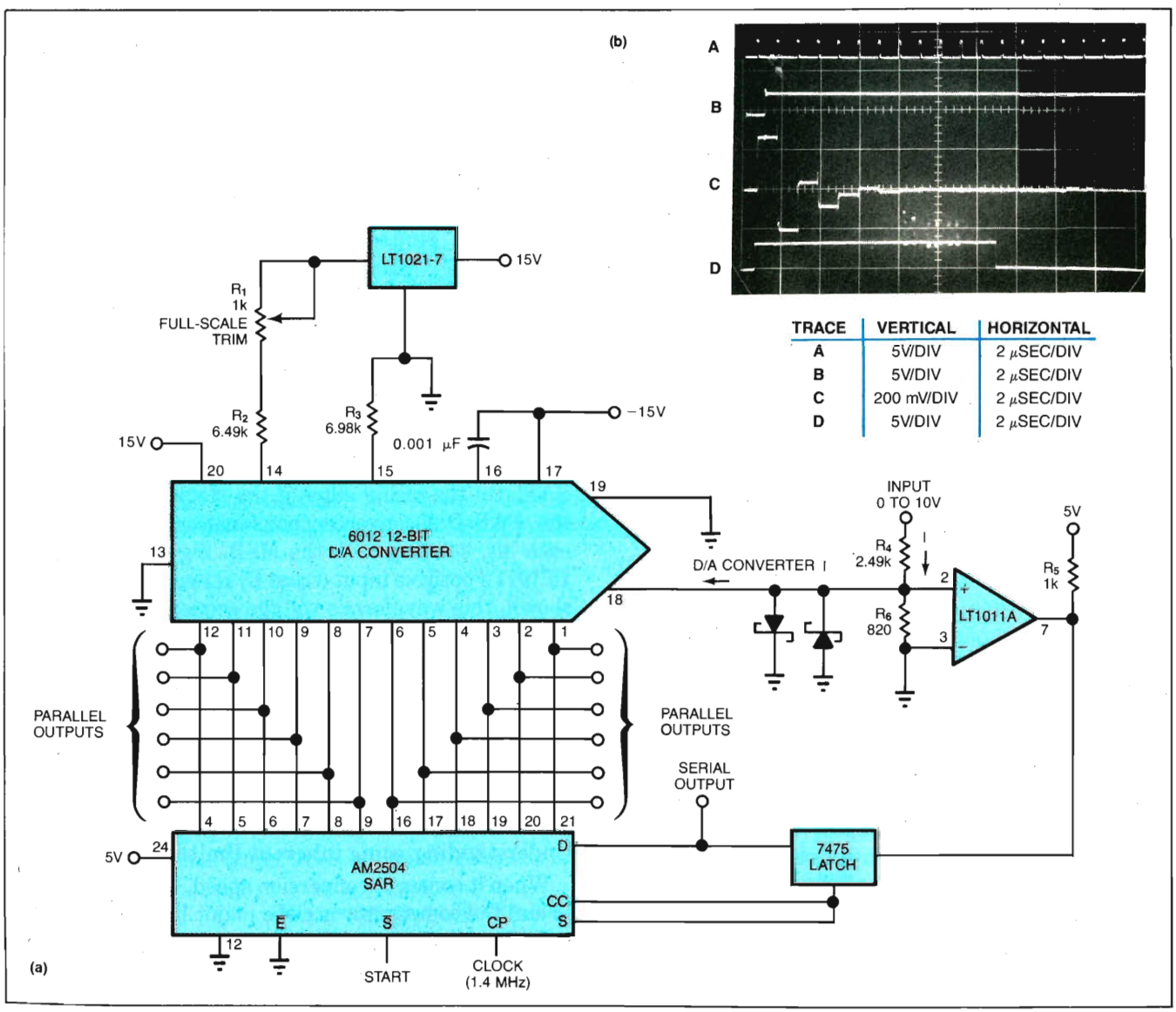
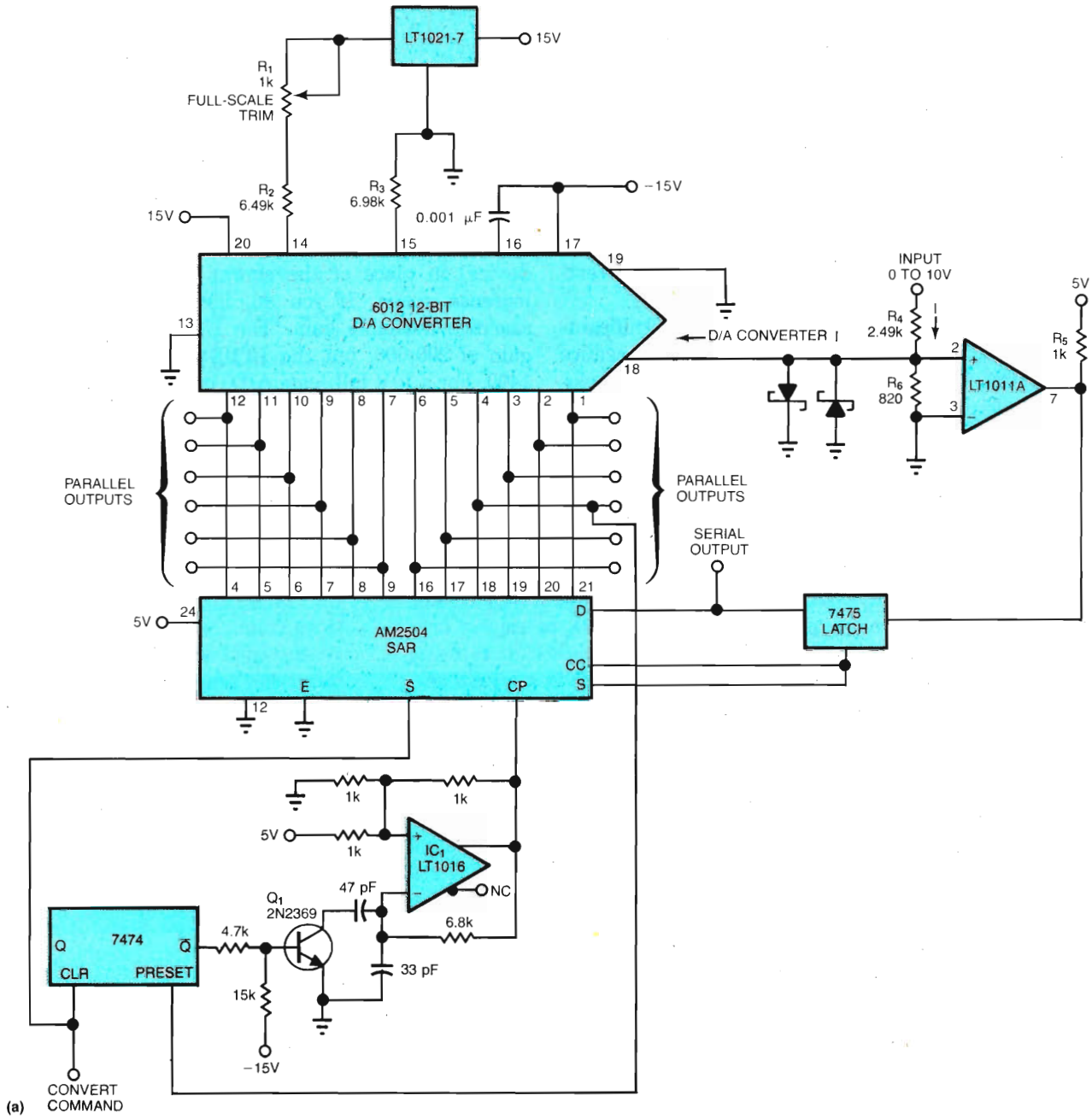
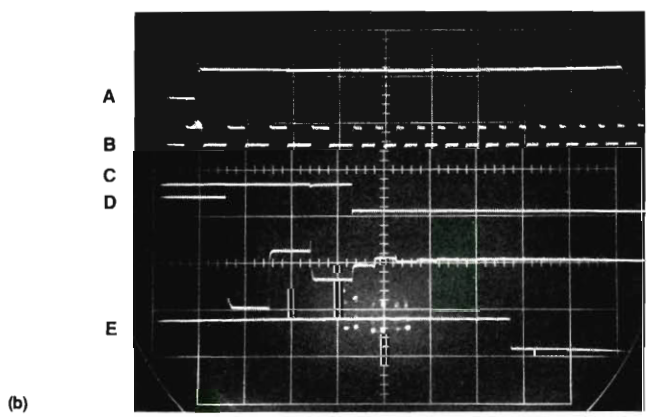


Fig 1—Designing fast converters becomes easier *when you understand the performance limitations of this simple 12-bit SAR design* ***(a).*** *In this case, both the D/A converter and the comparator limit circuit speed. The waveforms* ***(b)*** *reflect circuit operation.*





TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	1 µSEC/DIV
B	10V/DIV	1 µSEC/DIV
C	10V/DIV	1 µSEC/DIV
D	200 mV/DIV	1 µSEC/DIV
E	5V/DIV	1 µSEC/DIV

Fig 2—You can improve conversion speeds *by using a clock-modulation scheme* ***(a).*** *The circuit operation* ***(b)*** *shows that the flip-flop resets after conversion of the MSB bit (trace C), and oscillator frequency increases (trace B).*

Even when speed is not a prime design consideration, you may save money by building rather than buying an A/D converter.

converter junction (trace D), thereby decreasing total conversion time. As shown, the conversion-complete pulse (trace E) drops low 6.5 μsec after the convert-initiation command.

Although this clock-modulation approach significantly improves conversion speed, it does nothing to reduce the comparator's contribution to delay time. One solution to this problem is, of course, to use a faster comparator. But although the use of a faster comparator is a viable option at the 8-bit (or even the 10-bit) level, it causes problems at the 12-bit level.

For example, you could use an LT1016 (a 10-nsec device) in place of the slower (150-nsec) LT1011 to increase speed. If you do, however, you'll have to sacrifice available gain. The LT1011 has a minimum gain of 200,000, but the LT1016 specs a gain of only 1400. For a 10V full-scale A/D conversion, the LSB size is as follows:

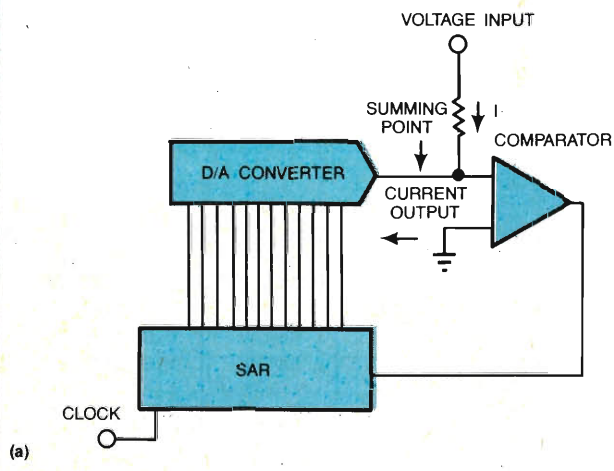
$$10V \div 4096 \text{ steps} = 2.44 \text{ mV}.$$

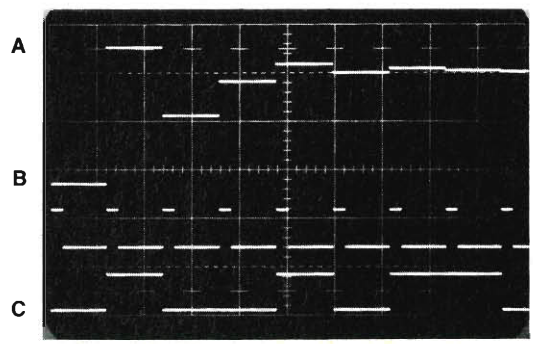
The successive-approximation technique

Use of the successive-approximation conversion technique probably dates to the invention of the weighing scale. In fact, you can most easily visualize this conversion technique by considering the operation of a beam balance.

With the beam balance, you determine an unknown weight held in one pan by successively placing standard weights in the other pan. The balance makes overweight/underweight decisions as you successively try standard weights (or combinations thereof) in a logical sequence to balance the scale.

Successive-approximation A/D converters start with the MSB and proceed towards the LSB after they make each under/over decision. Operation is straightforward (**Fig A**). Trace A shows the summing-node response as the converter, under instructions from the clock-driven successive-approximation logic (trace B), tries different bit weights. Trace C illustrates the comparator's decisions. Note how the summing point sequentially converges towards 0V—the analog of null in a beam balance.





(b)

TRACE	VERTICAL	HORIZONTAL
A	0.1V/DIV	20 μSEC/DIV
B	5V/DIV	20 μSEC/DIV
C	5V/DIV	20 μSEC/DIV

***Fig A—Operation is straightforward** in a SAR converter. As the converter, under control of the clock-driven SAR logic (trace B), tries different bit weights, the summing node response (trace A) sequentially converges towards 0. Trace C shows the comparator's decisions.*

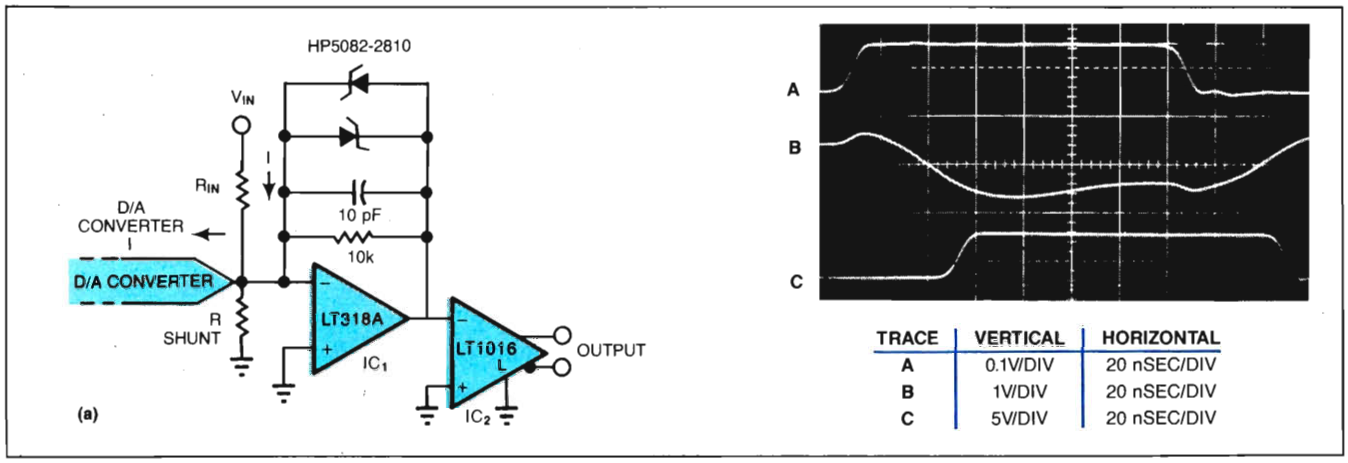


Fig 3—You can solve comparator gain problems *by using a simple preamplifier circuit* ***(a).*** *Although this is a fairly simple circuit, you can realize conversion times in the 3- to 5-μsec range* ***(b)*** *by using it in place of the LT1011 comparator.*

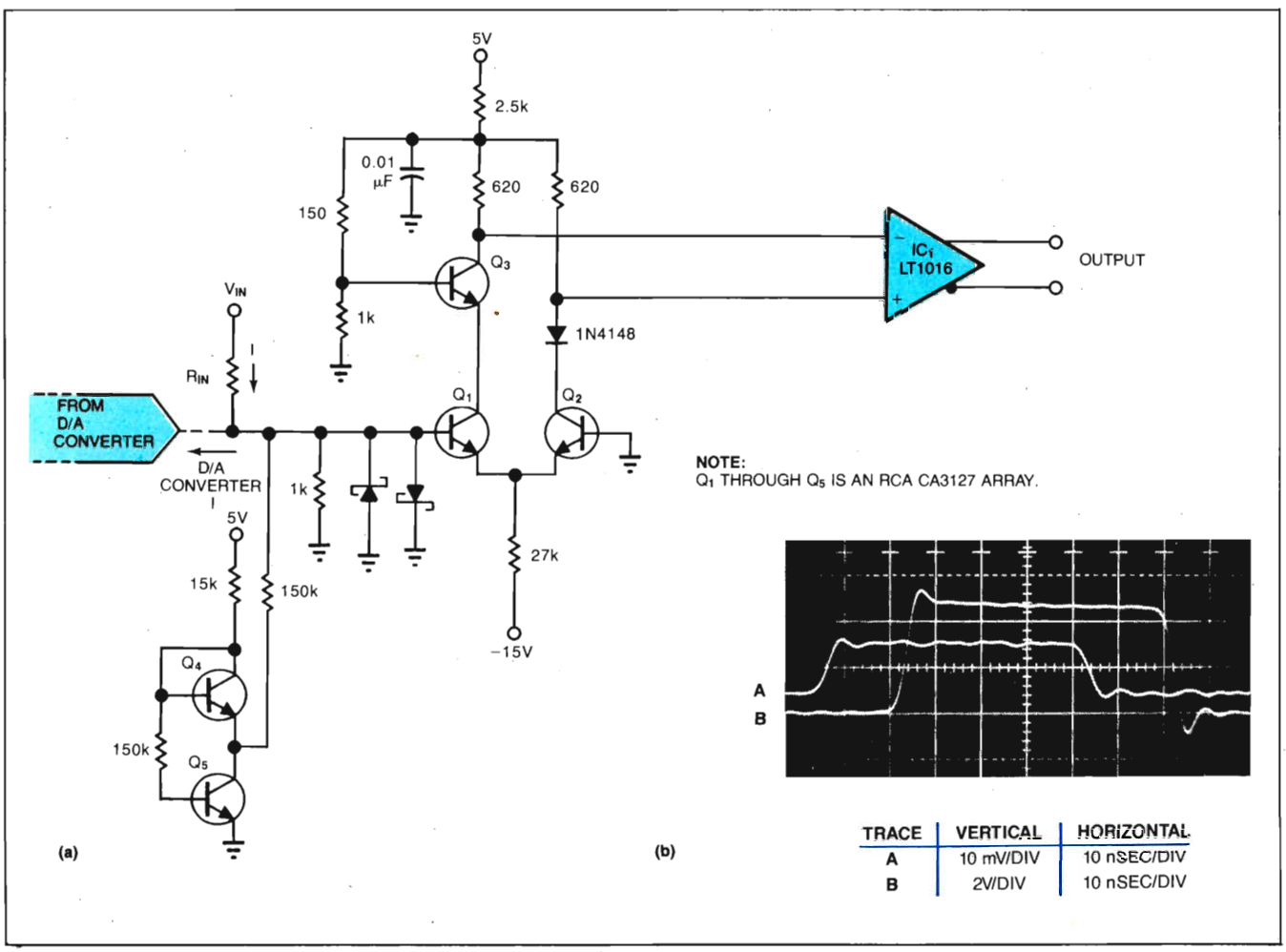


Fig 4—To minimize conversion times even further, *you can use high-frequency transistors to design a faster preamplifier* ***(a).*** *A look at the circuit's operating waveforms* ***(b)*** *shows that the circuit output (trace B) switches in 15 to 20 nsec.*

To increase conversion speed, you must place a gain stage before the comparator.

To switch a full TTL-output level with ½LSB overdrive (1.22 mV), the comparator must have a minimum gain as follows:

$$5V \div 1.22\ mV = 4098.$$

Given this gain requirement, the comparator clearly requires assistance. In addition, the shunt resistor at the D/A-converter output reduces the input signal, making the conversion task more difficult. Finally, comparator speed will suffer with such a low-level overdrive.

You can solve the gain problem by placing a gain stage in front of the comparator. Although this scheme adds delay, it provides the needed overdrive for the comparator.

Fig 3a shows a simple preamplifier circuit. The preamp-comparator combination provides adequate gain (typically 4 to 10) and an overall response time of 40 to 50 nsec. IC_1 is configured as an amplifier bounded by Schottky-diode clamps. The diodes improve response time by keeping IC_1 out of saturation when summing-point overdrive is excessive. The 10-pF ca-

Specifying the D/A converter

In choosing a D/A converter for use in SAR-based A/D-conversion applications, you should remember that speed is often important and that the D/A converter is the slowest part of the A/D converter. The selection process therefore requires careful consideration.

Given the high speed inherent in bipolar current-mode D/A converters, such devices are popular. You still have to specify carefully, however. The output capacitance of CMOS D/A converters—in the 100- to 150-pF range—can excessively extend summing-node settling times. Of course, monolithic bipolar D/A converters, whose output capacitance is about 30 pF, settle faster. Voltage-mode D/A converters, on the other hand, are unpopular candidates for SAR applications. They aren't required to achieve summing action, and they are substantially slower than current-output types.

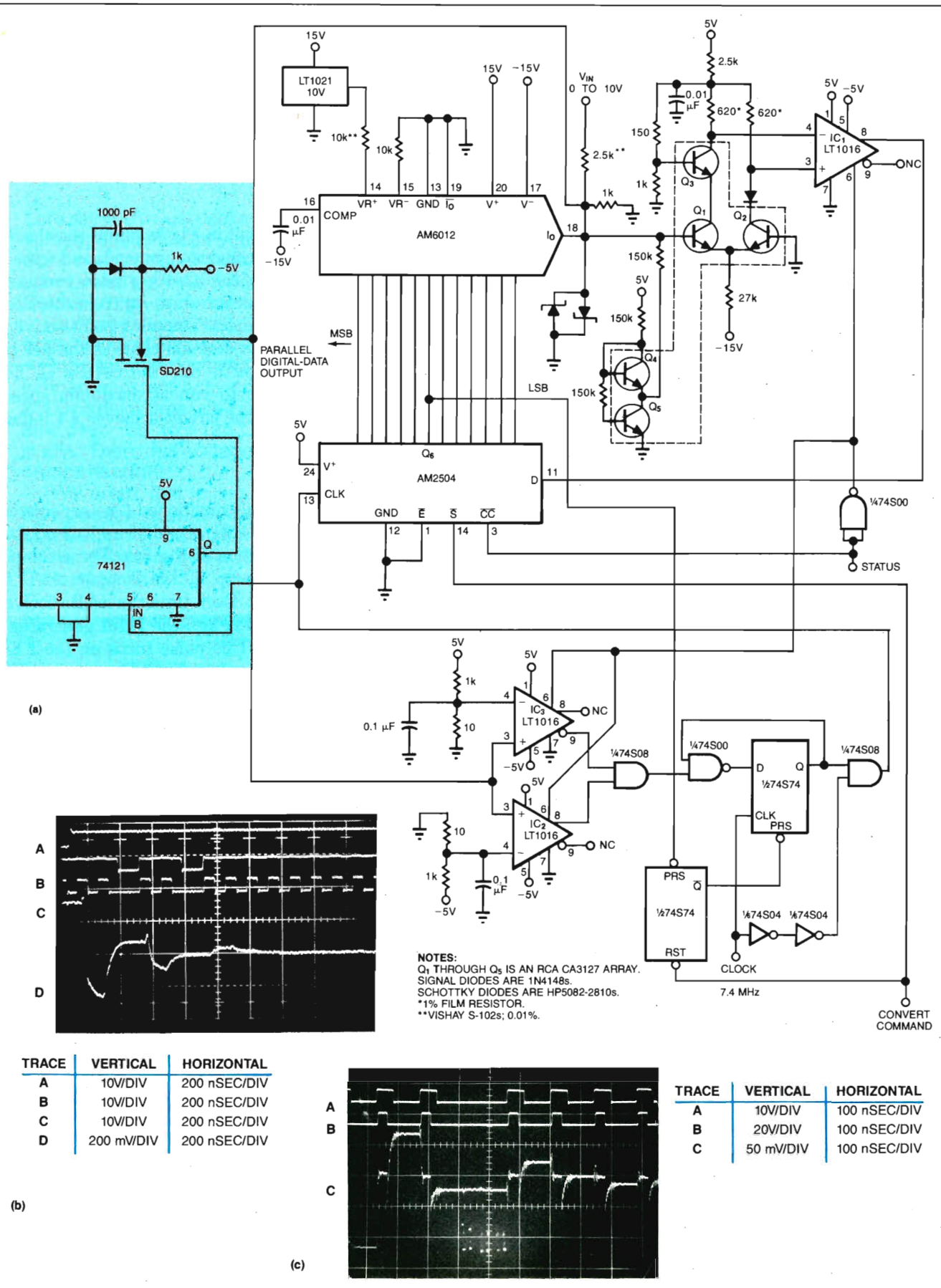
Extrapolate settling time

Settling-time specs for D/A converters are usually quoted for full-scale transitions. Smaller bit changes take less time, so you can extrapolate from full-scale settling time when you consider the D/A converter's effective settling time per bit in an A/D-conversion application. Unfortunately, the complex internal dynamics of a D/A converter rules out simple straight-line calculations; 1 LSB will not settle in $\frac{1}{12}$ of full-scale time in a 12-bit unit.

For moderate speeds, you can assume that each bit transition will require the full-scale settling time. This conservative approach will never get you into trouble, but it will almost certainly guarantee slower-than-necessary D/A-converter performance. The best way to find out just how far you can push the D/A converter's settling-time specs in an SAR application is to consult the manufacturer. You can also measure the settling time under conditions that reflect the application environment. (For circuits that you can readily adapt to measure D/A-converter settling time, see "Settling-time measurements demand precise test circuitry," EDN, November 15, 1984, pg 307.)

Considering the variety of D/A converters available, each with individual termination requirements, measurement results will vary considerably. In addition, the dynamics of D/A-converter types can vary substantially among manufacturers. It is possible, however, to provide some guidelines on what to expect. For example, the popular 565A, with a full-scale settling time of 250 nsec into 0Ω, can achieve a per-bit effective settling time of 110 to 150 nsec with careful design techniques.

Speed is not the only concern. A D/A converter's dc specifications translate directly into A/D-converter error terms. Linearity, drift, accuracy, and other dc terms contribute on a 1:1 basis to the converter's error characteristics. Monotonicity contributes as well. In a worst-case situation, a nonmonotonic D/A converter will cause an A/D converter to miss some output codes under certain input conditions.



TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	200 nSEC/DIV
B	10V/DIV	200 nSEC/DIV
C	10V/DIV	200 nSEC/DIV
D	200 mV/DIV	200 nSEC/DIV

(b)

(c)

TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	100 nSEC/DIV
B	20V/DIV	100 nSEC/DIV
C	50 mV/DIV	100 nSEC/DIV

Fig 5—Primary speed-enhancing features *in this 12-bit SAR converter* ***(a)*** *include a closed-loop clock-control scheme and active summing-node clamping. Using a closed-loop clocking scheme, the circuit achieves a 1.9-µsec conversion time* ***(b)****. When you include the active summing-node clamp circuitry (the shaded portion of* ***a****), circuit conversion time is 1.8 µsec* ***(c)****.*

By combining closed-loop clock control with active summing-node clamping, you can enhance conversion speeds.

pacitor (a typical value in this case) compensates for the D/A converter's output capacitance. The capacitance value is application dependent, so you should use a value that provides the best amplifier damping. The feedback resistor (10 kΩ in this example) is selected for best gain-bandwidth performance.

As **Fig 3b** shows, a test input pulse (trace A) causes IC_1's output to slew through 0V (trace B), developing a negative bias level at IC_2's input. After a 10-nsec delay, IC_2 generates a clean TTL output (trace C).

Despite its simplicity, this circuit can significantly improve comparison speed. Use it in place of the LT1011 in **Fig 2a,** and you can realize conversion times in the 3- to 5-μsec range. If these conversion times are still too slow, you can use high-frequency transistors (at the GHz level) and design a faster discrete preamplifier **(Fig 4a)** to drive the LT1016 comparator.

In this cascoded differential amplifier, Q_4 and Q_5 provide bias-current compensation for Q_1's base current. **Fig 4b** illustrates how the circuit performs when you apply a test input signal (trace A). As shown, the LT1016's output (trace B) switches in 15 to 20 nsec. The LT1016 causes about 10 nsec of this delay; the preamp contributes the rest.

Preamplify for better speed

You can put this discrete preamplifier to good use in a high-speed 12-bit SAR converter (Fig 5a). Closed-loop clock control and active summing-node clamping are the primary speed-enhancing features. This circuit will perform a full 12-bit conversion in 1.8 μsec—about the practical limit with off-the-shelf components.

Conceptually, this circuit is similar to that in **Fig 2a.** However, the high-speed discrete preamplifier replaces the LT1011, and digital logic controls the clock speed. In this instance, the clock rate accelerates after conversion of the fifth MSB. During conversion of the upper four bits, a closed loop controls the clock rate to maximize overall speed.

The closed loop monitors conditions at the comparator-D/A-converter summing node. If the summing-node voltage excursion is greater than ±50 mV, the SAR operates at the maximum clock rate. If the excursion at the node is less than ±50 mV, the loop retards the clock rate to provide adequate settling time. The clock loop enhances conversion-time performance by not waiting for the bits that won't settle within ±50 mV. IC_2 and IC_3 form a high-speed window comparator that provides digital summing-node information to the clock logic.

Fig 5b details the performance of the closed-loop clocking scheme (the circuit in **Fig 5a** minus the shaded portion). Trace A is the convert command, and trace B shows the gated output of the IC_2-IC_3 window comparator. The comparator's output state controls the clock line (trace C). Trace D depicts summing-point activity. The window comparator's decision controls the per-bit dwell time. After the fifth bit, the SAR's Q_6 line instructs the clock logic to run at maximum speed. Under these conditions, the circuit achieves a 1.9-μsec conversion time.

Converting still faster

To achieve the previously mentioned 1.8-μsec conversion time, include the 74121 one-shot and associated circuitry (the shaded portion of **Fig 5a).** These components form an active clamp at the comparator-D/A-converter summing node. Each time the SAR receives a clock pulse (trace A in **Fig 5c),** the 74121 generates a 30-nsec pulse (trace B). This pulse turns on the FET and shunts the summing node (trace C) to ground. The FET's low on-resistance discharges the D/A converter's 30-pF output capacitance for 30 nsec to reduce the converter's settling time. Each SAR-conversion step resets the summing node to 0. When the one-shot changes state, the node settles to its final value. This active clamping technique provides about a 10-nsec/bit savings in conversion time.

The 1.8-μsec conversion time provided by the circuit in **Fig 5a** approaches the practical limit for a 12-bit SAR converter. The effective D/A-converter settling time is about 100 nsec/bit. Comparator/preamp delay is about 20 nsec/bit, and SAR chip delays are about 25 nsec/bit.

EDN

Author's biography

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and -instrumentation design. He has served in related capacities at National Semiconductor Corp, Arthur D Little Inc, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art, and collecting antique scientific instruments.

Composite amplifiers yield high speed and low offset

You can find an op-amp technology that excels in any one performance area, but today's applications often demand high performance in several areas. You must therefore employ some ingenious circuit-design techniques to circumvent the limitations.

Jim Williams, *Linear Technology Corp*

Amplifier design is a study in compromise: A single device can't achieve optimal speed, drift, bias-current, noise, and output-power specs. Various families emphasizing one or more of these areas have evolved, but you might find that your application requires performance figures that can only be obtained with dedicated designs. If a single device can't provide the desired characteristics (high speed and dc precision, for example), you can configure a composite amplifier to do the job. Composite designs combine the best features of two or more amplifiers to achieve a level of performance unobtainable in a single device.

Fig 1 shows a composite amplifier made up of an LT1012 low-drift device and an LT1022 high-speed device. The overall circuit is a unity-gain inverter whose summing node is located at the junction of the three 10-kΩ resistors. The LT1012 monitors this summing node, compares it to ground, and drives the LT1022's positive input, completing a dc-stabilizing loop around the LT1022. The 10-kΩ/300-pF network allows the LT1012 to respond only to low-frequency signals; the LT1022 handles high-frequency inputs while the LT1012 stabilizes the dc operating point.

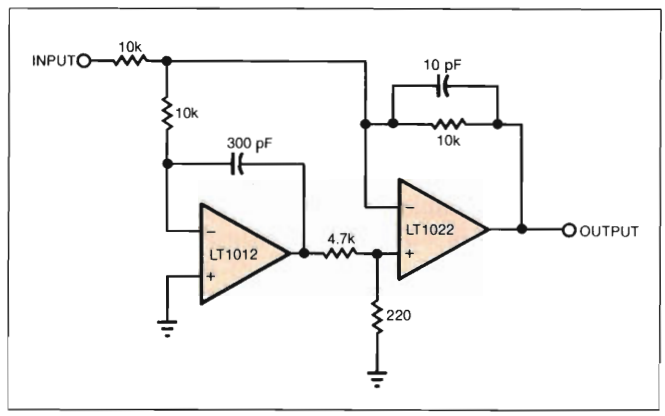


***Fig 1—This composite circuit combines low-drift and high-gain devices** to form a unity-gain inverter. The LT1022 handles high-frequency inputs, while the LT1012 stabilizes the dc operating point.*

The 4.7-kΩ/220Ω divider at the noninverting input of the LT1022 prevents excessive input overdrive during start-up. The circuit's performance combines the LT1012's 35-μV offset and 1.5V/°C drift with the LT1022's 23V/μsec slew rate and 300-kHz full-power bandwidth. The bias current is approximately 100 pA.

Fig 2's circuit is similar to **Fig 1**'s, but the former employs discrete FETs to more than triple the speed. In the circuit, IC_1's inputs are tied to the negative rail,

thereby turning IC_1's input stage off. The differentially connected FETs bias the second stage via IC_1's offset pins. This connection replaces IC_1's input stage, reducing bias current and increasing speed.

FET mismatch would normally result in excessive offset and drift, but IC_2 corrects this problem by monitoring the summing point (the junction of the two 4.7-kΩ resistors) and forcing Q_2's gate to eliminate the overall offset. The 10-kΩ/1000-pF network inhibits IC_2's response to low frequencies, and the 1-kΩ divider chain prevents overdrive to Q_2 on start-up. The 1-kΩ/10-pF damper network at the summing node helps ensure high-frequency stability. **Fig 2b** shows the pulse response; trace A is the input, and trace B is the output.

The slew rate exceeds 100V/μsec with clean damping. The full-power bandwidth is about 1 MHz, and the input bias current is approximately 100 pA. DC offset and drift specs are similar to those of the **Fig 1** circuit.

Unity-gain buffer for high impedance

Fig 3 shows a highly stable unity-gain buffer with good speed and high input impedance. Q_1 and Q_2 constitute a simple high-speed FET-input buffer. Q_1 functions as a source follower, with the Q_2 current-source load setting the drain-source channel current. The LT1010 buffer can drive cables or other loads.

Normally, this open-loop configuration would be quite drifty because of the lack of dc feedback. The LTC1052 contributes the needed stability by comparing the filtered circuit output with a similarly filtered version of the input signal. The amplified difference between these signals sets Q_2's bias and hence Q_1's channel current, which in turn forces Q_1's V_{GS} to the level required to match the circuit's input and output potentials. The 2000-pF capacitor at IC_1 provides stable loop compensation. The RC network at IC_1's output prevents that output from seeing high-speed edges coupled through Q_2's collector-base junction. IC_2's output is also fed back to the shield around Q_1's gate lead, bootstrapping the circuit's effective input capacitance down to less than 1 pF.

The LT1010's 15-MHz bandwidth and 100V/μsec slew rate, combined with its 150-mA output capability, ensure that the circuit in **Fig 3a** is fast enough for most applications. For applications requiring very fast performance, the alternate discrete-component buffer in **Fig 3b** should prove useful. Although its output is current-limited at 75 mA, the gigahertz-range transistors that the buffer employs provide an exceptionally wide bandwidth, fast slewing, and very little delay. **Fig 3c** shows the LTC1052-stabilized buffer circuit's response using the discrete stage: The response is clean and quick; the delay is less than 4 nsec; the slew rate exceeds 2000V/μsec; and the full-power bandwidth approaches 50 MHz. Note in **Fig 3c** that the rise time is limited by the pulse generator, not by the circuit. The offset, with or without the discrete-component stage, is set at 5 μV by the LTC1052; the gain is about 0.95.

This last spec points out a factor that could lead to potential difficulty with the **Fig 3** circuits: The gain is not quite unity. The circuit in **Fig 4** maintains a high speed and low bias current while achieving a true unity-gain transfer function.

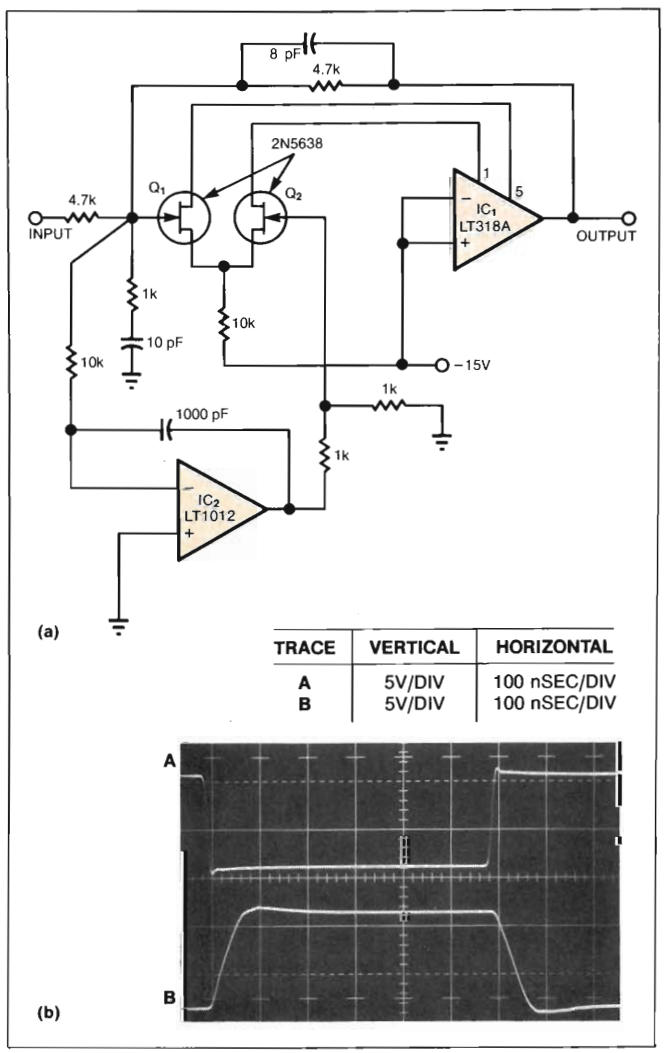


Fig 2—Otherwise similar to the Fig 1 circuit, *this composite amplifier* ***(a)*** *employs discrete FETs to achieve a threefold speed improvement. The scope photo* ***(b)*** *illustrates the circuit's pulse response.*

The use of discrete FETs can effect a three-fold improvement in a composite amplifier's speed.

In **Fig 4**'s circuit, IC_2 provides dc stability for the I/O path, and IC_1 provides drive capability. Feedback is to Q_2's emitter from IC_1's output. The 1-kΩ adjustment allows precise setting of the gain to unity. With the LT1010 serving as the final output stage, the slew rate is 100V/μsec and the full-power bandwidth (1V p-p) is 10 MHz. The −3-dB bandwidth exceeds 35 MHz. For a gain of A=10 (that is, when the 1-kΩ variable resistor is set at 50Ω), the full-power bandwidth remains at 10 MHz, but the −3-dB bandwidth falls to 22 MHz.

If you include the optional discrete stage, the slew rate exceeds 1000V/μsec, the full-power bandwidth extends to 18 MHz, and the −3-dB bandwidth reaches 58 MHz. For A=10, full power is available to 10 MHz; the −3-dB point becomes 36 MHz. In **Fig 4c**, traces A and B show the input and output without the discrete stage; traces C and D show the input and output with the discrete stage. With or without the discrete stage, the circuit should be more than adequate for driving video cables or data converters; the LT1012 maintains dc stability under all conditions.

Fast amplifier delivers 1V p-p

Fig 5 shows another dc-stabilized fast amplifier that functions over a wide range of gains (typically from 1 to 10). It combines the LT1010 and a fast discrete stage within LT1008-based stabilizing loop. Q_1 and Q_2 form a differential stage that provides a single-ended input into the LT1010. The circuit delivers 1V p-p into a typical 75Ω video load. At A=2, the gain is within 0.5

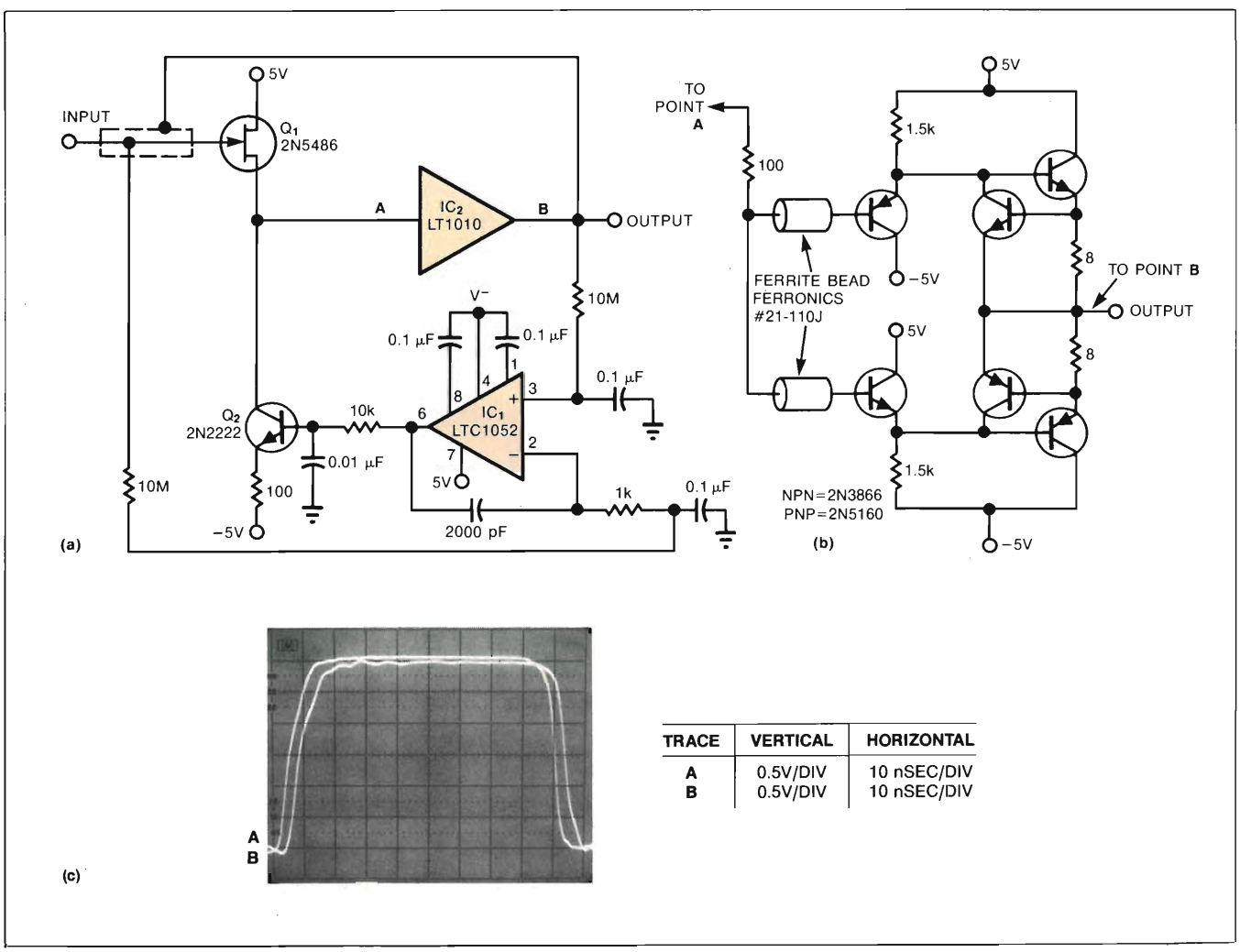
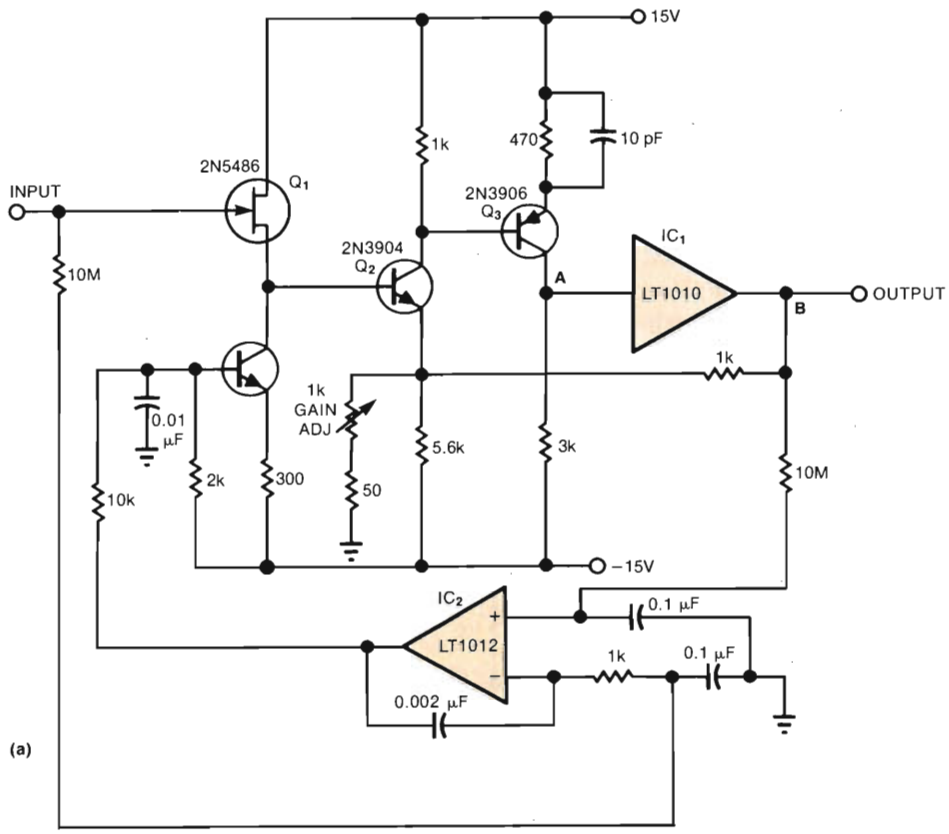
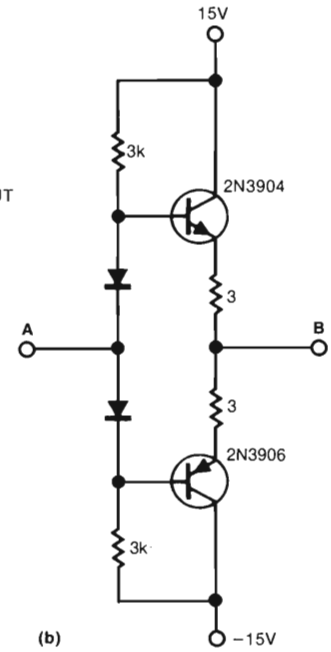
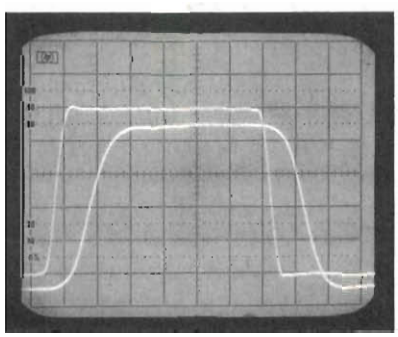
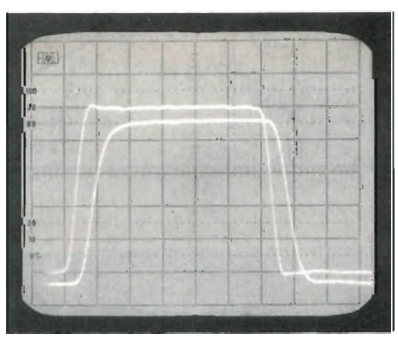


Fig 3—A FET input stage ensures high input impedance for this not-quite-unity-gain buffer (a). *The LTC1052 contributes stability. A discrete-component output stage* ***(b)*** *increases the circuit's already impressive speed. The response is clean and quick* ***(c).***









(c)

TRACE	VERTICAL	HORIZONTAL
A	0.2V/DIV	10 nSEC/DIV
B	0.2V/DIV	10 nSEC/DIV
C	0.2V/DIV	10 nSEC/DIV
D	0.2V/DIV	10 nSEC/DIV

Fig 4—This circuit (a) is somewhat similar to Fig 3's, *but it has the additional advantage of achieving a true unity-gain transfer function. The optional discrete stage* ***(b)*** *extends the full-power bandwidth from 10 to 18 MHz. In the scope photos* ***(c),*** *traces A and B show the input and output without the discrete stage; traces C and D show the input and output with the discrete stage.*

One composite amplifier's 1V p-p output works nicely for video circuits; providing additional output swing requires more circuitry.

dB to 10 MHz; the −3-dB point occurs at 8 MHz. You should optimize the peaking adjustment under loaded output conditions.

Normally, the Q_1-Q_2 pair would be quite drifty, but the LT1008 provides the necessary correction. The correction stage in **Fig 5** is similar to the ones in the circuits of **Figs 3** and **4**, except that **Fig 5**'s version takes the feedback from a divided-down sample of the fast amplifier. You should set the divider's ratio to the same value as the circuit's open-loop gain. The frequency roll-off of this stage is set by the 1-MΩ/0.22-μF filters in the LT1008's input lines. The 0.22-μF capacitor at the amplifier eliminates oscillations. The dc servo loop controls drift by biasing the dc operating point of Q_2's collector to force zero error between the LT1008's inputs.

The **Fig 5** circuit is a simple stage for fast applications requiring relatively low output swings. Its 1V p-p output works nicely for video circuits. A possible problem is the relatively high bias current—typically 10 μA. You need more circuitry to provide additional output swing.

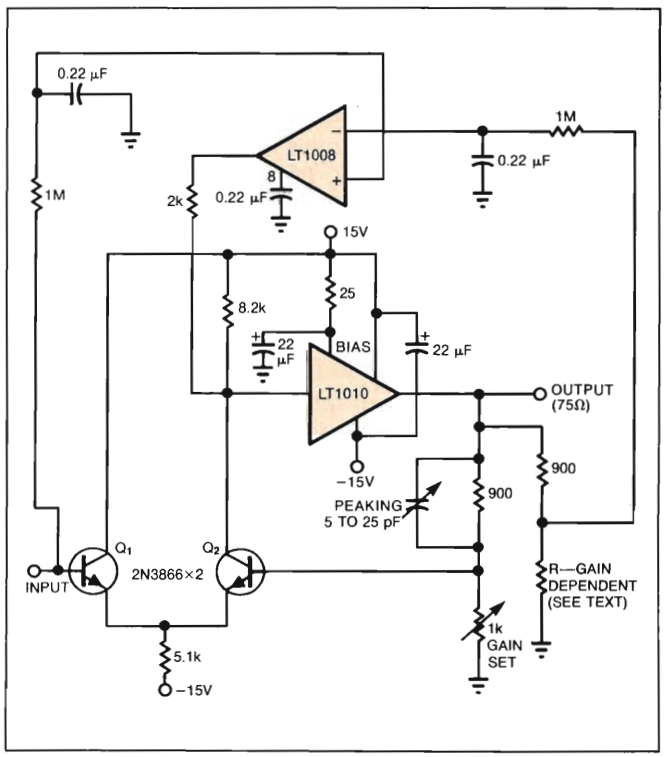


***Fig 5—A discrete differential input stage** that drives a single-ended LT1010 combines with an LT1008-based dc stabilizing loop to yield a fast amplifier that functions over a wide range of gains.*

Trade speed for output swing

The circuit shown in **Fig 6** is an attempt to remedy this situation. It trades speed for output swing and reduced bias current. As in the circuit just discussed, a separate loop maintains dc stability. **Fig 6**'s circuit is a good example of an approach made practical by composite techniques; without the separate stabilizing loop, the dc imbalances in the signal path would preclude any level of operation.

The **Fig 6** circuit adds a pnp level-shifting stage (Q_4) to the **Fig 5** circuit to increase available skewing at the LT1010 output. This improvement comes at the expense of available bandwidth and amplifier stability. The 33-pF capacitor from Q_4's collector to the circuit's summing node (Q_3's gate) affords stable loop compensation. Q_3, a FET source-follower, eliminates the bias-current errors present in **Fig 5**'s circuit by buffering the summing point from the relatively high bias current that Q_2 requires.

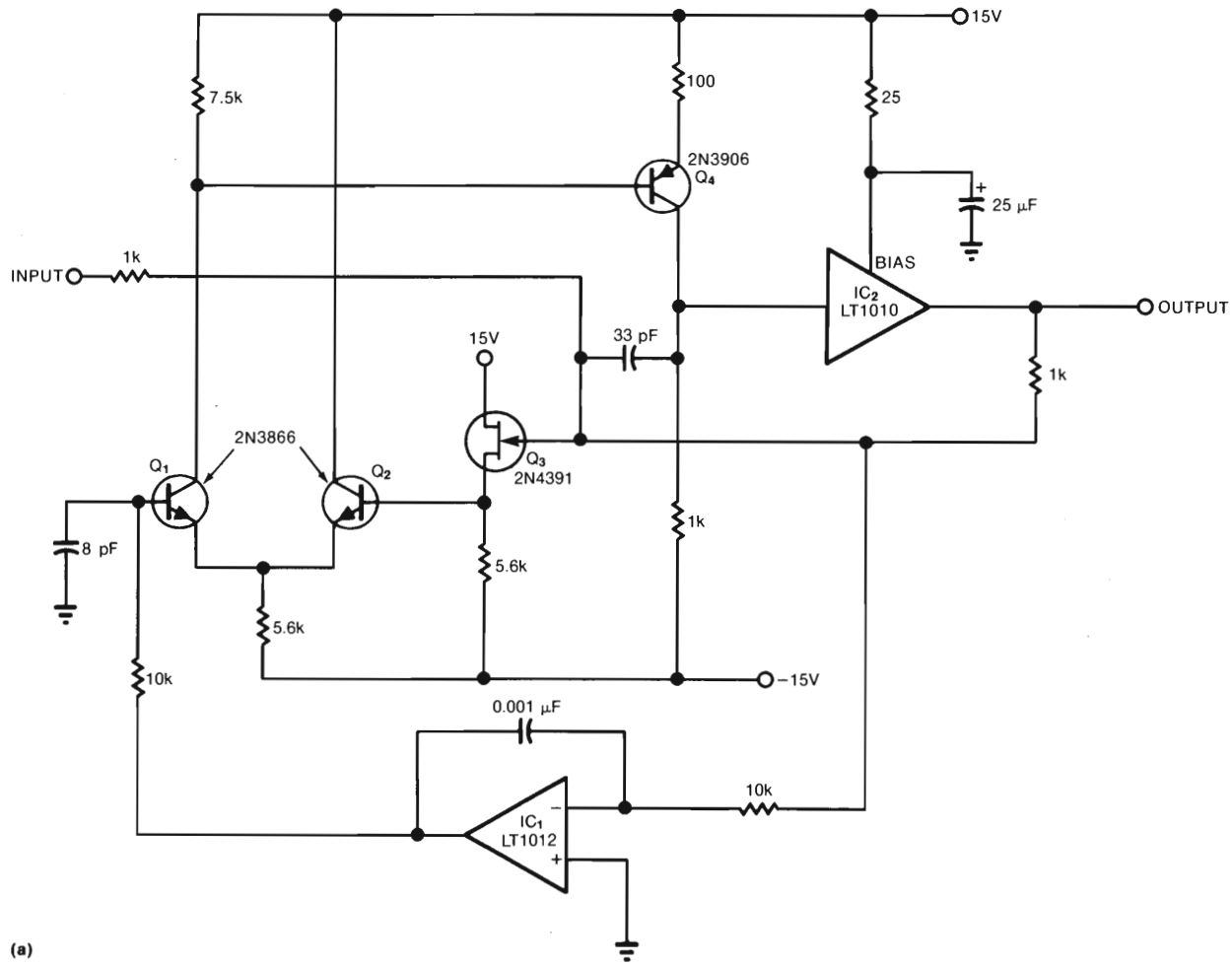
DC loop cuts offset

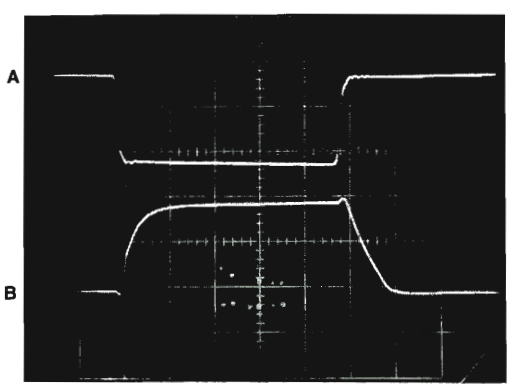
Normally, such a configuration would cause several volts of offset because of Q_3's gate-source voltage, but here IC_1 closes a dc restoration loop, forcing Q_1's base to whatever point is required to compensate the offset. Consequently, IC_1's operation not only provides dc error but helps form a simple approach to minimizing summing-point bias current. **Fig 6b** shows the operating waveforms for a 10V output (traces A and B are the input and output, respectively). The slew rate is about 100V/μsec, and the full-power bandwidth is 1 MHz. The LT1010 can furnish 100-mA outputs, making high-speed cable driving possible.

Circuit uses current-mode feedback

Fig 7 shows another fast stage with a wide output swing. The circuit is a noninverting one and has a higher input impedance than **Fig 6**'s circuit. In addition, its operation employs an arrangement commonly called "current-mode feedback." This technique, well established in RF design and also employed in some monolithic instrumentation amplifiers, allows the circuit to maintain a fixed bandwidth over a wide range of closed-loop gain. The technique contrasts with normal feedback schemes, in which the bandwidth degrades as the closed-loop gain increases.

The overall amplifier comprises two LT1010 buffers and a gain stage (Q_1 and Q_2). IC_3 acts as a dc restoration loop. The 33Ω resistors sense IC_1's operating current and bias Q_1 and Q_2. These transistors in turn furnish





TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	100 nSEC/DIV
B	5V/DIV	100 nSEC/DIV

Fig 6—This circuit (a) offers wide output swing *and low bias current, but it sacrifices speed. The photo* ***(b)*** *shows the response (trace B) to a pulse input (trace A).*

A current-mode feedback arrangement allows a circuit to maintain a fixed bandwidth over a wide range of closed-loop gain.

complementary voltage gain to IC_2, which provides the circuit's output. The feedback is from IC_2's output to IC_1's output, which is a low-impedance point.

Skewing ensures adequate loop capture

IC_3's stabilizing loop compensates large offsets in the signal path, which are dominated by a mismatch in Q_1 and Q_2. Q_3 shunts Q_2's base bias resistor to correct for these offsets. Deliberate skewing of Q_1's operating point by the 330Ω resistor ensures an adequate loop capture range. The 9-kΩ/1-kΩ divider network that provides feedback to IC_3 determines the gain ratio of the circuit—in this case 10.

The feedback scheme makes IC_1's output look like the negative input of the amplifier, with the closed-loop gain set by the ratio of the 470Ω and 51Ω resistors. The outstanding feature of this connection is that bandwidth becomes relatively independent of closed-loop gain over a reasonable range. For this circuit, the full-power bandwidth remains at 1 MHz for gains ranging from 1 to about 20. The loop is quite stable, and the 15-pF value at IC_2's input provides good damping over a wide range of gains. The LT1010 buffers limit bandwidth in this circuit.

Discrete stage eliminates IC buffers

In the **Fig 8** circuit, discrete stages replace the LT1010s to provide a dramatic speed improvement. Although this arrangement is substantially more complex, it realizes an amplifier of extraordinarily wide

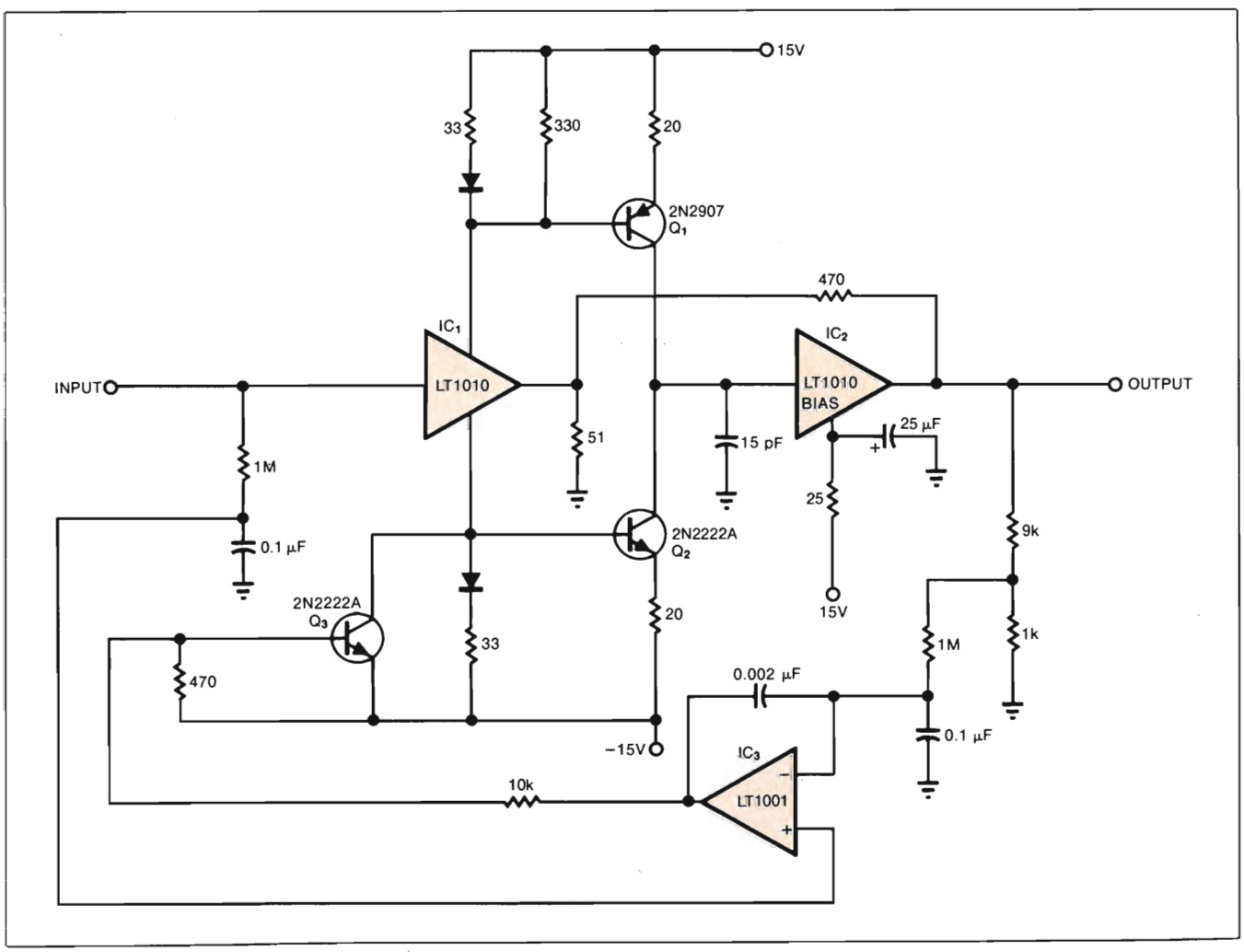
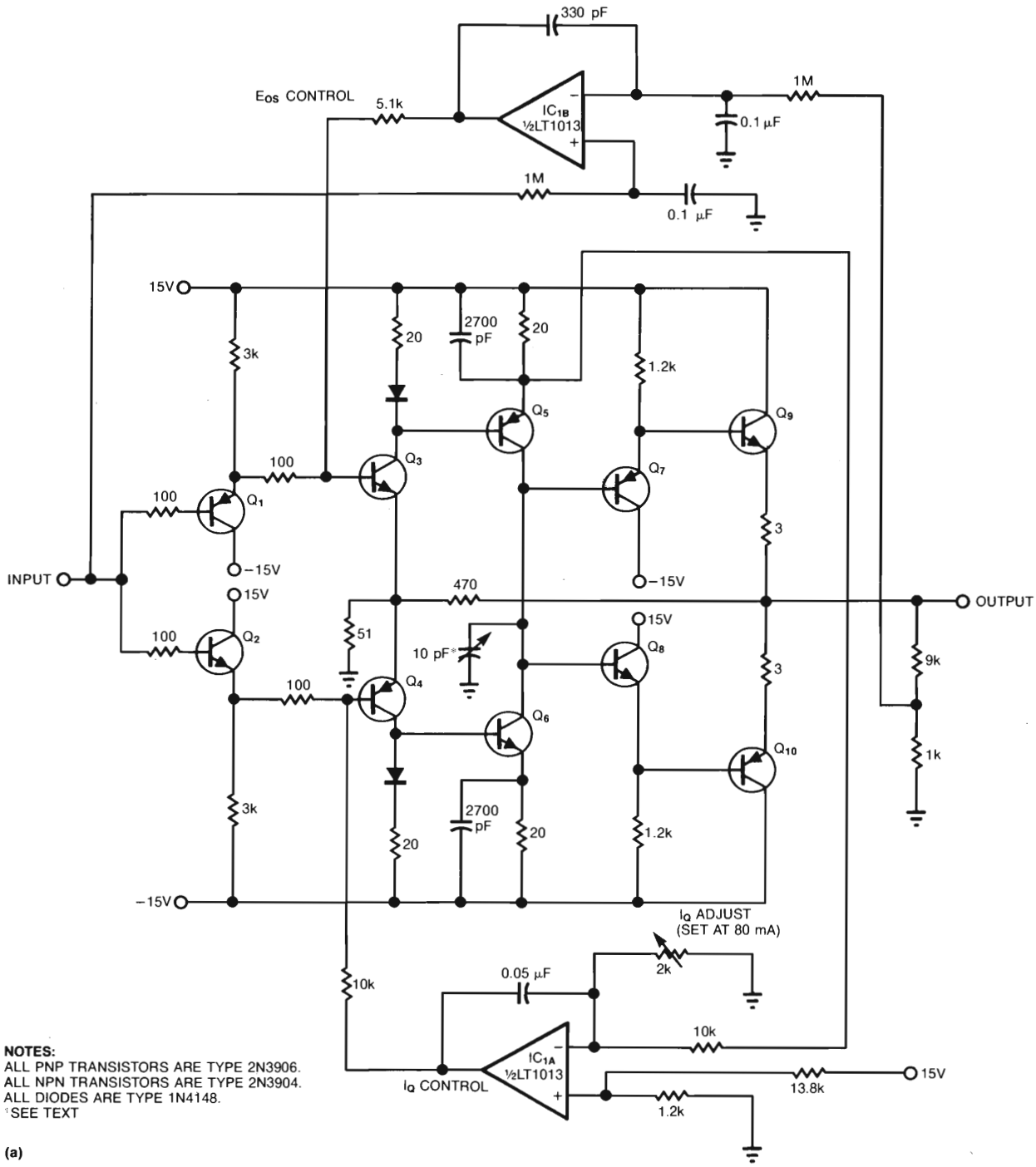


Fig 7—This noninverting amplifier circuit *employs current-mode feedback, which allows it to offer a 1-MHz full-power bandwidth for gains ranging from 1 to about 20.*



TRACE	VERTICAL	HORIZONTAL
A	4V/DIV	10 nSEC/DIV
B	4V/DIV	10 nSEC/DIV

Fig 8—Discrete transistors replace *the LT1010 buffers in this variation* ***(a)*** *of the circuit shown in* ***Fig 7.*** *In response to a pulse input, a ±12V pulse output exhibits only about 6 nsec of delay* ***(b).***

Improvement in speed and offset specs constitutes the most common reason for employing composite techniques, but circuits excelling in other areas are also possible.

bandwidth. This composite design comprises three amplifiers: the discrete wideband stage, a quiescent current-control amplifier, and an offset servo. Q_1 through Q_4 replace **Fig 7**'s IC_1, although a complementary voltage gain is taken at the collectors of Q_3 and Q_4. Q_5 and Q_6 provide additional gain, as do Q_1 and Q_2 in **Fig 7**'s circuit. Q_7 through Q_{10} form the output-buffer stage.

The feedback scheme is identical to **Fig 7**'s, with summing action occurring at the Q_3-Q_4 emitter connection. To obtain the maximum bandwidth, the circuit must maintain a high quiescent current. Without closed-loop control, the circuit would quickly go into thermal runaway and destroy itself. IC_{1A} provides the required servo control of the quiescent current by sampling a resistively divided version of the voltage across Q_5's emitter resistor and comparing it to a reference derived from the power supply. IC_{1A}'s output biases Q_4, completing a loop that forces fixed current through Q_5. This action effectively controls overall quiescent current in the discrete stage.

Simultaneously, IC_{1B} corrects for offset by forcing Q_3's base to equalize the dc input and output values at the discrete stage. Because the closed-loop gain is set at 10 (by the 470Ω and 51Ω resistors), IC_{1B} samples the output via the 10:1 divider. Both IC_{1A} and IC_{1B} have local roll-off, attenuating their response to high frequencies. Casual consideration of IC_{1A}'s and IC_{1B}'s operation might raise concern about interaction, but detailed analysis shows that the offset and quiescent-current loops do not influence each other's operation.

−3-dB bandwidth extends beyond 110 MHz

When this circuit is constructed using high-frequency layout techniques and a ground plane, the performance is quite impressive. For gains ranging from 1 to 20, the

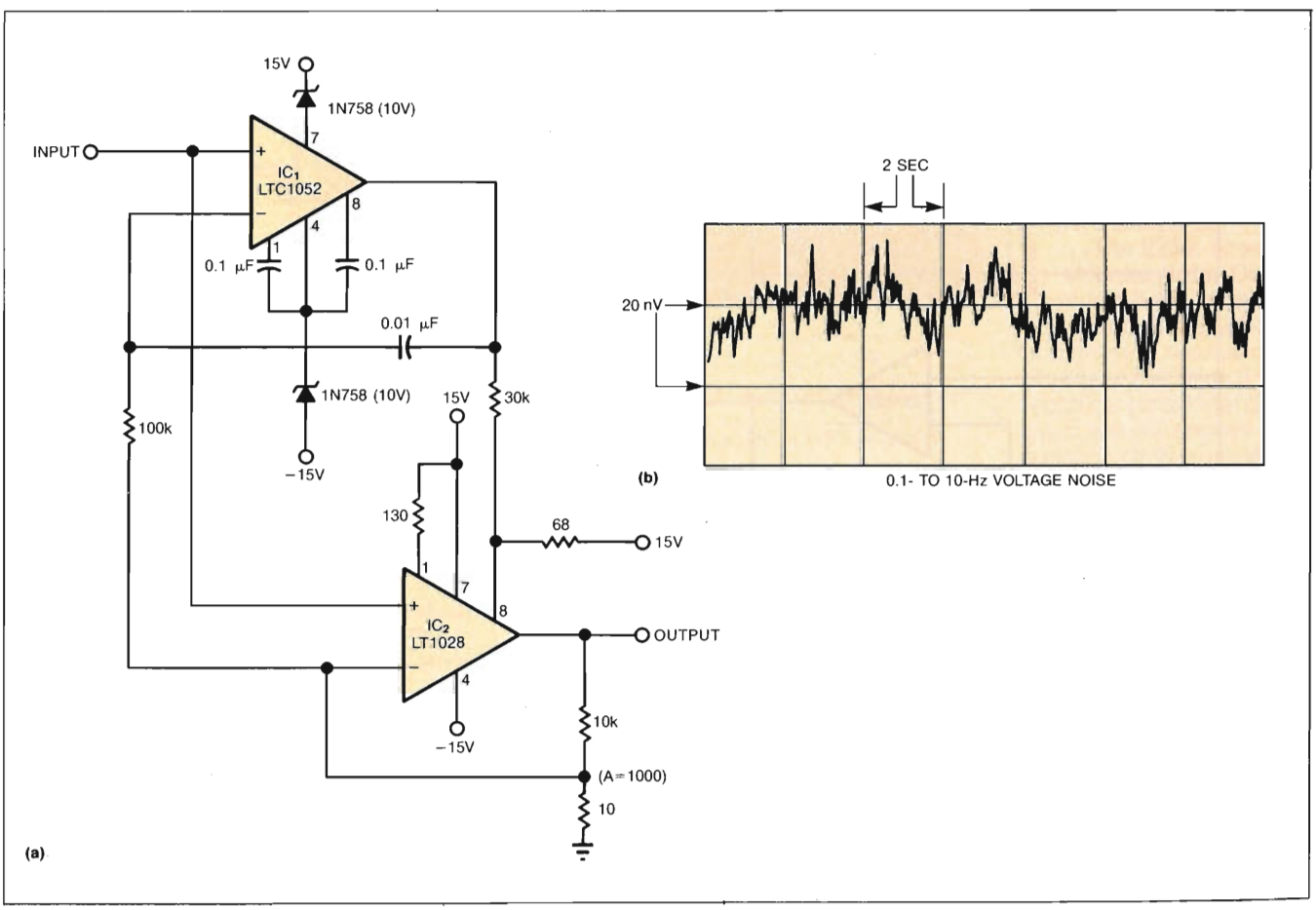


Fig 9—Composite amplifiers aren't limited *to combinations of low-offset and high-speed stages. This circuit* ***(a)*** *offers low noise performance* ***(b)*** *as well as low drift.*

You can build a circuit that uses a composite of paralleled buffers to create a simple high-current stage.

full-power bandwidth remains at 25 MHz, and the −3-dB point extends beyond 110 MHz. The slew rate exceeds 3000V/μsec. The use of RF transistors can improve these specs, although the transistors shown are inexpensive. **Fig 8b** shows the circuit's ±12V output (trace B) in response to a pulse input (trace A) for a circuit gain of 10. The delay is about 6 nsec; the rise time is limited by the input pulse generator. The 10-pF trimmer at the Q_5-Q_6 connection optimizes damping.

To use this circuit, adjust the I_Q level to 80 mA *immediately* after turn-on. Next, set IC_{1B}'s input resistor divider to a ratio appropriate to the closed-loop circuit gain. Finally, adjust the 10-pF trimmer for the best response. Note that, in the interest of achieving high speeds, this circuit has no output protection.

Composites cut drift and noise

Although improvement in speed and offset specs constitutes the most common reason for employing composite techniques, you can also build composite circuits that excel in other areas. For example, **Fig 9** shows a combination of a low-drift chopper-stabilized amplifier and an ultralow-noise bipolar amplifier. In the circuit, the LTC1052 measures the dc error at the LT1028's input terminals and biases its offset pins to force the offset to a few microvolts. The IN758 zener diodes allow the LTC1052 to function from ±15V rails. The offset-pin biasing at the LT1028 is arranged so that the LTC1052 will always be able to find a servo point. The 0.01-μF capacitor rolls off the LTC1052 at a low frequency, and the LT1028 handles the high-frequency signals. The combined characteristics of the amplifiers yield the following performance:

- Offset voltage=5 μV max
- Offset drift=50 nV/°C max
- Noise=1.1 nV/$\sqrt{\text{Hz}}$ max.

Fig 9b plots the noise amplitude over time within a 0.1- to 10-Hz bandwidth.

Fig 10 uses multiple LT1028 low-noise amplifiers to implement a statistical noise-reduction technique. The

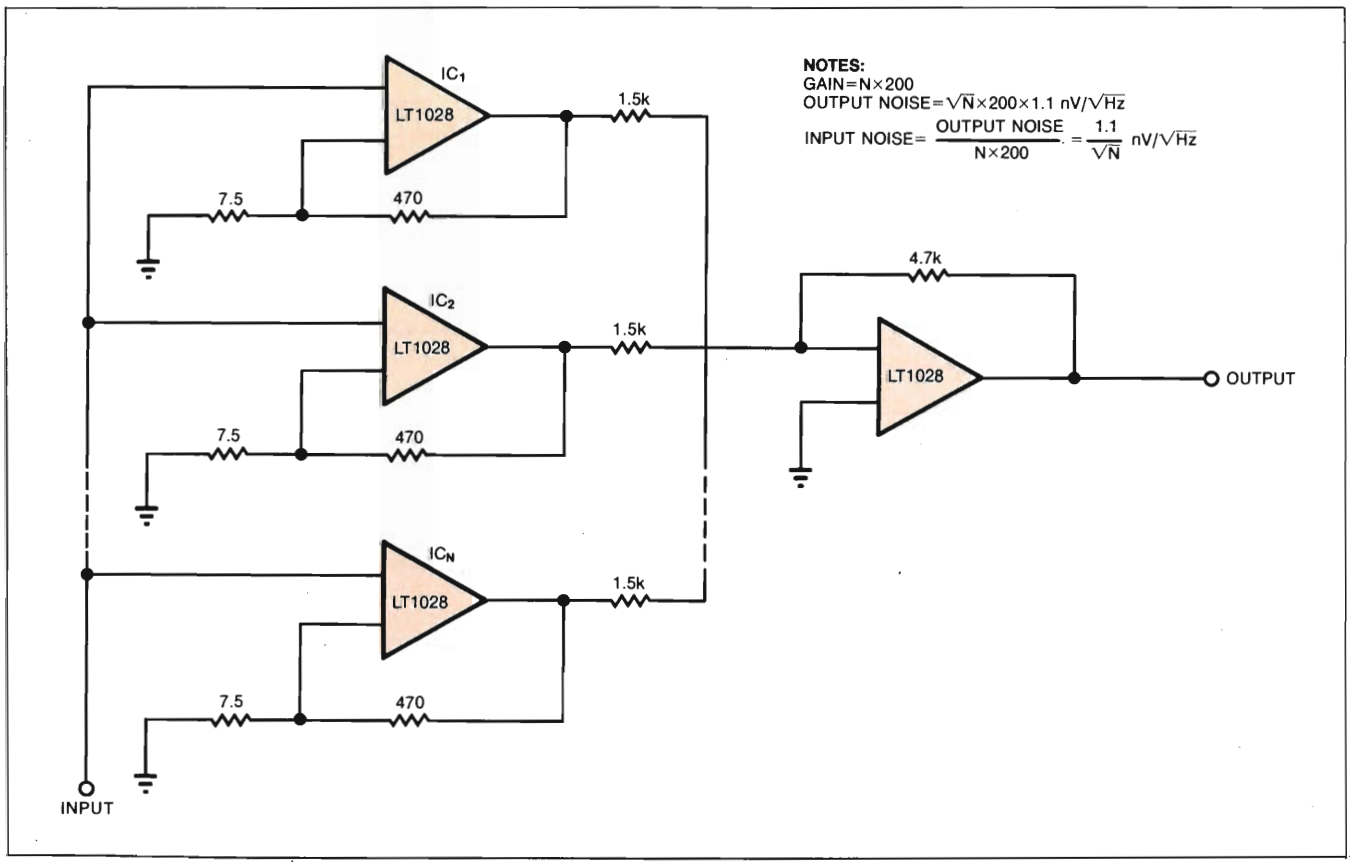


Fig 10—This multiple-amplifier design makes use of a statistical technique *to reduce noise. The decrease in noise is proportional to the* $\sqrt{N}$*, where N is the number of devices in parallel.*

Parallel connection might require some increased attention to heat sinking.

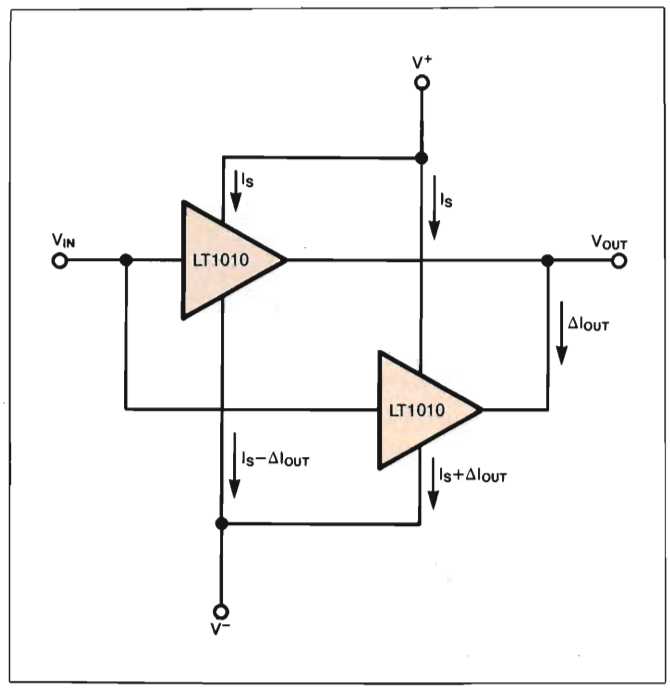


Fig 11—Paralleled LT1010 buffers *create a simple high-current stage. You can parallel any number of LT1010s as long as you take into account the increased dissipation within individual units that results from mismatches in output resistance and offset voltage.*

circuit is based on the fact that noise changes in inverse proportion to the $\sqrt{N}$, where N is the number of devices in parallel. For example, for nine amplifiers in parallel, the noise would decrease by a factor of three, to about 0.33 nV/$\sqrt{Hz}$ at 1 kHz. A potential difficulty is that, with such a configuration, the input-current noise increases with $\sqrt{N}$.

Paralleled buffers increase drive

A final circuit, shown in **Fig 11**, uses a composite of paralleled LT1010 buffers to create a simple, high-current stage. Parallel operation provides reduced output impedance, more drive capability, and improved frequency response under load. You can directly parallel any number of LT1010s as long as you take into account the increased dissipation in individual units caused by mismatches of output resistance and offset voltage.

When the inputs and outputs of two buffers are connected together, a current (ΔI_{OUT}) flows between the outputs:

$$\Delta I_{OUT} = \frac{V_{OS1} - V_{OS2}}{R_{OUT1} + R_{OUT2}},$$

where V_{OS} and R_{OUT} are the offset voltages and output resistances of the respective buffers.

Normally, the negative supply current of one unit will increase and that of the other unit will decrease, with the positive supply current staying the same. You may assume that the worst-case increase in standby dissipation (that is, when V_{IN} approaches V^+) is $\Delta I_{OUT} V_T$, where V_T is the total supply voltage.

The offset voltage for LT1010s is specified for the worst case over a range of supply voltages, input voltage, and temperature. It would be unrealistic to use these worst-case numbers for the **Fig 11** circuit, because the paralleled units are operating under identical conditions. The offset voltage specified for $V_S = \pm 15V$, $V_{IN} = 0V$, and $T_A = 25°C$ will suffice for a worst-case condition.

Use 25°C for worst-case calculations

The circuit divides the output load current according to the output resistance of the individual buffers. Therefore, the available output current will not quite be doubled unless the output resistances are matched. As for the offset voltage above, you should use the 25°C limits for worst-case calculations. Parallel operation is not thermally unstable. Should one unit get hotter than its mates, its share of the output and its standby dissipation will decrease.

As a practical matter, parallel connection requires only some increased attention to heat sinking. In some applications, a few ohms of equalization resistance in each output might be wise. Only the most demanding applications require matching, and then just of output resistance at 25°C. **EDN**

Author's biography

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and -instrumentation design. He has served in similar capacities at National Semiconductor Corp, Arthur D Little Inc, and the Instrumentation Development Lab at MIT. Jim is a former student of psychology at Wayne State University, and he enjoys tennis, art, and collecting antique scientific instruments.

Jim Williams: Circuits as art

Deborah Asbrand, *Associate Editor*

After spending years on the design of a particular group of circuits, analog-circuit designer Jim Williams sat down at his laboratory bench only to discover that the system didn't work. Months of refinement still could not get the circuits to do their intended job, which was to measure the small amounts of heat produced in a biochemical reaction. After yet another application of the soldering iron, a trace on the oscilloscope began to oscillate very slowly and then settled to a dc value. The circuits were working.

"I went crazy, running down the hall and out onto the grass," remembers Williams, who was then teaching and conducting research at MIT. "I ran into Walker dining hall and I yelled, 'It worked!' I had a one-man celebration and ran all over the campus."

Williams's enthusiasm that day is typical of the zeal that has marked his successful if unorthodox career in electronic engineering. Although his only college education consisted of the year and a half he spent studying psychology at Wayne State University, he began teaching electronic circuitry at MIT at the age of 20. Since then, he has devoted himself to analog-circuit design. In recent years, his career has taken a new turn: Now working for Linear Technology (Milpitas, CA), he spends a good portion of his time writing analog-circuit applications articles for electronics trade magazines.

Williams's approach to his work is equally unconventional. For him, designing circuits is not work at all, but an artistic endeavor that is—above all—fun. The circuit-as-art theme is evident in Williams's office, where mounted on the wall behind his desk is a colorful painting of a high-voltage amplifier circuit. Six circuit boards from the Minuteman missile-guidance system sit on top of his desk, creating a rainbow with their colorful protective coatings. Also on his desk is a package addressed to "Dr Jim Williams," the sender unaware of Williams's brief student career.

In fact, aside from the 10 years he spent as an instructor at MIT, the most fertile educational ground for Williams proved to be television-repair shops. Growing up in Detroit, he rummaged through the dumpsters behind repair shops, plucking out discarded circuit boards and lugging them home to pull apart. At 14, he got a job repairing televisions. And in 1968, when he decided to drop out of college and move to Cambridge, MA, to be closer to MIT's technical community, he supported himself by working as a TV repairman.

When Williams arrived in Cambridge at the age of 20, he had no classroom training in engineering. In fact, he had developed an acute aversion to the rigid structure found in most classrooms. But he did like to learn, and he brought to Cambridge a wealth of knowledge culled from years of dissecting shortwave radios, fans, and heaters: years of "bumbling around circuits," as he calls it. He started hanging around

Photographs by Tim Davis

the MIT campus and eventually met a professor who got him a job as a technician in a campus laboratory.

A pivotal friendship

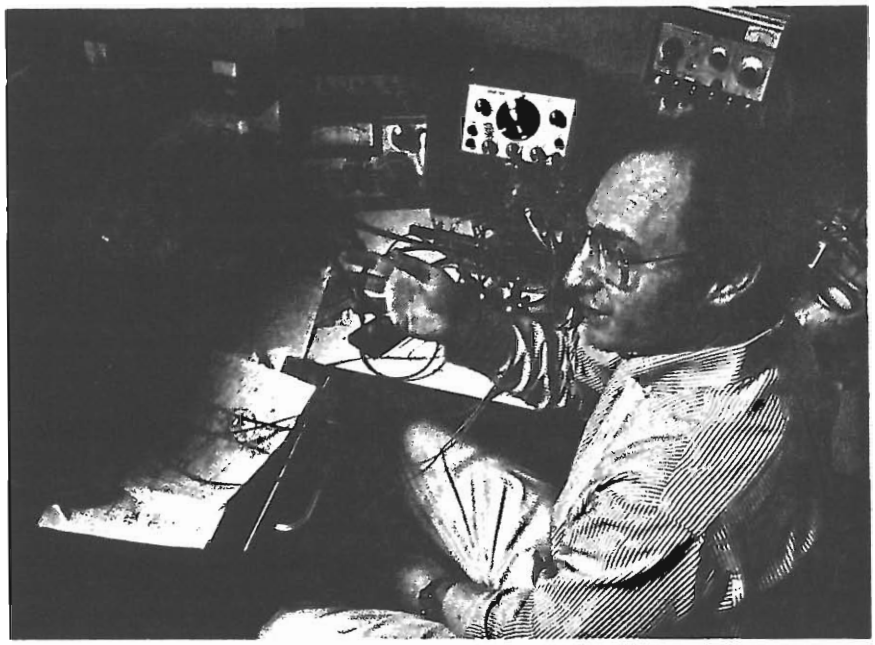
Among the bonds he established early during the MIT years was his friendship with the late Jerrold Zacharias, a professor emeritus of physics and an internationally recognized nuclear physicist. Leader of the engineering division of the Manhattan Project, Zacharias had taught at MIT for 30 years. His research on the radio-frequency spectra of atoms led to the development of the first atomic clock.

Believing that the conventional education system discriminated against individuals who didn't fit within its narrow confines, Zacharias actively worked for educational reform. He was instrumental in the formation of the Physical Sciences Study Committee, a group whose revamped curriculum for teaching high-school physics is now widely used.

Learning through teaching

After being introduced, Williams and Zacharias talked at length and often "about everything from Archimedes to art to physics to biochemistry to education to circuits," Williams says. "One day he said to me, 'If you don't like to learn [in a classroom], maybe you'd like to teach.' Zacharias said the best way to learn is to teach."

With Zacharias's support, Williams began teaching electronic circuitry to MIT students, and he thrived on teaching to others what he had learned on his own. In fact, classroom learning took on a new look for him. "I loved it. In that role, I enjoyed going to school," he says.



"For tests, I'd give students problems to work on and tell them they could talk to me or to other people in class or they could use the library. A final exam was three or four weeks long.

"I wasn't interested in whether they got the right answer—I was interested in how they approached the problem, how they perceived it, and how they pursued it. I thought that was more useful intellectually. I'm sure Einstein was able to look up anything in the library when he was pursuing the theory of relativity."

"Digital didn't seem to have any charm or poetry. I could see where it would be challenging and difficult, but it always seemed that analog design was much prettier."

Analog's allure

Comfortable in the academically open atmosphere at MIT, Williams continued to teach there for the next nine years. And his love of analog-circuit design grew steadily throughout that period. In spite of the phenomenal growth in digital design at that time, he remained fascinated by the intricacies of linear circuits. "Digital didn't seem to have any charm or poetry," he says. "I could see where it would be challenging and difficult, but it always seemed that analog design was much prettier."

Indeed, linear design's great appeal for Williams is aesthetic, and his conviction that designing is an art goes far beyond decorating his office with circuit boards. "I don't see any difference between a breadboard and a sculpture, and I never have. A circuit is a piece of sculpture because it's got a physical form —colors, shapes, lines—soul and emotion."

Williams looks at circuit designs much the same way some people approach a painting or a sculpture. "You look at it and wonder why did the designer decide to do it that way, what is his history, who did he work with? What are the hidden motivators? I can look at a circuit and know 'That's Paul Brokaw of Analog Devices.'"

An aficionado of the visual arts, Williams includes among his favorite artists sculptor Alexander Calder, known for his deft juggling of form and space, and painter Joan Miro, a modernist whose paintings are noted for their humor and gaiety. Williams's designs express a

combination of those qualities: Working in the three-dimensional medium of circuit design, he is more artist than engineer, yet despite his obvious zeal for his work, he maintains a lightness and irreverence about what he does, interspersing his artistic analogies with confessions that his job is mostly "horsing around."

While working on a particular project, Williams focuses all his energy on the design itself. "Things that are completely disparate remind me of a piece of the circuit," he says. "The way food is arranged on a plate, for example. If you go to hear the symphony, you hear the way the horns and the strings blend together, and you think, 'That's the way the base and emitter current come together.' You're lovesick for the circuit."

So personal an expression are Williams's circuits to him that they form a picture book of his life. Looking at one of his designs, he can intuit what was happening in his life at the time. "During the times when I was happiest emotionally, the circuits are simple, minimal, direct, more closely approaching elegance. At times when I was less happy, there is a lot of clutter."

Technological intrusions into the analog artist's world don't faze Williams. Despite the innovations of analog CAE techniques, linear circuits remain best designed first on paper and then manually on a breadboard, he says. "Much of the ultimate achievable perfection is defined by the imperfection of the components and the skills of the designer in getting around that." He happily remains "virtually digitally illiterate. I've never programmed a computer or designed a digital circuit. I can't give you the truth tables for simple logic gates."

"Some people think about skiing while they're at work; I think about circuit design while I'm skiing."

As for his analog-design skills, he says they reflect "lots of enthusiasm and not too much formality." An abundance of impatience makes him "more likely to try something than to think about it," he says. "I iterate rather than create. I've seen people who can pull elegantly simple ideas out of their heads, but I have to slosh through the mud to get where I'm going."

By his own definition, his analog chauvinism precludes his presence among the elite designers. "The best circuit designers I've seen are generalists . . . . They don't view themselves as analog designers or digital designers. They look at themselves as working within the whole spectrum of design and they use whatever tool is required."

At age 38, Williams has already achieved a goal that is high on many people's lists: He is doing what he loves to do. He became an independent consultant after leaving MIT in 1978, and then worked as a linear designer for National Semiconductor. In 1981, he became a staff scientist at Linear Technology; it's the company's highest ranking title for nonmanagers.

At Linear Technology, Williams spends one half of his time on applications designs and the other half writing articles on analog design. The decision to devote such a large chunk of his time to writing is part mission—to spread the analog gospel—and part career move. Too many engineers, he says, leave their careers to the vagaries of fate and the economy. Writing articles is a way for Williams to sharpen his writing skills and enhance his marketability.

In his present job, Williams also participates in policy-making decisions, a responsibility he says irks him when he has to drop a design project to attend executive meetings, yet also serves to relieve him of his "white-socks laboratory existence." Like other designers at the company, he works informally with a young engineer, teaching him the finer points of analog circuitry and acting as a mentor, a role he consid-

ers both fun and obligatory. "They teach people analog fundamentals in universities, but in the end, industry is going to have to spend years training these people. There really is no substitute for sitting at a lab bench with a lot of expensive equipment around and having someone hold your hand." He gets several job offers a year, but finds few interesting. "I don't want just a job. I want fun. There's a difference."

Circuits, skiing, and tennis

Despite his passion for circuit design, it remains only part of his life's focus. "I'm not a workaholic, but I don't see a [boundary line] between circuit design and skiing, tennis, or travel. They all seem to fit together nicely. Some people think about skiing while they're at work; I think about circuit design while I'm skiing."

Indeed, he's taken the same immersion approach to learn other activities that he took to learn circuit design. When he wanted to learn to ski, he started with a lesson, but then drifted away from the rest of the class, spending the rest of the week skiing—and falling—down the slopes until he had begun to master the techniques. After completing a course on cooking, he tackled coq au vin at home, making it five nights in a row until it met his approval. When one restaurant's hollandaise sauce struck him as especially well made, he convinced the chef to let him into the kitchen and teach him her techniques.

Out of all the activities he engages in, writing about his designs is the least satisfying. Descriptive articles about circuit design can never recapture the thrill of the design process, he says. "On paper, it's just never good enough. I can never match the level of emotion I feel for a circuit when I see it on paper."

EDN

Micropower circuits assist low-current signal conditioning

Part 1 of this 2-part series focuses on micropower signal conditioning for the various sensors and transducers that have inherently low impedance or output voltage. Those characteristics can complicate the design of a circuit that must operate at low current and low power. Part 2, scheduled for the August 20 issue, will look at micropower design techniques for the signal conditioning of A/D and V/F converters, of an a S/H circuit, and of several low-power regulator circuits.

Jim Williams, *Linear Technology Corp*

Applications such as medical instrumentation, remote data acquisition, and power monitoring are all excellent candidates for battery operation, making low power consumption increasingly desirable in electronic apparatus. Micropower analog circuits for transducer-based signal conditioning present their own special problems. Although ICs that operate at low current are available, the interconnection of these devices to form a micropower circuit requires care (see **box,** "Designing micropower circuits: some guidelines"). In particular, tradeoffs between signal levels and power dissipation become painful when you want good performance in the 10- to 12-bit range. Also, many transducers intrinsically produce small outputs, complicating an already difficult situation when dealing with micropower requirements. Despite these problems, the design of micropower circuits is possible by using high-performance, low-current-drain ICs with the appropriate circuit techniques.

Fig 1 illustrates a simple circuit for signal conditioning a platinum RTD (resistance temperature detector); the circuit includes correction for the sensor's nonlinear response. The circuit accuracy is ±0.25°C over a sensed range of 2 to 400°C. To improve noise immunity, you should connect one side of the sensor to ground. Current consumption is 250 μA for a sensed temperature of 2°C and increases to 335 μA at 400°C. You connect the platinum sensor in a current-driven bridge with the 1-kΩ resistors.

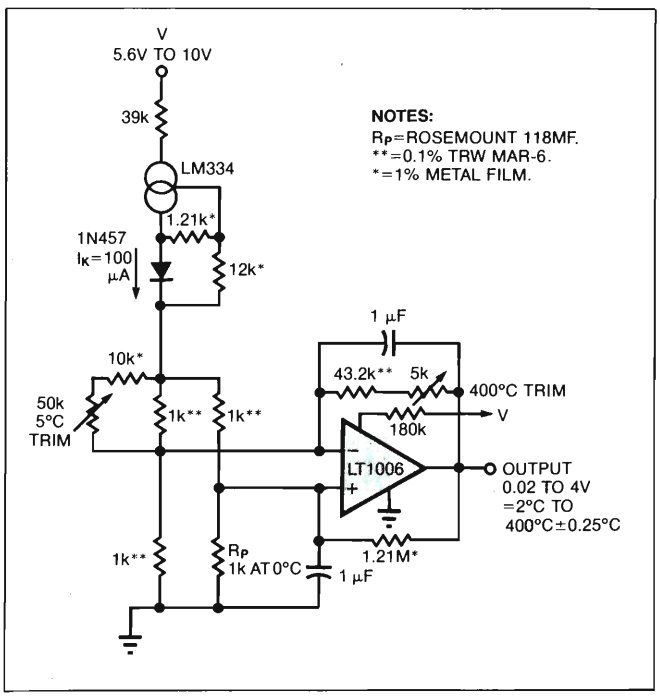


Fig 1—This signal-conditioning circuit *for a platinum temperature sensor includes correction for the sensor's nonlinear response. Current drain is 250 μA at a 2°C sensed temperature, increasing to 335 μA at 400°C.*

Text continued on pg 126

Designing micropower circuits: some guidelines

The most obvious way to save power is to choose components that use little energy. Although they require more effort, some subtler procedures can give you additional savings. First, you should examine the circuit current flow in terms of all ac and dc paths. Check, for example, to see that dc base currents are going where they can do some useful work. Try to minimize ac signal swings, particularly where you must continually charge and discharge capacitors (both designed-in and parasitic capacitors).

In addition, you should examine the circuit for areas where power strobing or sampling is possible. To avoid surprises, consider the quiescent power requirements of components in comparison to the dynamic ones. Data sheets usually specify quiescent power requirements because the manufacturer doesn't know what the user's circuit conditions are.

Similarly, the common assumption that MOS devices draw no current can get you into trouble. Natural law dictates that, as frequencies and signal swings increase, the capacitances associated with MOS devices begin to require more power. So it's often a mistake to associate low-power operation with any particular process technology. Although it's likely that CMOS will provide lower power operation than a 12AX7 vacuum tube, a bipolar approach may be even better. In the end, you might opt for a combination of technologies—CMOS and bipolar ICs, for example, along with discrete transistors and diodes—for best results.

Obtaining low-power operation usually requires performance tradeoffs. Minimizing signal swings and current drain saves power, but it also moves circuit operation closer to the noise floor. As you constrict signal amplitudes to save power, you'll find that offsets, drift, bias currents, and noise become increasingly significant error factors. Circuits using power strobing can sometimes avoid this problem by resorting to low duty cycles. Using this technique, the circuit in **Fig 3** (pg 127), for example, achieves dramatic power savings with an on-state current drain that approaches 20 mA.

Fig A shows a rudimentary version of a V/F converter. When the input current-derived ramp at IC_{1A}'s negative input crosses zero, IC_{1A}'s output drops low, pulling a charge through capacitor C_1 and forcing the negative input below zero. Capacitor C_2 provides positive feedback, allowing a complete discharge for C_1. When C_2 decays, IC_{1A}'s output goes high and clamps at the level set by D_1, D_2, and V_{REF}. C_1 receives a charge, and recycling occurs when IC_{1A}'s negative input again reaches zero. The frequency of this action relates to the input voltage. Diodes D_3 and D_4 steer, while diodes D_1 and D_2 provide temperature compensation. The sink saturation voltage of IC_{1A} is small and uncompensated. IC_{1B} acts as a start-up loop.

Although the LT1017 and LT1034 have low operating currents, the circuit in **Fig A** draws almost 400 μA. The ac-current paths include C_1's charge-discharge cycle and C_2's branch circuit. The dc path through D_2 and V_{REF} is particularly costly. C_1's charging must occur quickly enough for 10-kHz operation—that is, the clamp seen by IC_{1A}'s output must have a low impedance at that frequency.

Capacitor C_3 helps, but you still need significant current to keep the impedance low. IC_{1A}'s current-limited output cannot do the job alone; it uses the supply's resistor to help in keeping the impedance low. Even if IC_{1A} could supply the necessary current, V_{REF}'s settling time would be an issue.

Dropping C_1's value reduces the impedance requirements proportionally and seems to solve the problem. Unfortunately, such a reduction magnifies the effects of stray capacitance

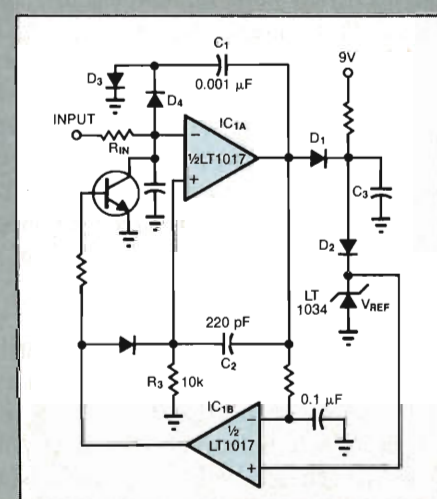


***Fig A—This rudimentary version of a V/F converter** draws almost 400 μA. The dc path through D_2 and V_{REF} is particularly costly.*

at the D_3-D_4 junction. It also mandates an increase in the value of R_{IN} to keep the scale factor constant. This increase lowers the operating currents at IC_{1A}'s negative input and thus makes bias current and offset more significant sources of error.

Attacking the problems

Fig B shows an initial attempt at dealing with these issues. This scheme is similar to **Fig A**'s, except for the addition of Q_1 and Q_2. Instead of being on all the time, V_{REF} now receives switched bias via Q_1, and Q_2 provides the sink path for C_1. These transistors invert IC_{1A}'s output, requiring an exchange in its input-pin assignments. Resistor R_1 provides a small current from the supply, improving the reference settling time. This arrangement decreases supply current to about 300 µA.

Several problems remain, however. The switched operation of Q_1 is really only effective at higher frequencies. In the lower ranges, IC_{1A}'s output is low most of the time, biasing Q_1 on and wasting power. Also, when IC_{1A}'s output switches, Q_1 and Q_2 simultaneously conduct during the transition, effectively shunting R_2 across the supply. Finally, the base currents of both transistors flow to ground and are lost. The basic temperature compensation is thus the same as before, except that Q_2's saturation term replaces that of the comparator.

Fig C presents a better solution. Q_1 is gone, but Q_2 remains with the addition of Q_3, Q_4, and Q_5. V_{REF} and its associated diodes receive bias from R_1. Q_3 is an emitter follower and sources current to C_1. Q_4 provides temperature compensation for Q_2's V_{BE}, and Q_5 switches Q_3.

This method has some distinct advantages. The V_{REF} string can operate at greatly reduced current because of Q_3's current gain. Also, the simultaneous conduction problem in **Fig B** is largely alleviated because Q_2 and Q_5 are switched at the same voltage threshold from the output of IC_{1A}. Q_3 delivers its base and emitter currents to capacitor C_1. Q_5's currents are wasted, although they are much smaller than Q_3's. Q_2's small base current is also lost. The circuit design changes the values for C_2 and R_3. The time constant is the same, but some current reduction occurs because of the increase in the value of R_3.

If, for performance reasons, you cannot reduce the value of C_1, then you must accept its ac currents. The only significant wasted values are the Q_2 and Q_5 currents, along with the now smaller R_1 loss. Current drain for this circuit is about 200 µA max.

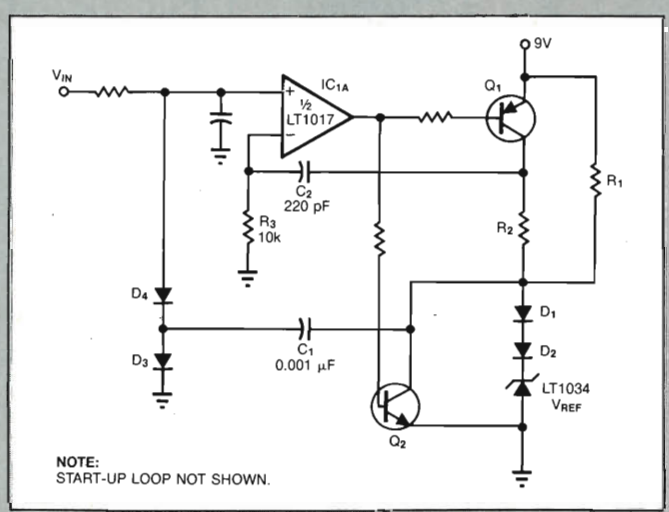


Fig B—This improved version of the Fig A circuit needs only 300 µA of current. Instead of being on continuously, V_{REF} now receives switched bias.

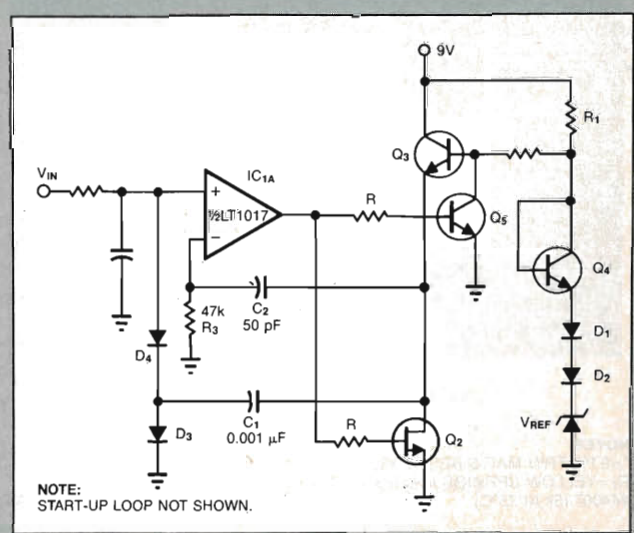


Fig C—Needing only 200 µA, this circuit operates the V_{REF} string at greatly reduced current.

ICs that operate at very low currents do not, by themselves, guarantee the successful design of micropower circuits. Techniques are of equal importance.

The LM334 current source drives the bridge at an operating current of 100 μA, determined by the bridge's equivalent resistance. The 1N457 diode in series with the bridge provides temperature compensation. By reducing the voltage across the LM334, the 39-kΩ resistor minimizes its temperature rise and ensures its closer temperature tracking with the diode. The low current of 100 μA, which is split by the bridge, restricts the platinum sensor's output to about 200 μV/°C.

To achieve a circuit accuracy of ±0.25°C and stable gain, you should use a low-power precision op amp like the LT1006. The LT1006 takes the signal differentially from the bridge to provide the circuit's output. The platinum sensor's slightly nonlinear response normally causes several degrees of error over the sensed temperature range, but the 1.21-MΩ resistor provides a slight positive feedback to correct for this error. The amplifier's negative feedback path dominates, and the circuit configuration is stable. The 1-μF capacitor rolls off the circuit's high-frequency response, and the 180-kΩ resistor programs the LT1006 for 80 μA of quiescent current.

Use decade box for calibrating

To calibrate this circuit, you can substitute a precision decade box (such as the General Radio #1432) for R_P. Set the box to the 5°C value (1019.9Ω) and adjust the 5°C trim for 0.05V at the output of the LT1006. Next, set the box for the 400°C value (2499.8Ω) and adjust the 400°C trim for 4.00V output. Repeat this sequence until both points remain fixed.

The resistance values set by the decade box are for a nominal 1000.0Ω (0°C) sensor. You can use sensors deviating from this nominal value by factoring in the deviation from 1000.0Ω. Because it is an offset value that arises from winding tolerances during the fabrication of the RTD, the manufacturer specifies this deviation for each individual sensor. The platinum's gain slope, which is primarily fixed by the purity of the material, is a very small error factor.

The temperature-sensing circuit in **Fig 2** uses a thermocouple as the transducer. It is accurate within 1.5°C over the sensed temperature range of 0 to 60°C. Current consumption is about 125 μA.

Not only are thermocouples inexpensive, they have low impedance and generate their own outputs. They do, on the other hand, produce low-level outputs and require cold-junction compensation, both of which complicate signal conditioning. The bridge network, composed of a thermistor and its associated resistors, provides cold-junction compensation with the LT1004 acting as a voltage reference. The lithium battery lets the bridge float and also lets the thermocouple have a ground reference, thereby eliminating the need for a multi-amplifier differential stage with its attendant

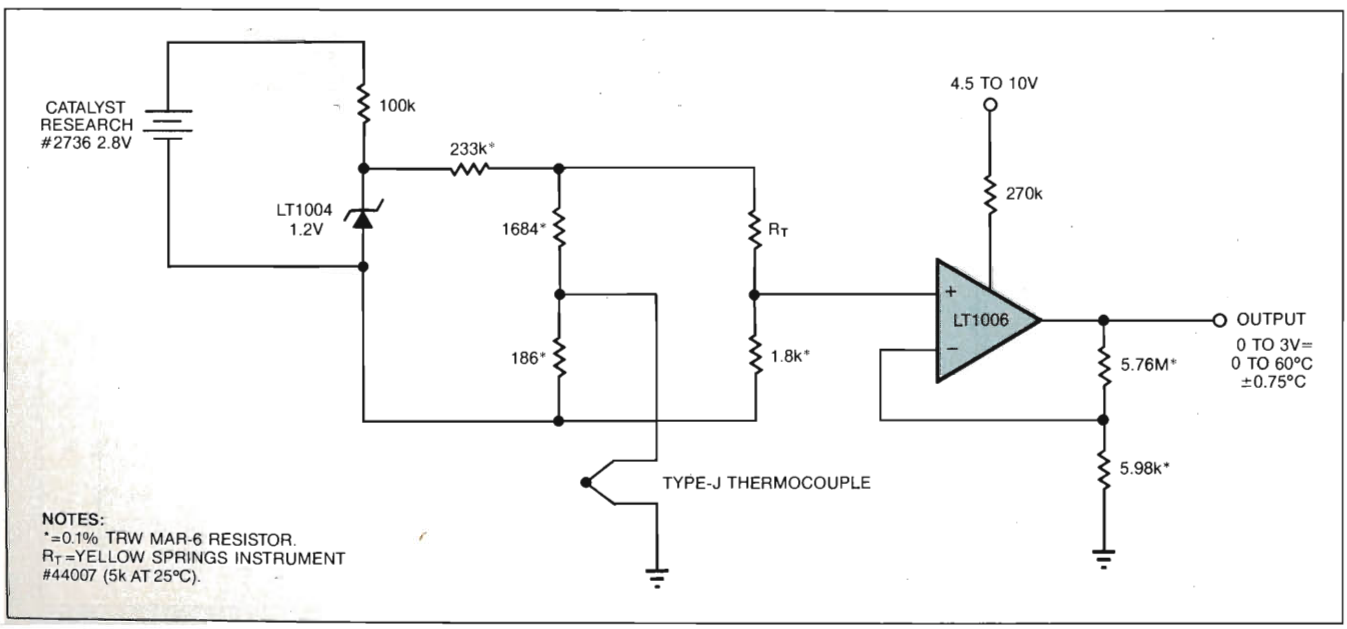


Fig 2—This thermocouple-type temperature-sensing circuit features cold-junction compensation *and is accurate within 1.5°C over a 60°C temperature range. Current-drain is about 125 μA.*

power drain. (The battery specified in the figure is supposed to last nearly 10 years.) The gain adjustment of the LT1006 provides the output shown, and the 270-kΩ resistor programs the IC for low current drain. Note that this circuit requires no trimming.

Bridge-based, strain-gauge transducers present a challenge for low-power designs. Some common values for the transducers are a 350Ω impedance and a low output signal (typically 1 to 3 mV per volt of drive), and these common values create problems for low-power designs. Even with only 1V of drive, the bridge current consumption approaches 3 mA. Reducing the drive to 100 mV drops the current to acceptable levels, but precludes any great accuracy because of the minuscule output available.

In many situations, continuous transducer information is unnecessary, and consequently a sampling operation is viable. Sampling at a low duty cycle permits a high-current bridge drive while keeping the average power consumption low (see **box,** "Sampling techniques reduce circuit current"). **Fig 3** uses such a scheme to achieve dramatic power savings in a strain-gauge bridge application.

In the circuit of **Fig 3**, Q_2 is off when the sample command is low. Under these conditions, only the LT1006 and the CD4016 receive power, and the current

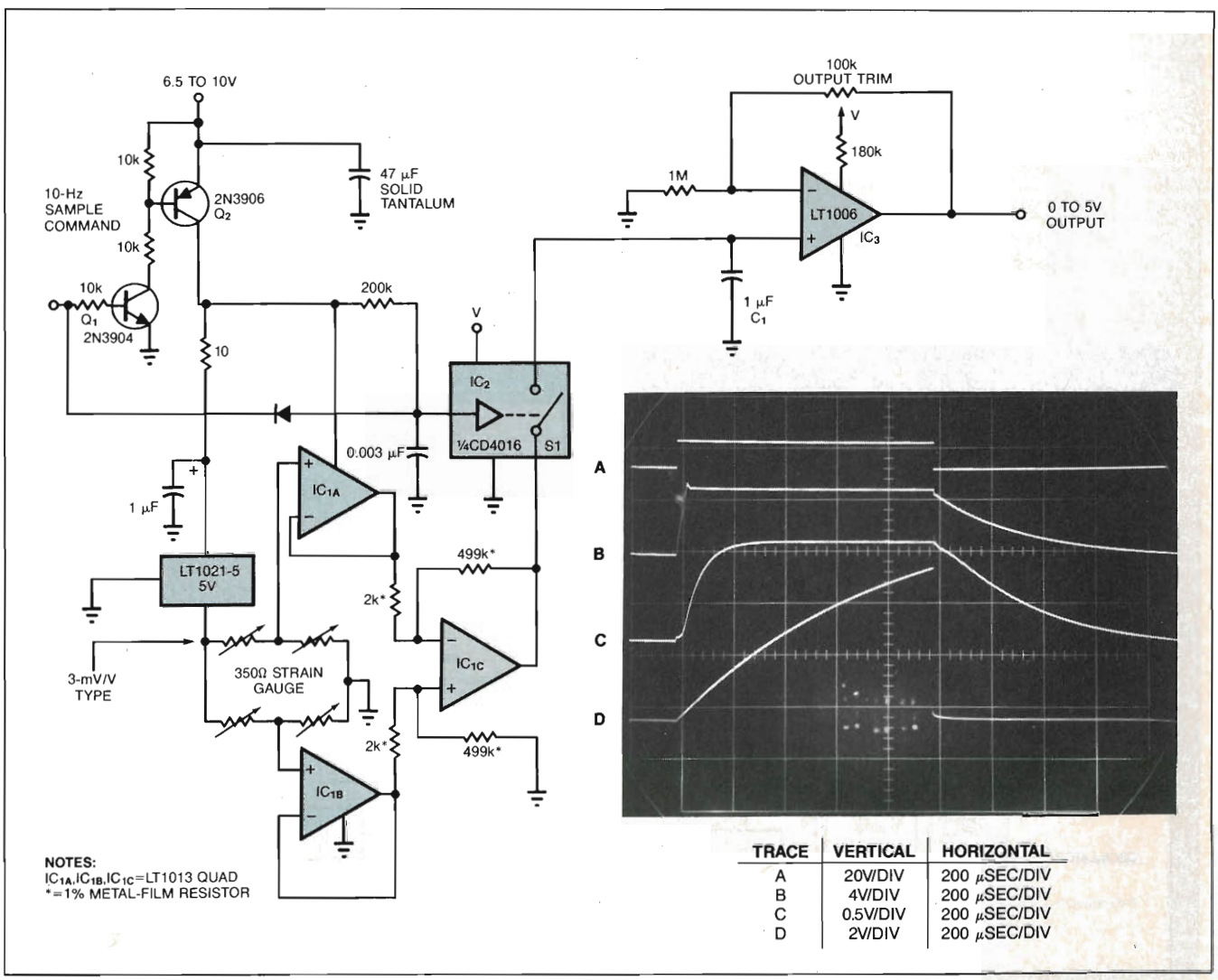


Fig 3—Strain-gauge bridge-type transducers present problems *in achieving low-current operation because of their low impedance and low output signals. The circuit shown in* ***a*** *uses a sampling approach to lower the average current. The operating waveforms shown in* ***b*** *are described in the text.*

Sampling or strobing techniques can drastically reduce the average current drain in many circuits while still providing full drive power when needed.

drain is less than 125 μA. When the sample-command pulse goes high, the collector of Q_2 (trace A, **Fig 3b**) goes high, providing power to all other circuit elements. The 10Ω resistor and the 1-μF capacitor at the input of the LT1021 prevent the strain bridge from having to handle a fast-rising pulse, which could cause long-term transducer degradation.

The LT1021-5 reference output (trace B) drives the strain bridge, and the output of the differential amplifier IC_{1A}, IC_{1B} appears at IC_{1C} (trace C). At the same time, S_1's switch-control input (trace D) ramps toward Q_2's collector. At about half of Q_2's collector voltage (in this case, just before midscreen), S_1 turns on, and the output of IC_{1C} charges capacitor C_1. When the sample command drops low, Q_2's collector falls, the bridge and its associated circuitry shuts down, and S_1 turns off.

Sampling techniques reduce circuit current

The best way to achieve low-power circuit characteristics is to turn off the power. Obviously, there are some problems with this approach, but in many applications, continuous circuit power is not necessary. If bandwidth requirements are low, sampling techniques offer a simple way to save power. With low duty cycles, instantaneous current can be relatively high, and average current drain remains low.

One of the issues you need to examine when considering a sampling approach is that the desired circuit bandwidth dictates the minimum sampling frequency in accordance with Nyquist criteria. The circuit's settling time (to the desired accuracy) determines the required duration of the sampling interval.

You should consider this settling time for all circuit elements (transducers, ICs, and discrete components) separately and together. You should also examine the effects of a sampled operation on component life and oper-

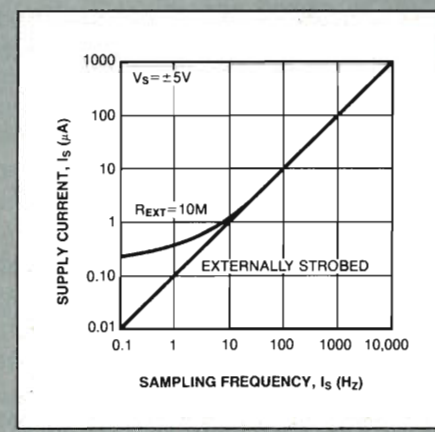


***Fig B—This graph plots supply current vs frequency** for the circuit in **Fig A**.*

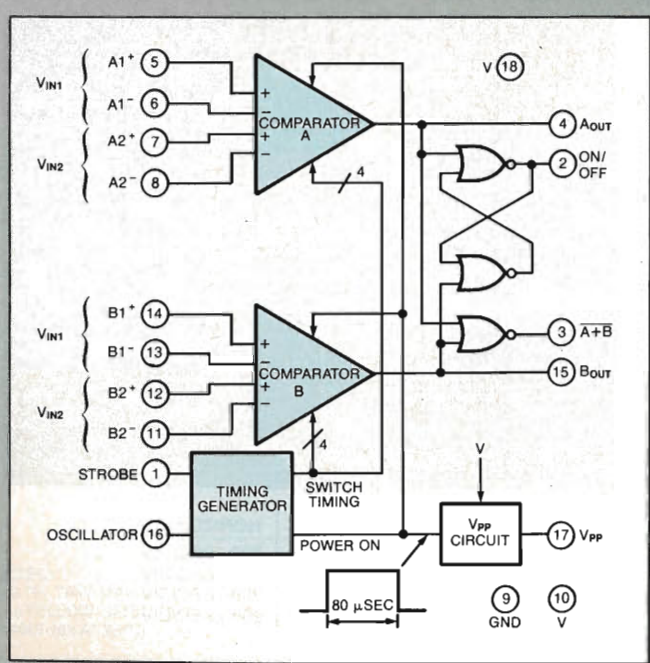


***Fig A—The output of the LTC1040 dual comparator** supplies power only during the programmed sampling interval.*

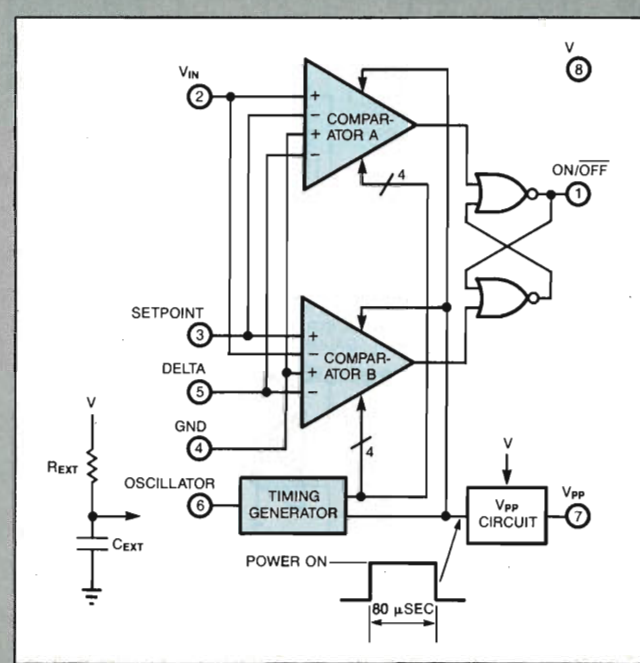


***Fig C—The LTC1041 shown here** is dedicated to on-off servo operation.*

Capacitor C_1's stored value appears at the gain-scaled output of the LT1006 (IC_3).

By preventing the updating of C_1 until IC_{1C} settles, the RC delay at S_1's control input ensures glitch-free operation. During the 1-msec sampling phase, supply current approaches 20 mA, but the 10-Hz sampling rate cuts the effective current drain below 200 μA. Slower sampling rates will further reduce current drain, but C_1's droop rate (about 1 mV/100 msec) limits the accuracy. The 10-Hz rate provides adequate bandwidth for most transducers. The gain trimming shown allows calibration for 3-mV/V slope-factor transducers. You should rescale the trimming for other types. The current drain of this circuit is about 300 μA, and the output is accurate enough for 12-bit systems.

By switching most of the power into the circuit, the

ating characteristics. This latter issue is particularly important in the case of transducers, which are often designed and tested under dc operating conditions.

The LTC1040, 1041, and 1042 are specifically designed for sampled operation. **Fig A** details the LTC1040 dual micropower comparator. Its programmable internal oscillator sets a sampling rate with an interval lasting 80 μsec. The V_{PP} output supplies power during the sampling interval, thereby providing drive for the external circuitry or transducers. Note that the input common-mode range includes both rails. **Fig B** plots supply current vs sampling frequency.

The LTC1041 is shown in **Fig C**. Although similar to the 1040, it is specially dedicated to on-off servo loops. You can control the servo setpoint and delta at the inputs. The **Fig D** diagram graphically defines its operation. The operating current is similar to the 1040's.

The final example, the LTC1042, is also similar to the 1040, but it's laid out as a window comparator. Its internal construction is shown in **Fig E**, and its graphic operation, in **Fig F**. The operating current, input range, and sampling characteristics are similar to the LTC1040's and 1041's.

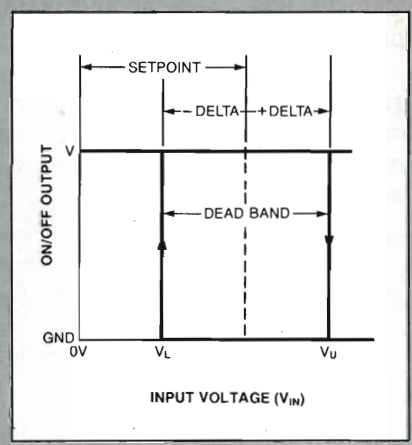


Fig D—This plot of the LTC1041's setpoint and delta graphically defines its operation.

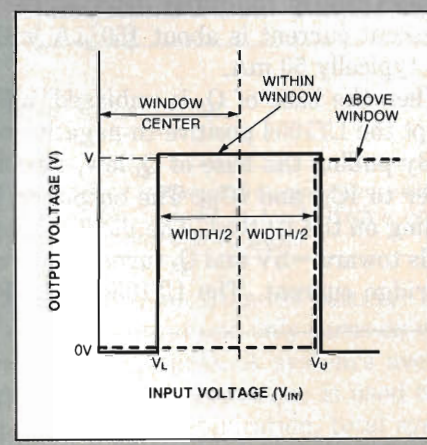


Fig F—This graph illustrates the window characteristics of the LTC1042 comparator.

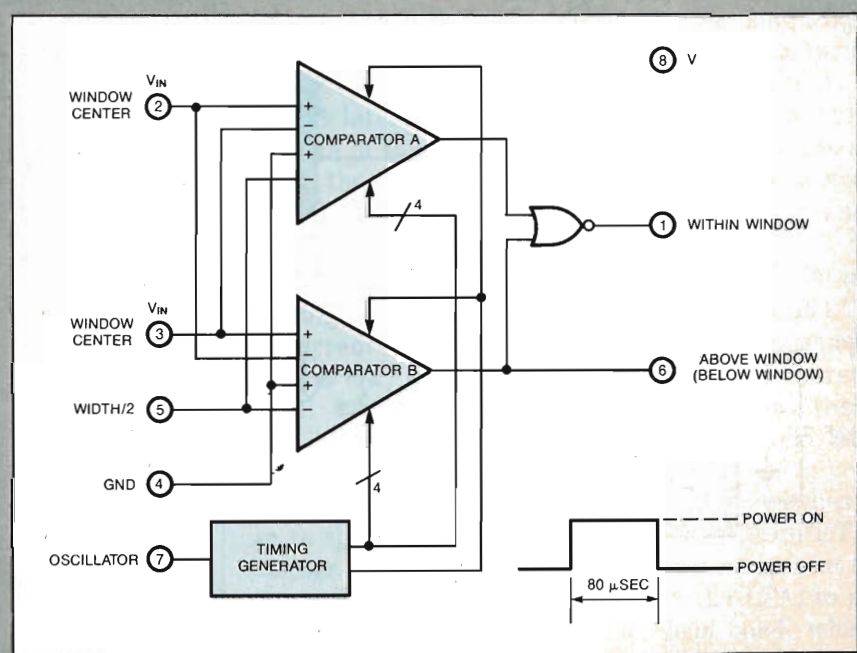


Fig E—The LTC1042 window comparator is similar to the 1040 and 1041 in terms of operating current and sampling characteristics.

The low impedance and low output-voltage of many transducers present special problems in the design of micropower circuits.

circuit in **Fig 4** helps to reduce losses caused by the strain-gauge bridge. Rather than operate in a continuously sampled mode, this circuit sits in a quiescent state for long periods, with relatively brief on times.

A typical application for this circuit is the remote measurement of the contents of a storage tank when weekly readings are sufficient. Despite the floating output of the strain-gauge bridge, the circuit has the advantage of not needing a differential amplifier. In addition, it improves measurement accuracy because it provides nearly full-rated drive to the strain bridge. Quiescent current is about 150 μA with on-state current typically 50 mA.

When the base of Q_1 is unbiased, all circuitry is off except the LT1054 positive-to-negative voltage converter. By pulling the base of Q_1 low, its collector supplies power to IC_{1A} and IC_{1B}. The output of IC_{1A} goes high, turning on the LT1054. The pin 5 output of the LT1054 heads toward −5V and Q_2 turns on, permitting the flow of bridge current. The LT1054, with IC_{1A} acting as a servo, balances the inputs to the bridge and drives the midpoint of the bridge to 0V. The bridge ends up with about 8V across it, and so requires the LT1054, which can handle 100 mA, to sink about 24 mA. The 0.02-μF capacitor then stabilizes the loop.

The negative output of the IC_{1A} and LT1054 loop sets the common-mode voltage of the bridge to zero, allowing IC_{1B} to make a simple single-ended measurement. The output trim adjustment scales the circuit for a 3-mV/V strain-gauge bridge transducer. The 100-kΩ resistor and 0.1-μF capacitor together provide noise filtering.

2-wire thermistor needs no external supply

Current-loop control in the range of 4 to 20 mA is common in industrial environments, and circuits that are used to modulate data into this type of loop must operate well below the 4-mA minimum current. The 2-wire thermistor used in a complete temperature-transducer interface (**Fig 5**) has an output in the 4- to

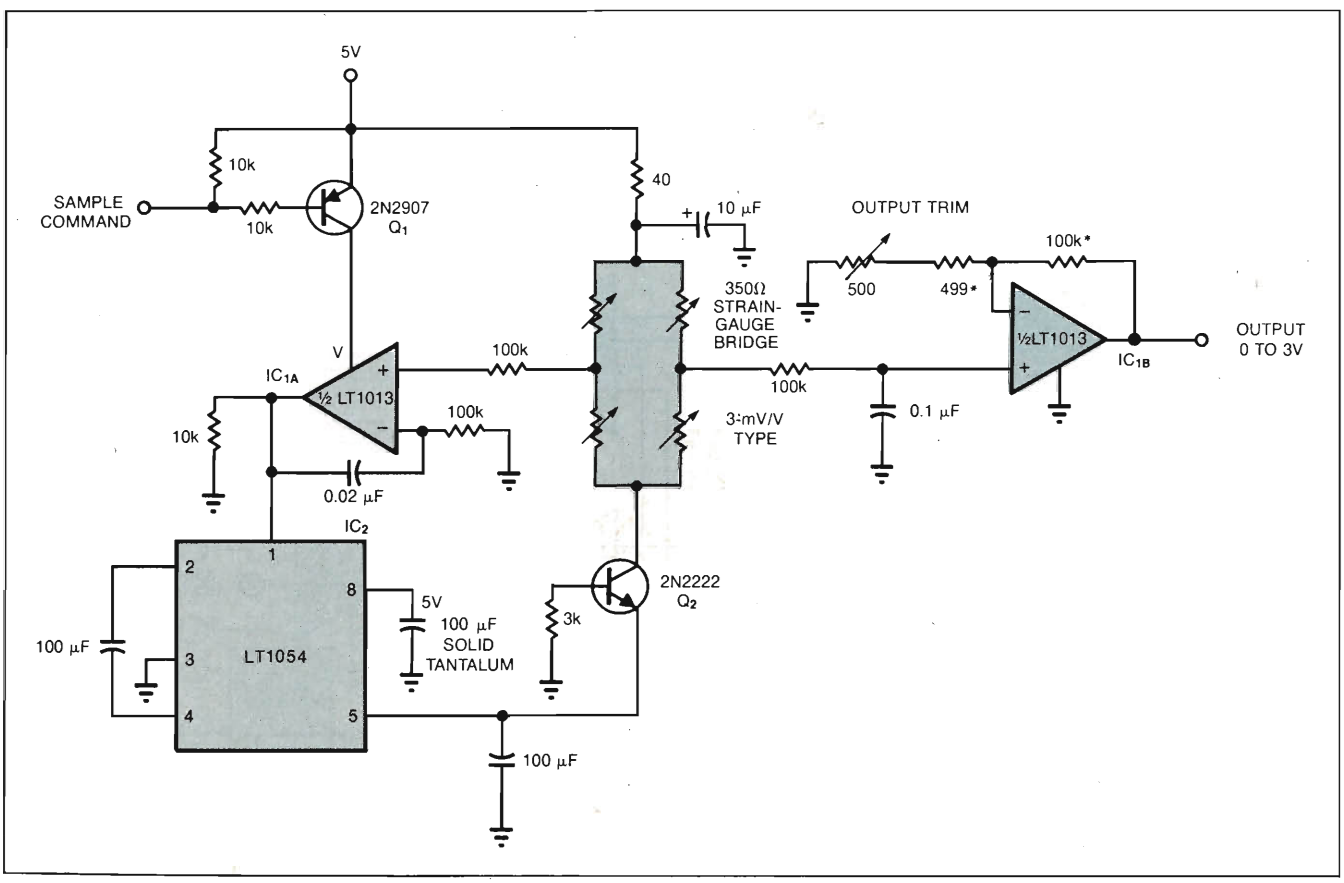


Fig 4—The strobed operation of this circuit uses only 150 μA of quiescent current. *Full-rated drive up to 50 mA occurs only on command.*

20-mA range. Accuracy for this current-loop circuit is ±0.3°C over a 0 to 100°C range. The circuit does not require an external supply.

By fixing the current well below the 4-mA minimum, the LM134 current source saves the LTC1040 from having to handle too high a supply voltage (see **box,** "Sampling techniques reduce circuit current"). The LTC1040 senses the thermistor-network output and forces this voltage across the output resistor to set the total circuit current. You can adjust the current by varying the gate voltage of the 2N6657 FET. The comparator output operates in a PWM mode, with the FET-gate voltage filtered by the 1-MΩ resistor and the 1-μF capacitor.

An important feature of the LTC1040 is that very little current—something on the order of nanoamperes —flows from the V− supply. The V− supply therefore connects to ground with negligible current error in the output-sensing resistor. The differential input of the LTC1040 can sense the current through the output resistor because its common-mode range includes the V− supply. You make the trimming adjustments for 0 and 100°C (full scale) by exposing the thermistor to those temperatures or by electrically simulating those conditions.

Fig 6 shows a circuit for a battery-powered thermostat using the LTC1041 and a bridge-connected thermistor to sense the temperature. A potentiometer at the output of the bridge provides a means of setting the temperature. The power for driving the bridge comes

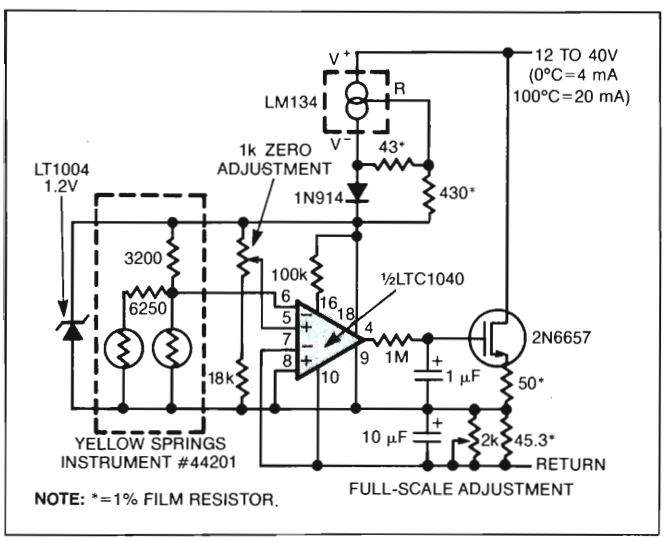


Fig 5—This 2-wire thermistor signal-conditioning circuit requires no external supply. *Powered by a current-loop, the circuit accuracy is ±0.3°C over a 100°C range.*

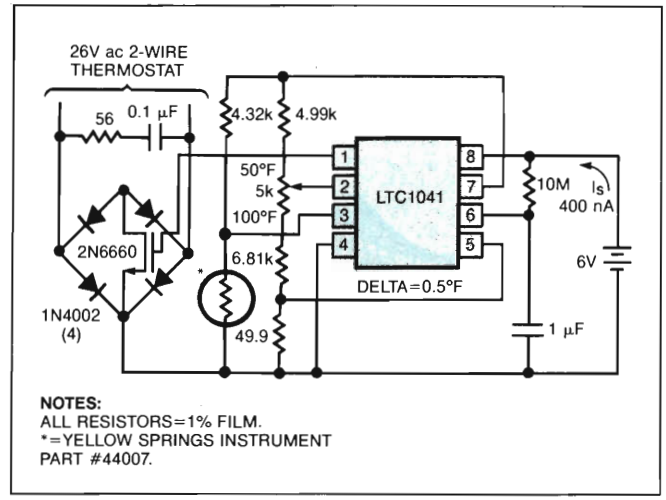


Fig 6—This thermistor-based temperature-sensing circuit uses pulse techniques to limit the current to 1 μA. *With a lithium battery, this circuit can operate for over 10 years.*

from pin 7 of the LTC1041, not from the battery. Pin 7 is the pulse-power (V_{PP}) output and only turns on when the LTC1041 samples the inputs. A system's average power consumption when this technique is used turns out to be quite small: In this application, total system current is less than 1 μA. This is far less than the self-discharge rate of the battery. A lithium battery can operate this circuit for over 10 years.

An external R-C network sets the sampling frequency. The initiation of an internal sampling cycle turns on power to the comparators and the V_{PP} output. The CMOS latches in the LTC1041 store the resulting outputs of the sampled analog inputs. After the sampling, the circuit switches off the power but keeps the outputs on. The unclocked CMOS logic consumes negligible current.

The sampling process takes approximately 80 μsec. During this interval, the LTC1041 draws about 1.7 mA of current from the 6V supply. Because the sampling rate is low, average power consumption is extremely small. The low sampling rate is adequate for a thermostat, however, because of the low rate of change associated with temperature.

A power MOSFET in the diode bridge switches 26V ac to the heater control circuitry. The MOSFET is a voltage-controlled device that requires no current from the battery. The voltage from pin 5 (DELTA) to pin 4 (GND) sets the dead band. The dead band, which is desirable to prevent excessive cycling in the heating unit under control, equals two times DELTA and is independent of both V_{IN} (pin 3) and setpoint (pin 2).

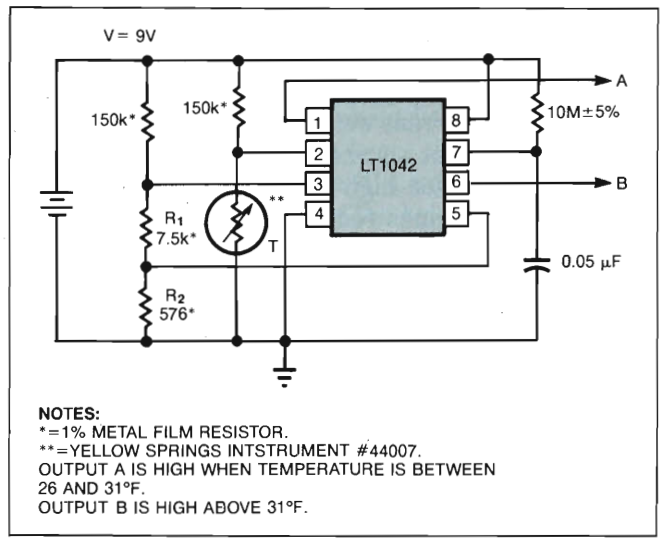


Fig 7—This simple freezer-alarm circuit draws only 80 μA of current *and uses the LTC1042 as a sampling window-comparator.*

Thus as you vary the setpoint, the dead band remains fixed at two times DELTA. Conversely, as you vary the dead band, the setpoint stays the same.

Fig 7 is a very simple configuration for a freezer alarm. Circuits such as this one are useful in industrial and home freezers as well as in refrigerated trucks and rail cars. The LTC1042 acts as a sampling window comparator. The 10-MΩ resistor and 0.05-μF capacitor set a sampling rate of 1 Hz and the bridge-network values program the internal window comparator for the outputs shown. During normal freezer operation, pin 1 is high and pin 6 is low. Overtemperature conditions reverse this state and can trigger an alarm. The circuit consumes about 80 μA. **EDN**

Author's biography

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor Corp, Arthur D Little Inc, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art, and collecting antique scientific instruments.

Article Interest Quotient (Circle One)
High 470 Medium 471 Low 472

Signal conditioning circuits use μpower design techniques

Part 1 of this 2-part series covered micropower signal conditioning for sensors and transducers. Part 2 completes the series with coverage of the types of micropower circuits and techniques required for implementing A/D converters, V/F converters, low-power regulator circuits, and a sample/hold circuit. This part also includes a discussion of the parasitic effects of test equipment on the measurement and design of micropower circuits.

Jim Williams, *Linear Technology Corp*

When designing micropower circuits, some sensors and transducers can present special problems because of the components' inherently low impedance and low output voltage (see EDN, August 6, 1987, pg 123). Although these constraints don't apply to all transducer-based circuits, other factors can affect circuit performance when attempting to operate them at micropower levels. In data converters, for example, circuit speed, accuracy, and resolution all tend to suffer at low operating current. In addition, a circuit's capacitance can slow its operation, and tradeoffs are sometimes necessary between signal levels and power dissipation.

Although integrating 12-bit A/D converters that have low power consumption are available, they are quite slow—typically in the 100-msec range. Higher speeds require a successive-approximation register (SAR). To date, no commercially produced 12-bit SAR features micropower capability, which is defined as the capability of operating below 1 mA. The design shown in **Fig 1a** converts in 300 μsec while consuming only 890 μA.

Conceptually, this design is a straightforward SAR converter, except that the circuit uses special measures to operate at low power. The circuit arranges the SAR chip and the DAC chip in the standard fashion, with IC_1 closing the loop. Normally, one would not use CMOS DACs for SAR applications because their output capacitance slows down the operation. In this case, however, the CMOS DAC's low power consumption is attractive enough that the consequently slower speed is acceptable. And because the micropower comparator (IC_1) works well with the speed of the DAC specified, the speed penalty is minimal.

One limitation of CMOS DACs is that their outputs must terminate into 0V. This constraint mandates a current-summing comparison, wherein the reference's polarity must be the opposite of the input's. Because most micropower systems run from single-sided positive rails, it's unrealistic to expect the end user to supply the A/D converter with a negative input. To be readily usable, therefore, the converter should accept positive inputs and derive a negative reference internally. IC_2 and the LTC1044 address this issue with a plus-to-minus voltage conversion that results in a negative reference. IC_2, compensated as an op amp, controls the LTC1044 via the boost transistor. The negative

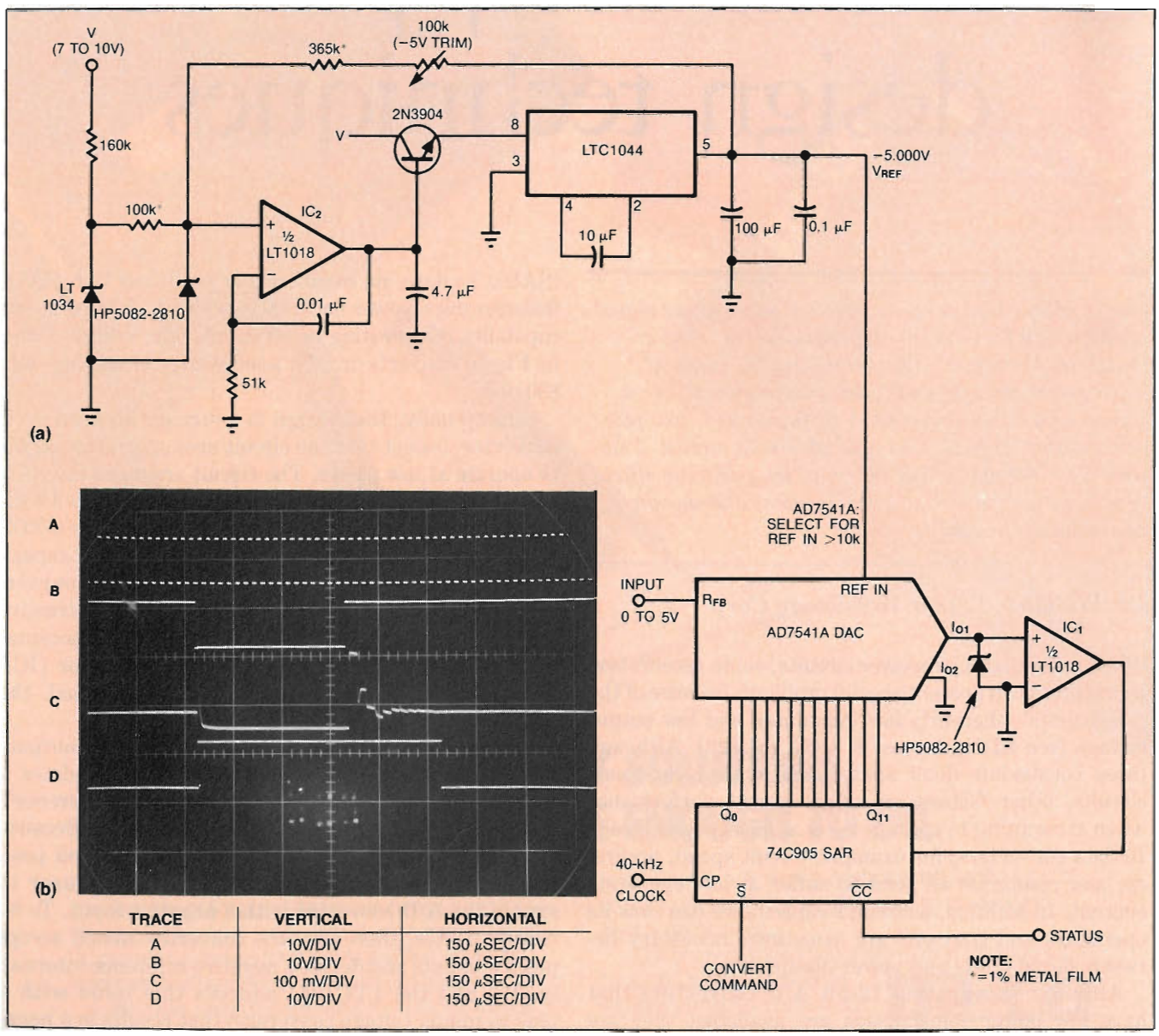
With micropower circuits you can build A/D converters that offer 10- and 12-bit resolution but consume well under 1 mA of current.

output of the LTC1044 is fed back to the input of IC_2, closing a regulation loop.

Scaled current summing from the output and from the LT1034 forces a −5.000V output. The Schottky diode prevents any negative summing-point overdrive during start-up. The 5V reference maintains a reasonable LSB overdrive for IC_1, but it accounts for over half the circuit's current requirement. (The DAC's relatively low input impedance sets this current requirement.) Dropping the reference voltage might save significant power, but it also reduces the LSB size below a millivolt. And an LSB below a millivolt causes both comparator offset and gain to become substantial error sources.

DAC accepts negative reference

Although the DAC has no negative supply, it can accept the negative reference because its thin-film resistors are extrinsic to its monolithic structure. However, IC_1, which is referred to ground, cannot accept



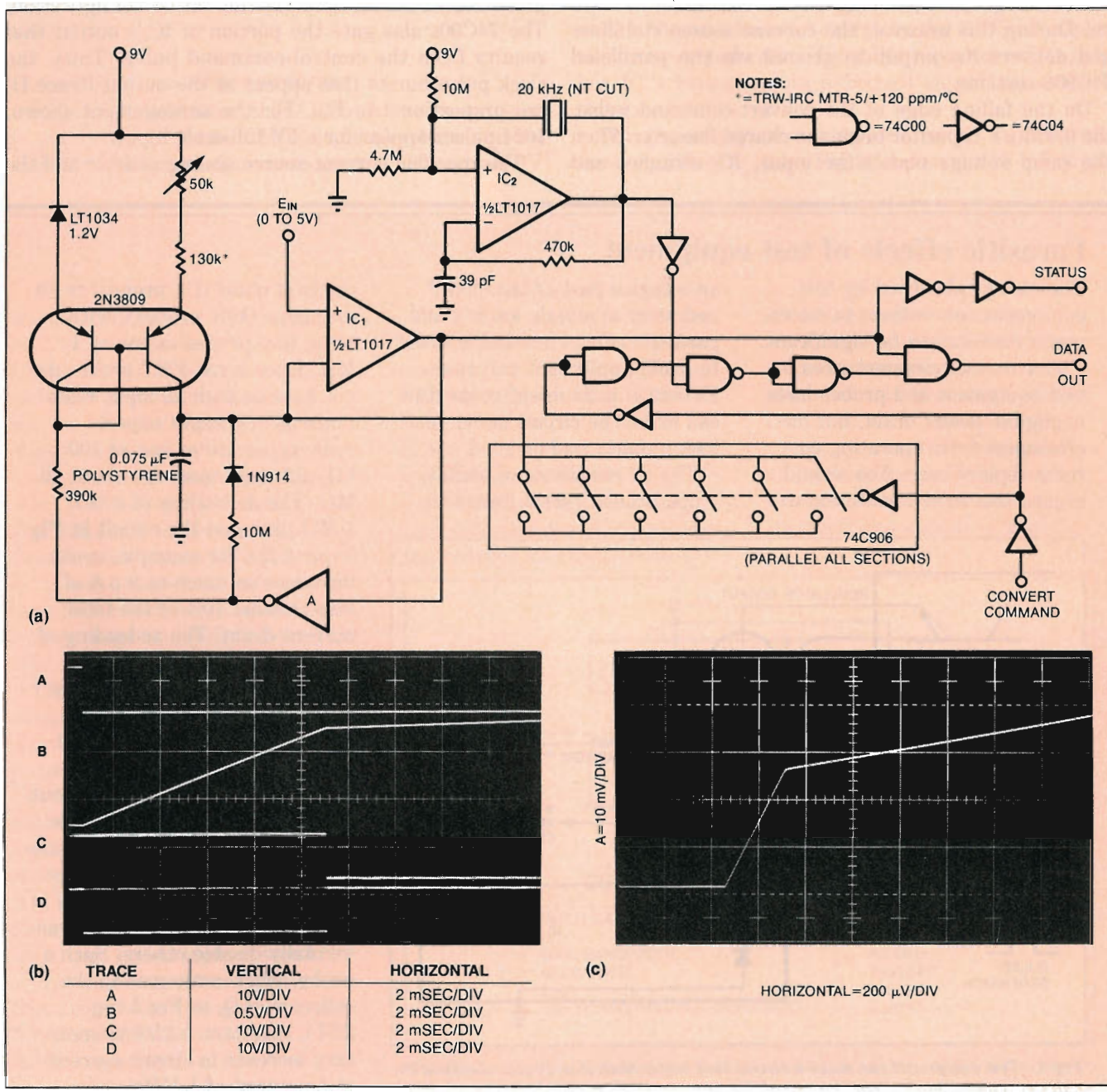
TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	150 µSEC/DIV
B	10V/DIV	150 µSEC/DIV
C	100 mV/DIV	150 µSEC/DIV
D	10V/DIV	150 µSEC/DIV

Fig 1—This 12-bit A/D converter needs only 890 µA of current. *It uses a successive approximation approach that provides conversion in 300 µsec.*

any negative voltages and is clamped by the Schottky diode. Overall performance specifications include typical temperature compensation of 30 ppm/°C, a 300-μsec conversion time, an 890-μA current consumption, and an accuracy of ±2 LSBs. To trim, adjust the 100-kΩ resistor for exactly −5V at V_{REF}.

The DAC's internal feedback resistor serves as the input. In **Fig 1b,** trace A is the clock, and trace B is the convert command. Trace B's falling edge clears the SAR, and conversion commences on its rise. During conversion, IC_1's input (trace C) sequentially converges towards zero. When conversion is complete, the status line (trace D) drops low.

The 10-bit A/D converter shown in **Fig 2a** has less



TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	2 mSEC/DIV
B	0.5V/DIV	2 mSEC/DIV
C	10V/DIV	2 mSEC/DIV
D	10V/DIV	2 mSEC/DIV

Fig 2—Using CMOS logic elements and a low-current comparator, *this 10-bit A/D converter requires only 100 μA of current.*

An S/H circuit that has a 20-μsec acquisition time and a hold current of 430 μA uses low-current op amps, CMOS logic, and a handful of discrete components.

resolution than the previous circuit, but it does operate at the much lower current of 100 μA. The design consists of a current source, an integrating capacitor, a comparator, and some logic elements. With a pulse applied to the convert-command input (trace A, **Fig 2b**), the paralleled 74C906 sections reset the 0.075-μF capacitor to zero (trace B). Simultaneously, 74C04 inverter A goes low, biasing the 2N3809 current source on. During this interval, the current source stabilizes and delivers its output to ground via the paralleled 74C906 sections.

On the falling edge of the convert-command pulse, the 0.075-μF capacitor begins to charge linearly. When the ramp voltage equals the input, IC_1 switches and inverter A goes high, shutting off the current source. A small current is bled through the 10-MΩ resistor and the 1N914 diode to keep the ramp charging at a lower rate. That current ensures overdrive for IC_1 but minimizes the current source's on time and so saves power. The 0 to 5V input voltage (E_{IN}) to IC_1 directly determines the output pulse width (trace C). This pulse gates IC_2's clock output via the 74C00 configuration. The 74C00s also gate the portion of IC_1's output that results from the control-command pulse. Thus, the clock pulse bursts that appear at the output (trace D) are proportional to E_{IN}. For the arrangement shown, 1024 pulses appear for a 5V full-scale input.

The specified current-source scaling resistor and the

Parasitic effects of test equipment

The energy absorbed by test-equipment connections to micropower circuits can be significant. Under normal circumstances, test equipment and probes have negligible power drain, but microampere-level operating currents require care. You should regard test instrumentation as an integral part of the circuit and keep ac and dc loading and parasitic effects in mind in order to avoid unpleasant surprises. Errors in instrument connection can make the circuit under test look unfairly bad or good.

The dc resistance of oscilloscope probes varies from hundreds of ohms (1× probes) to 10 megohms (10× probes), with some 10× probes as low as 1 MΩ. Even some FET probes do not have as high an input resistance as one might expect—some types are as low as 100 kΩ, although most are about 10 MΩ. The dc loading of a 10× 1-MΩ probe on the circuit in **Fig 2** (pg 221), for example, could introduce as much as 9 μA of loss—almost 10% of the total current drain. The ac loading of a 10-pF probe, using **Fig 2**'s 20-kHz clock as a test example, increases circuit current by 5 μA momentarily, a significant loss in a low-power circuit.

Most 1× probes present about 50-pF loading, with a 1-MΩ dc resistance when connected to the oscilloscope. This kind of probe loading can cause large errors in some micropower circuits; it can virtually disable others. Such a probe, when connected to the collector of Q_8 in **Fig 5** (pg 227), results in a 25% momentary increase in circuit current at an output of 1 MHz.

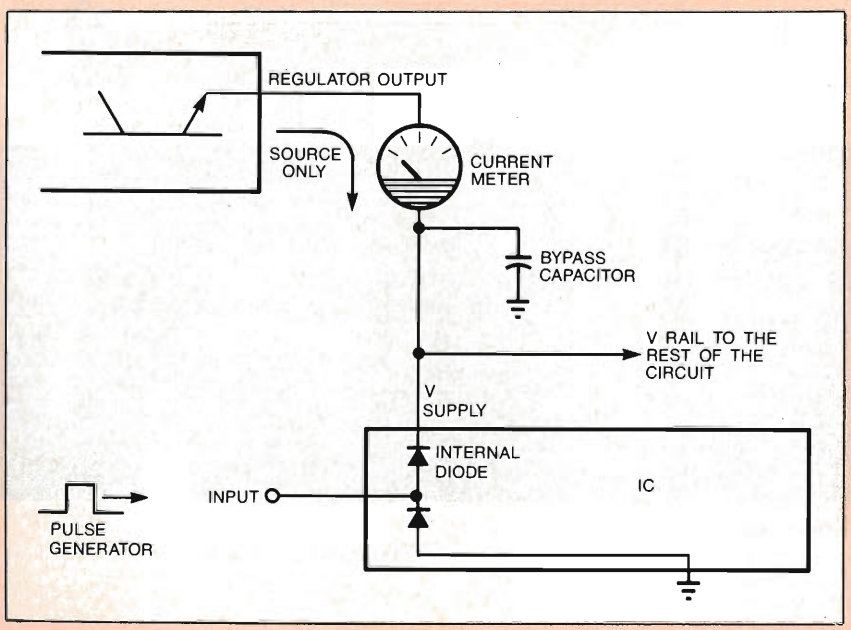


Fig A—Test equipment can make a circuit look better than it is. *If you misadjust the pulse generator, for example, the circuit functions when the current meter reads zero.*

specified ramp capacitor provide good temperature compensation because of their opposing thermal coefficients. The circuit typically maintains an accuracy of ±1 LSB over the temperature range of 0 to 70°C; the asynchronous relationship between the clock and the conversion sequence causes an additional ±1 LSB. The conversion rate varies with the input voltage. At ⅒ scale, 150 Hz is possible; at full scale, the rate decreases to 20 Hz.

Lowest power sacrifices accuracy

Power consumption of this A/D converter is extremely low because of the CMOS logic elements and the LT1017 comparator. Quiescent current (E_{IN} equals 0V) is 100 μA at a supply voltage of 9V, decreasing to 80 μA at 7V. Because the time that the current source is on varies with the input, power consumption also varies with E_{IN}. When E_{IN} equals 5V, current drain rises to 125 μA with a 9V supply and 105 μA at 7V. You can save more power if you shut off the current source during the capacitor reset, but you lose accuracy because of the current source's settling-time requirements. The accumulated charge on the 0.075-μF capacitor is lost at each reset. A smaller capacitor might help, but IC_1's bias currents introduce significant error in this case.

Turning off the current source after IC_1 switches also saves significant power. **Fig 2c**, taken at a 25-mV input,

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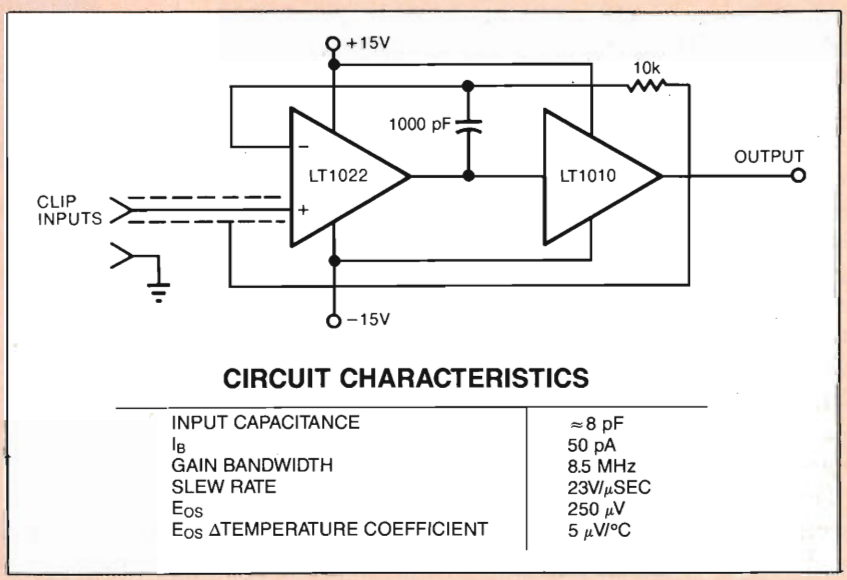
Probe ac and dc loading are not the only effects. The input switching networks of some DVMs (digital voltmeters) sink or source a parasitic charge. Such a parasitic charge, when introduced into high-impedance nodes, can cause substantial errors. It's also worth remembering that DVM dc loading may change with the range it is set to: Lower ranges may have a very high input impedance, but higher ranges typically have only 10 MΩ.

Fig A shows a way that test equipment can make the circuit look too good. If you adjust the pulse generator more than a typical diode voltage drop above the regulator's output, the bypass capacitor will detect the peak charge delivered through the IC's internal diode. The regulator can't sink current, and, with its output forced high, it won't source anything either. Under these conditions, the circuit functions when the current meter reads zero—a very low-power circuit indeed.

A very simple and useful circuit **(Fig B)** greatly aids probe-loading problems in micropower circuits. The LT1022 high-speed FET op amp drives an LT1010 buffer. The output of the LT1010 drives the DVM cable and probe and also biases the circuit's input shield. This connection bootstraps the input capacitance and reduces its effect. Both the dc and ac errors of this circuit are low enough for nearly all work, with enough bandwidth for most low-power circuits. If you build this circuit in a small enclosure with its own power supply, you can use it ahead of an oscilloscope or DVM with good results. The pertinent specifications appear in **Fig B.**



CIRCUIT CHARACTERISTICS

INPUT CAPACITANCE	≈8 pF
I_B	50 pA
GAIN BANDWIDTH	8.5 MHz
SLEW RATE	23V/μSEC
E_{OS}	250 μV
E_{OS} ΔTEMPERATURE COEFFICIENT	5 μV/°C

Fig B—To aid in probe-loading problems, *this circuit provides ac and dc errors that are low enough for nearly all work.*

Using micropower circuits and appropriate design techniques, 10-kHz and 1-MHz V/F converters need only 145 μA and 635 μA of current, respectively.

shows the ramp zero reset and clean switching. When the current source switches off, the ramp slope decreases but still continues to move upward, ensuring overdrive. The 10-MΩ resistor and the 1N914 diode provide the charge, and less than a microampere is lost.

Fig 3a shows a companion sample/hold circuit for the SAR A/D converter. The acquisition time is 20 μsec, with low-power operation (see table in **Fig 3a**). This circuit takes full advantage of the programming pin on the LT1006 op amp to maximize both speed and power specifications. When the sample command (trace A, **Fig 3b**) is given, the CO4066 switch closes. S_1 and S_2 allow the output of IC_1 (trace B) to charge the capacitor (trace C is the capacitor current). S_3 and S_4 also close, raising the op amp's internal bias network.

At that point, both amplifiers then go into hyperdrive, boosting the slew rate in order to speed the acquisition time. IC_2 (trace D) settles cleanly to 1 mV in 20 μsec. When the sample command goes low, all switches go off, IC_2 follows the voltage stored on the capacitor, and the supply current drops by a factor of five (see the table in **Fig 3a**). In normal operation, the sampling time is short compared to the holding time, and current consumption is low. The 360-kΩ resistors set the circuit's hold-mode quiescent current at 430 μA.

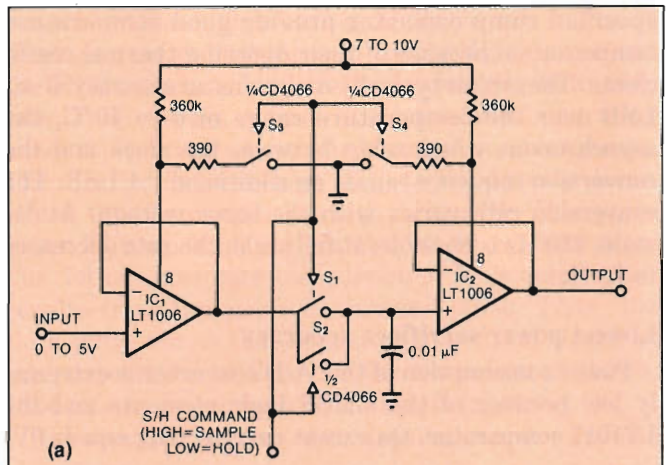
V/F converters also work at low current

Another data converter, this one a voltage/frequency (V/F) converter, is shown in **Fig 4a**. A 0 to 5V input produces a 0- to 10-kHz output with a linearity of 0.02% and a gain drift of 40 ppm/°C. Maximum current consumption is only 145 μA, far below that required by most other circuits.

To understand how the **Fig 4** circuit operates, assume that the positive input to IC_1 is slightly below its negative input and that the output of IC_2 is low. The input voltage causes a positive ramp at the input of IC_1 (trace A, **Fig 4b**). IC_1's low output biases the CMOS-inverter outputs high. This bias allows current to flow from Q_1's emitter through the inverter supply pin to the 0.001-μF capacitor. The 10-μF capacitor provides a high-frequency bypass, maintaining a low impedance at Q_1's emitter. Connected like a diode, Q_6 provides a path to ground.

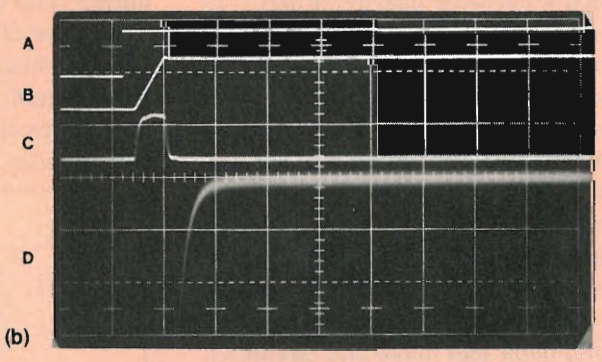
The 0.001-μF capacitor charges to a voltage that is a function of Q_1's emitter potential and the drop across Q_6. When the ramp at the positive input of IC_1 goes high enough, IC_1's output goes high (trace B) and the inverters switch low (trace C). The Schottky clamp prevents a CMOS-inverter input overdrive. This preventative action also pulls current from the capacitor at the positive input of IC_1 via Q_5 and the 0.001-μF capacitor (trace D). This removal of current resets IC_1's positive input ramp to a potential slightly below ground and thus forces the output of IC_1 to go low.

The 50-pF capacitor connected to the circuit output furnishes positive ac feedback, ensuring that the output



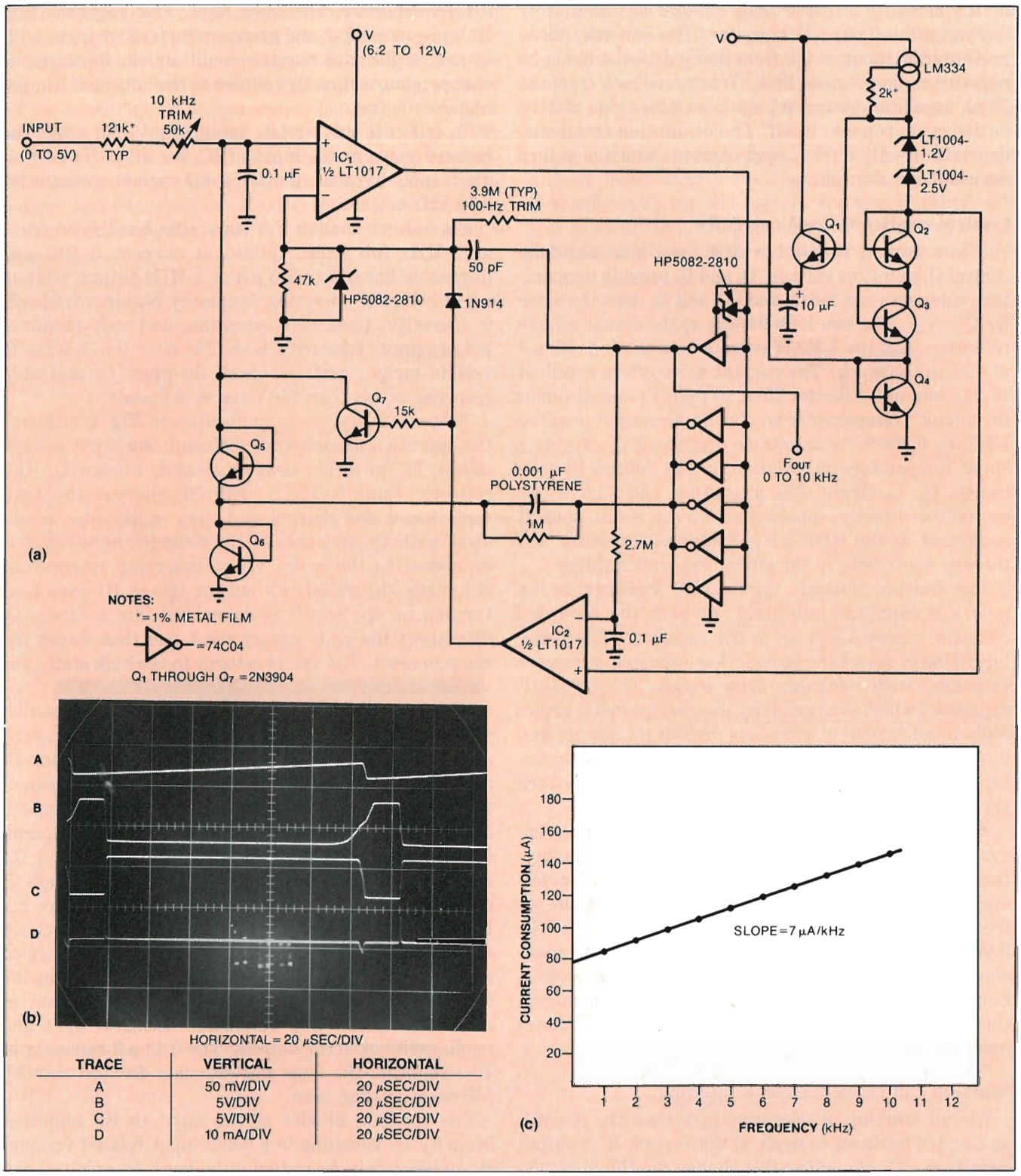
CIRCUIT CHARACTERISTICS

ACQUISITION TIME	20 μSEC
HOLD SETTLING TIME	10 μSEC
S/H OFFSET	1 mV
HOLD SUPPLY CURRENT	430 μA
SAMPLE SUPPLY CURRENT	2.2 mA
1-kHz-SAMPLE-RATE CURRENT	875 μA
DROOP RATE	1 mV/mSEC



TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	10 μSEC/DIV
B	5V/DIV	10 μSEC/DIV
C	10 mA/DIV	10 μSEC/DIV
D	5 mV/DIV	10 μSEC/DIV

Fig 3—A companion for the A/D converters, *this sample/hold circuit has a 20-μsec acquisition time and a hold-current of 430 μA.*



TRACE	VERTICAL	HORIZONTAL
A	50 mV/DIV	20 μSEC/DIV
B	5V/DIV	20 μSEC/DIV
C	5V/DIV	20 μSEC/DIV
D	10 mA/DIV	20 μSEC/DIV

Fig 4—Linearity for this V/F converter is 0.02%; a 0 to 5V input produces a 0- to 10-kHz output. Maximum current consumption is 145 μA.

Switching regulators are useful in limiting quiescent current while still providing higher output currents.

of IC_1 remains positive long enough to completely discharge the 0.001-μF capacitor. The Schottky diode prevents the input of IC_1 from being driven outside its negative common-mode limit. When feedback from the 50-pF capacitor decays, IC_1 again switches low, and the entire cycle repeats itself. The oscillation frequency depends directly on the input current, which is in turn derived from the voltage.

Control emitter voltage carefully

If you want to obtain low drift, you must carefully control Q_1's emitter voltage. Q_3 and Q_4 provide temperature compensation for Q_5 and Q_6, and Q_2 does the same for Q_1's V_{BE}. The two LT1004s act as the actual voltage reference, and the LM334 current source sends 35 μA of bias to the stack. The current drive offers excellent supply immunity (better than 40 ppm/V) and also aids the circuit's temperature coefficient because it uses the LM334's 0.3%/°C temperature coefficient to provide a slight temperature modulation on the voltage drop in the Q_2, Q_3, Q_4 string. The magnitude and sign of this correction directly oppose that of the −120 ppm/°C coefficient of the 0.001-μF polystyrene capacitor and thereby contribute to the circuit's overall stability.

The emitter follower, Q_1, delivers a charge to the 0.001-μF capacitor efficiently, as both the base and collector currents end up in the capacitor. The paralleled CMOS inverters provide low-loss spdt reference switching with minimum drive losses. The 0.001-μF capacitor, which is as small as accuracy permits, draws only small transient currents during its charge and discharge cycles, and a combination of the 50-pF capacitor and the 47-kΩ resistor produces positive feedback that draws insignificant switching currents.

Fig 4c, a plot of supply current vs operating frequency, reflects the low-power design. At zero frequency, the LT1017's quiescent current and the 35-μA reference-stack bias accounts for all of the current drain. As frequency increases, the charge-discharge cycle of the 0.001-μF capacitor introduces the 7-μA/kHz increase shown. A capacitor of a smaller value would cut power, but the effects of stray capacitance, charge imbalance in the 74C04, and LT1017 bias currents would introduce inaccuracies.

Start-up can cause feedback latching

Circuit start-up or overdrive can cause the circuit's ac-coupled feedback to latch. If this occurs, IC_1's output goes high. IC_2, detecting this change via the inverters and via the lag caused by the 2.7-MΩ resistor and the 0.1-μF capacitor, also goes high. This sequence lifts IC_1's negative input and grounds the positive input with Q_7 and so initiates normal circuit action. Because the charge pump is directly coupled to the output of IC_1, the response is fast.

To calibrate this circuit, apply 50 mV and select the resistor value at the input of IC_1 for a 100-Hz output. Then apply 5V and trim the 50-kΩ variable resistor for a 10-kHz output.

Fig 5 shows another V/F converter, but this one runs at 1 MHz full scale. Quiescent current is 245 μA, increasing linearly to 635 μA at 1-MHz output. Obtaining this higher operating frequency requires tradeoffs in linearity, power consumption, and step-response performance. Linearity is 0.12% over the 100-Hz to 1-MHz range; drift is about 50 ppm/°C; and step response is less than 350 msec to full scale.

This circuit has some similarities to **Fig 4**, although the operation is somewhat different. An input voltage causes IC_1 to swing toward ground, biasing Q_8. Q_8's collector ramp (trace A, **Fig 5b**) charges the 3-pF capacitor; it also charges any stray capacitance associated with Q_7 and the 74C14 Schmitt input that is connected to the node. When the ramp reaches the Schmitt's threshold, its output (trace B) goes low, turning on Q_7, which is connected like a diode. Q_7 discharges the node capacitances and thus forces the ramp to reset. The 74C14 returns to the high state, and oscillation commences.

A second 74C14 section (trace C) inverts this oscillation signal, drives the 74C90 dividers, and serves as the circuit's output. The dividers' ÷100 output (trace D) controls a reference charge-pump arrangement essentially identical to the one in **Fig 4**. The 1000-pF capacitor is alternately charged and discharged by the paralleled 74C14 sections and steering diodes Q_5 and Q_6, respectively. The charge increments pulled through Q_5 continually force IC_1's 2-μF capacitor to zero (trace E), balancing the input-derived current. This action closes a loop around IC_1 and thus controls the oscillator, which consists of Q_7, Q_8, and the 74C14, so that it runs at the frequency needed to keep its own negative input at zero. This closed loop eliminates oscillator drift and nonlinearity as error sources. The 0.33-μF capacitor at IC_1 stabilizes the loop and accounts for the circuit's 350-msec settling time.

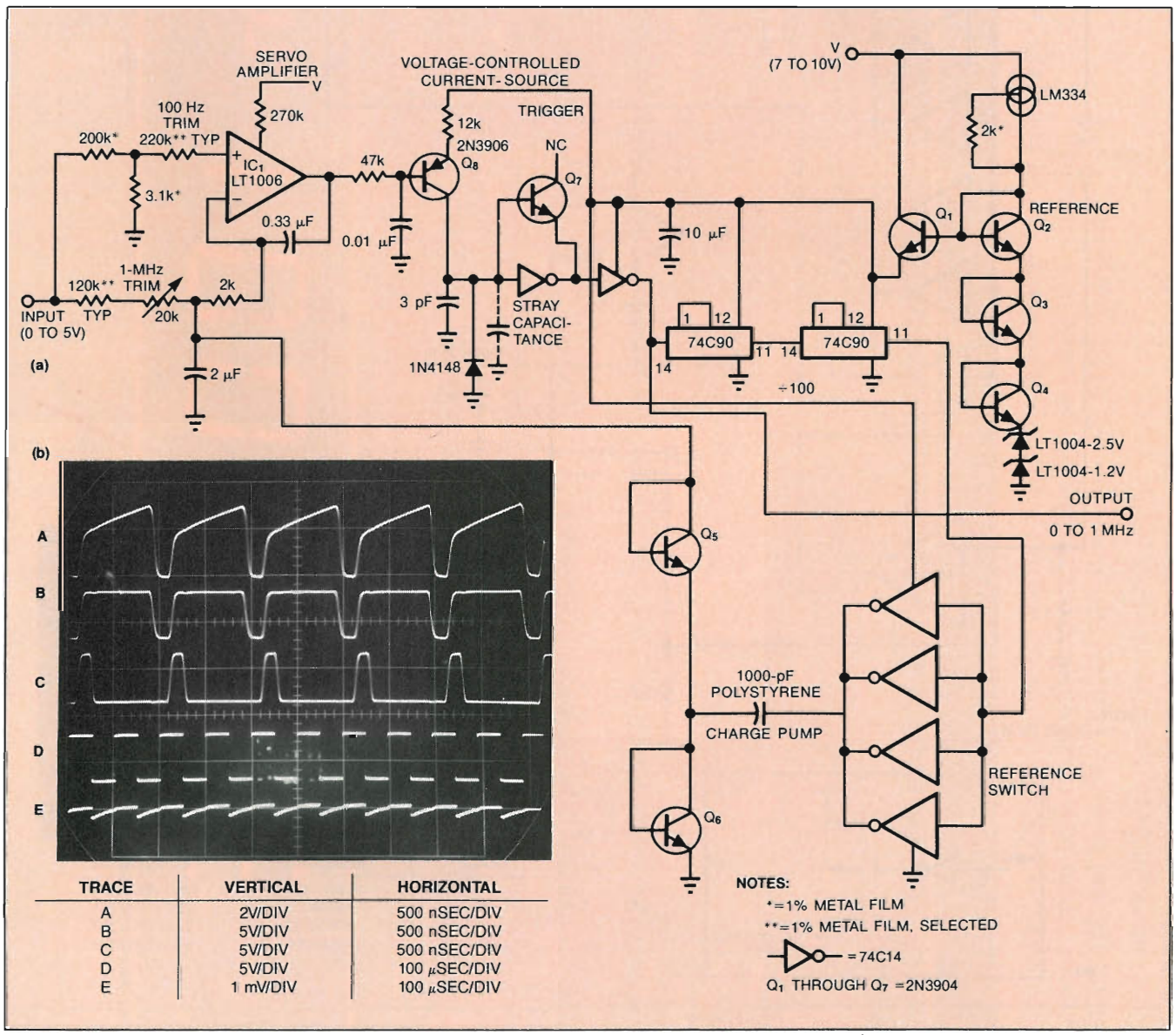
The resistive divider at the input to IC_1 improves linearity by summing in a small input-related voltage. By deliberately introducing leakage to ground, the diode at the collector of Q_8 dominates all node leakages.

This leakage control ensures low-frequency operation by forcing Q_8 to source current for oscillation purposes.

Although low, the current drain of the **Fig 5** circuit is higher than the one shown in **Fig 4**, primarily because of the former's high-frequency oscillator and its divider operation. The capacitance and the signal swing at the collector of Q_8 heavily influence the oscillator's current. The 74C14 threshold voltage determines the signal swing, and the capacitance value is the lowest possible value commensurate with the desired low-frequency operation.

To trim this circuit, apply 500 μV to the input and select the 220-kΩ (typ) resistor value at the positive input of IC_1 for an output frequency of 100 Hz. Then, with a 5V input, adjust the 20-kΩ variable resistor for 1-MHz output. Repeat this procedure until both points are fixed.

Any discussion of micropower circuitry is incomplete without mentioning switching regulators. Often you must efficiently convert battery voltages to other voltages to meet circuit requirements. **Fig 6** shows a buck switching regulator with a quiescent current of 70 μA



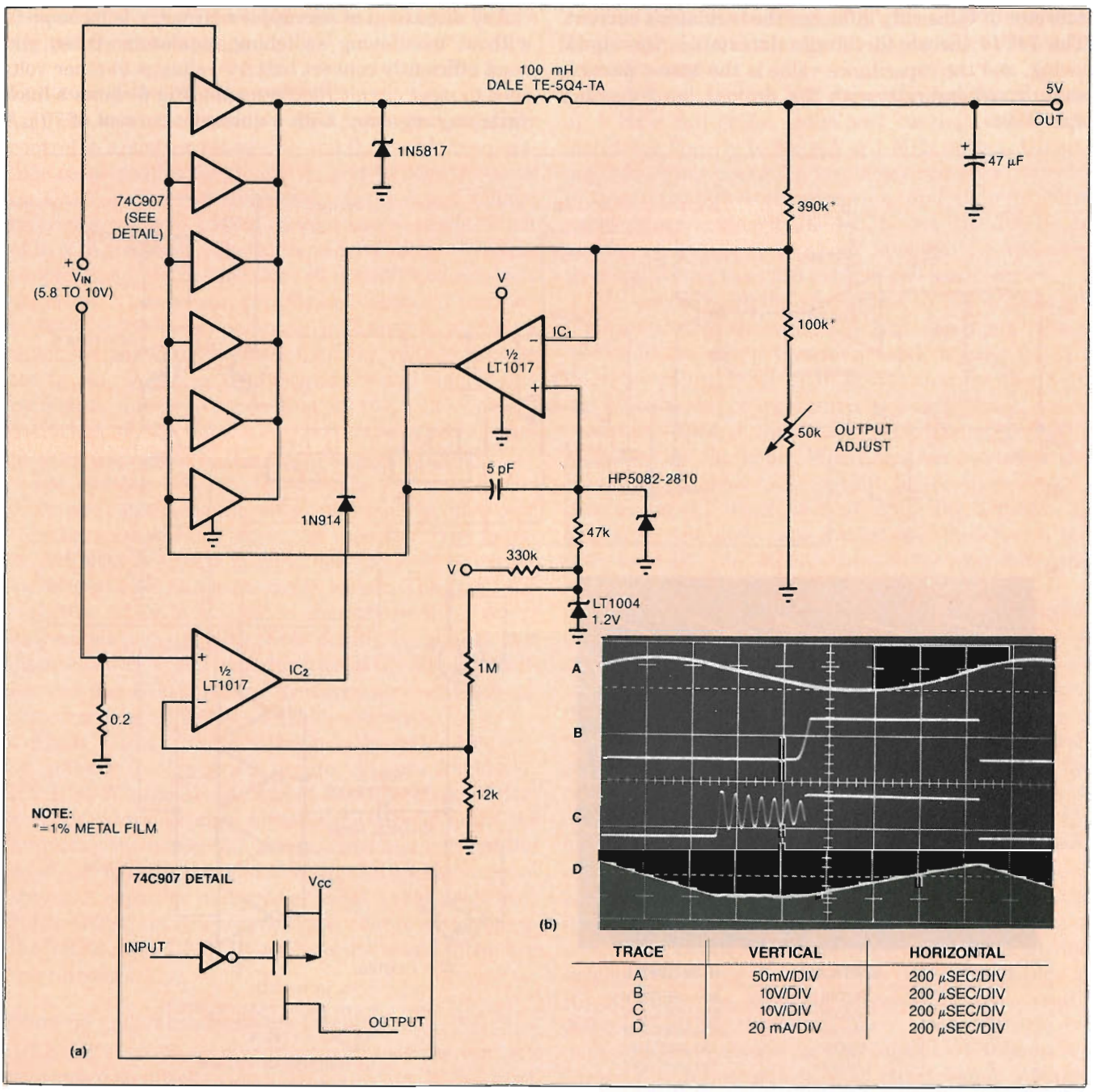
TRACE	VERTICAL	HORIZONTAL
A	2V/DIV	500 nSEC/DIV
B	5V/DIV	500 nSEC/DIV
C	5V/DIV	500 nSEC/DIV
D	5V/DIV	100 μSEC/DIV
E	1 mV/DIV	100 μSEC/DIV

Fig 5—This V/F converter needs from 245 to 635 μA to operate, *but it will run at 1 MHz full scale. Linearity is 0.12% over 100 Hz to 1 MHz.*

You should regard test instrumentation as an integral part of the circuit when evaluating any circuit design.

and an output-current capability of 20 mA. When the output voltage drops (trace A, **Fig 6b**), the negative input of IC_1 also falls, causing its output (trace B) to rise. This turns on the paralleled 74C907 open-source buffers, and their outputs (trace C) consequently go high. Current increases through the inductor and maintains the regulator output. When the output voltage rises a little, IC_1's output goes low again, and the cycle repeats itself.

In spite of line and load changes, this action main-



TRACE	VERTICAL	HORIZONTAL
A	50mV/DIV	200 µSEC/DIV
B	10V/DIV	200 µSEC/DIV
C	10V/DIV	200 µSEC/DIV
D	20 mA/DIV	200 µSEC/DIV

Fig 6—With a quiescent current drain *of only 70 µA and an output capability of 20 mA, this buck switching regulator can efficiently convert battery voltages to lower circuit-voltage requirements.*

A linear postregulator can provide lower noise than a straight switching approach.

tains a constant regulator output. The LT1004 serves as a reference, and the 5-pF capacitor ensures clean switching at IC_1. The 2810 Schottky diode prevents negative overdrive caused by the 5-pF capacitor's differentiated response, and the 1N5817 catching diode prevents excessive inductor-caused negative voltages.

The circuit's low quiescent current results from the LT1017's low operating current and the 74C907's low input-drive requirements. The circuit's resistor values are kept high to save current. IC_2 shuts down the regulator when output current exceeds 50 mA by comparing the voltage across the 0.2Ω shunt to the voltage across a resistively divided portion of the LT1004 reference. Excessive current drain trips IC_2 high and so forces IC_1's negative input high. This action removes drive from the 74C907 buffers and shuts down the regulator. Using a CMOS buffer as a pass switch for a switching regulator is unusual, but the results are quite good. Efficiencies as high as 90% are possible with an output current to 20 mA.

Linear postregulator reduces noise

Another buck switching regulator **(Fig 7a)** features a low-loss linear postregulator, a quiescent current of 40 μA, and an output current to 50 mA. The LT1020 linear regulator provides lower noise than would a straight

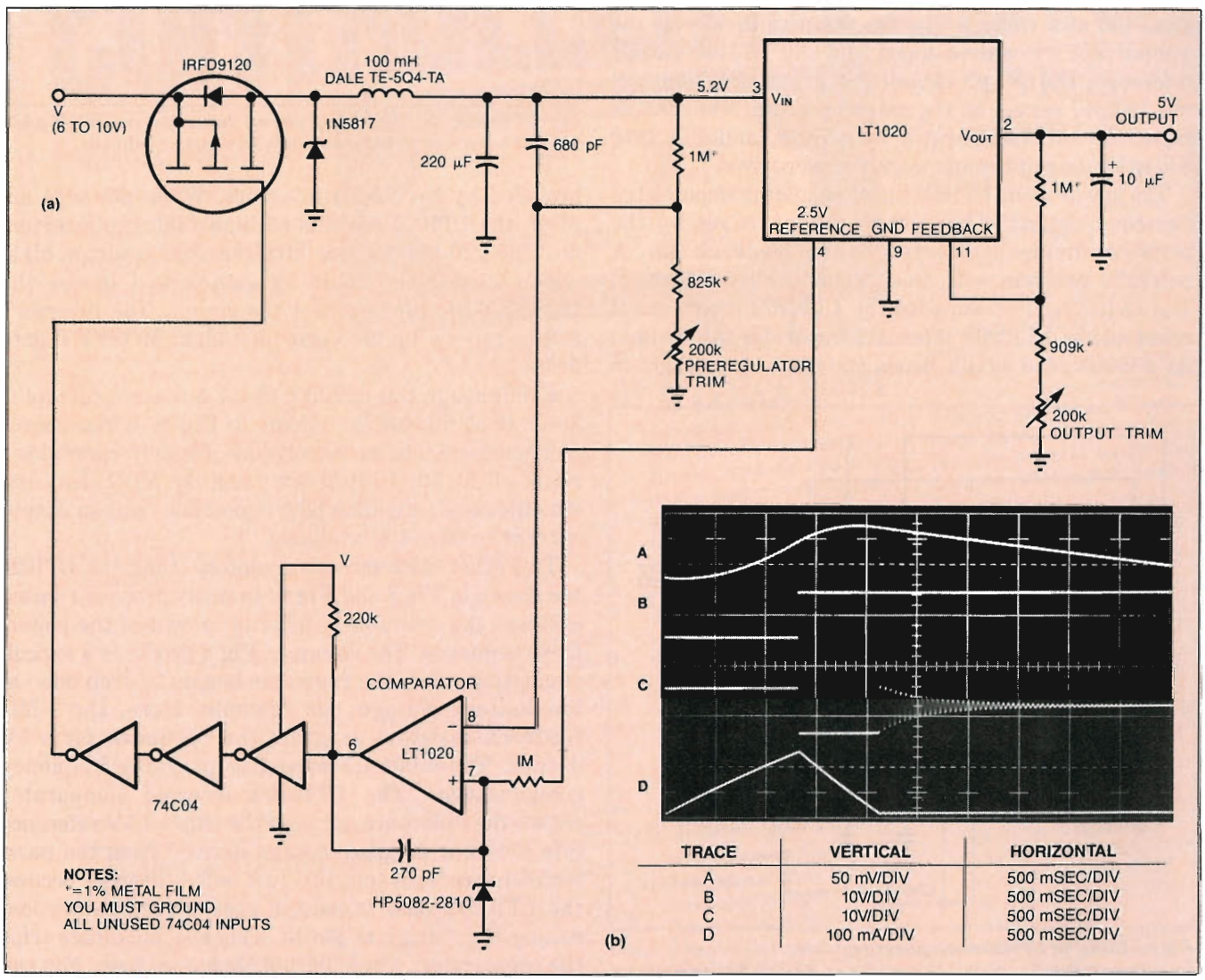


Fig 7—This buck switching regulator circuit includes a linear postregulator. *Providing a smoother output and lower noise than a straight switching regulator, this circuit has a quiescent current of only 40 μA and an output-current capability of 50 mA.*

In many processor-based systems, it's desirable to monitor or control the power-down sequence.

switching approach. It also offers internal current limiting and contains an auxiliary comparator that helps form the switching regulator in this circuit.

The switching loop is similar to that of the previous circuit. A drop at the output of the switching regulator (pin 3 of the LT1020 regulator, trace A in **Fig 7b**) causes the LT1020's comparator to go low. The 74C04 inverter chain switches and so biases the gate of the p-channel MOSFET (trace B). The MOSFET turns on (trace C), delivering current to the inductor (trace D). When the voltage at the junction of the inductor and the 220-μF capacitor goes high enough (trace A), the comparator switches high and turns off current flow in the MOSFET. This switching loop regulates the LT1020's input pin at a value set by the resistive divider at the comparator's negative input and the LT1020's 2.5V reference. The 680-pF capacitor stabilizes the loop, and the 1N5817 serves as the catching diode. The 270-pF capacitor aids comparator switching, and the 2810 Schottky diode prevents negative overdrives.

The low dropout LT1020 linear regulator smooths the switched output. The output voltage is set by the resistive divider connected to the feedback pin. A potential problem with this circuit involves start-up. The switching loop supplies the LT1020's input, but it relies on the LT1020's internal comparator to function. As a result, the circuit needs the start-up mechanism

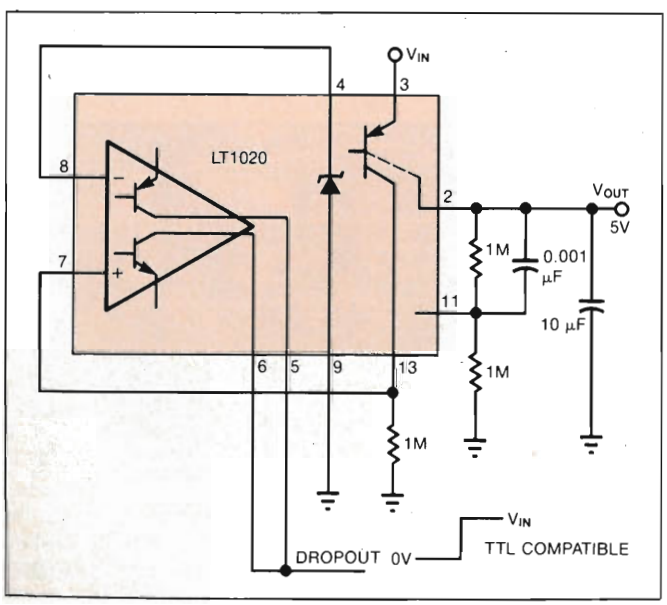


Fig 8—Using an LT1020 micropower regulator, *this circuit is useful in processor-based systems to monitor or control the power-down sequence. It produces a logical-one output when the regulator drops out.*

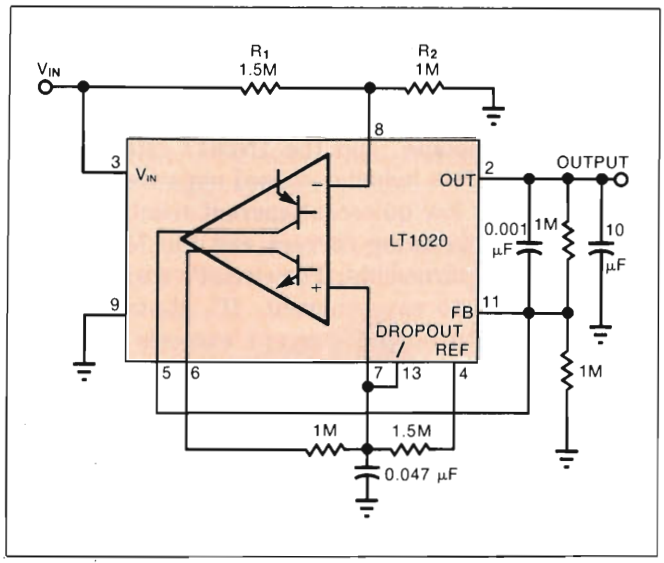


Fig 9—Similar to Fig 8, this circuit turns the power off when dropout occurs, *preventing unregulated supply conditions.*

provided by the 74C04 inverters. When power is applied, the LT1020 receives no input, but the inverters do. The 220-kΩ resistor lifts the first inverter high, which causes the chain to switch and biases the MOSFET in order to start the circuit. The inverter's rail-to-rail swing also provides ideal MOSFET gate drive.

Even though this circuit's 40-μA quiescent current is lower than that of the circuit in **Fig 6**, it can source more current. The extremely low quiescent current is a result of the low LT1020 drain and the MOS elements. An efficiency exceeding 80% is possible, and an output current to 50 mA is available.

Two other micropower regulators using the LT1020 are shown in **Fig 8** and **Fig 9**. In many processor-based systems, it's desirable to monitor or control the power-down sequence. The circuit in **Fig 8** produces a logical-one output when the regulator begins to drop out—at low battery voltage, for example. Here, the 1-MΩ feedback resistors program the regulator for a 5V output. The 0.001-μF capacitor provides frequency compensation. The LT1020's internal comparator senses the difference between the chip's 2.5V reference (pin 4) and a sampled voltage derived from the pass-transistor current (pin 13). Just before dropout occurs, the LT1020's pass transistor goes toward saturation, raising the voltage at pin 13. This rise in voltage trips the comparator, whose output then goes high. You can use this signal to alert a processor whose power is about to go down.

Fig 9 is similar, except that this circuit turns the power completely off when dropout occurs, preventing unregulated supply conditions. The comparator feedback arrangement is for a hysteretic response. The output turns off at dropout if

$$\text{TURN ON} = V_{IN} \times \frac{R_2}{R_1 + R_2} = 2.5V.$$

This setup prevents gradual battery-voltage reapplication, which can cause oscillation. **EDN**

Author's biography

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor Corp, Arthur D Little Inc, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art, and collecting antique scientific instruments.

Article Interest Quotient (Circle One)
High 494 Medium 495 Low 496

Designer's Guide to
Switching Power Supplies
Part 1

Regulator IC speeds design of switching power supplies

In part 1 of this 2-part series, you'll learn about simple switching regulators and a technique for stabilizing switching-supply feedback loops. Part 2, scheduled for the November 26th issue, will pick up where this article leaves off and delve into more complex, isolated switching power supplies.

Jim Williams, *Linear Technology Corp*

Switching power supplies are among the most difficult circuits to design. Mysterious operational modes; sudden, seemingly inexplicable failures; peculiar regulation characteristics; and just plain explosions are common occurrences. Diodes conduct the wrong way. Things get hot that shouldn't. Capacitors act like resistors, fuses don't blow, and transistors do. The output is at ground, and the ground terminal shows volts of noise.

In addition, there's the regulator's feedback loop, sampled in nature and replete with uncertain phase shifts. And of course everything varies with line and load conditions. A glance through conference proceedings and available literature yields either an undigestible store of mathematics or absurdly coy and simple little block diagrams that make everything look *so* easy.

Most engineers who need switching supplies don't require 98.2% efficiency or 100W/in^3. They aren't trying to get tenure, and they don't care about inventing a new type of circuit. What they do want are concepts directly applicable to the construction of working circuits that use readily available parts.

Standard parts ease startup

The circuits in this article employ standard, off-the-shelf magnetics exclusively, because most of the problems with switching power supplies center on the inductive components. The standard-magnetics approach almost certainly precludes precisely optimized performance and may horrify some veteran switching-supply designers, but it also eliminates inductor-construction uncertainties, saves time, and greatly increases your chances of getting a design running. A functional circuit is much easier to work with—and get enthusiastic about—than the smoking carcass of a decimated breadboard. Although the characteristics of standard inductors aren't optimal, it's easier to evaluate the performance of a working circuit on an oscilloscope than to guess why you don't see anything at all.

Also, once your circuit is running, you can obtain an optimized version of the standard product from the inductor manufacturer. Generally, the manufacturer can more easily modify its standard product than start from scratch. The process of communicating and translating circuit-performance requirements into inductor-construction details is tricky. Using standard products

Most engineers who want switching supplies don't need 98.2% efficiency or 100W/in³.

as a starting point accelerates the dialogue and minimizes the number of iterations required for satisfactory results. Besides, the standard product will often suffice.

Strictly speaking, it makes more sense to design an inductor to meet circuit requirements than to fashion a circuit around a standard inductor. Deliberately ignoring this point complicated the author's work considerably, but will hopefully simplify the reader's. (**Ref 1** discusses inductor design theory.)

Start with a basic flyback supply

Fig 1 shows a basic flyback supply using the LT1070 switching-regulator IC (see **box,** "Switching supply improves duty-cycle control" for details of the LT1070.) The circuit converts a 5V input to a 12V output. **Fig 2** shows the voltage (trace A) and current (trace B) waveforms at the IC's V_{SW} pin.

The V_{SW} output is the collector of a common-emitter npn transistor and pulls current through the 100-μH inductor. The LT1070's internal oscillator sets the circuit's 40-kHz repetition rate. During the time V_{SW} is low, the current flow through the inductor induces a magnetic field around the inductor. The amount of energy stored in this field is a function of the current level, how long the current flows, and the windings of the inductor and its core material. Control of the duty cycle of the V_{SW}'s base drive forces a constant 12V output.

It's useful to think of the inductor as a bucket and the current flow as water pouring into it. The bucket's capacity—corresponding to the inductor's saturation limitations—sets the ultimate limit on energy storage.

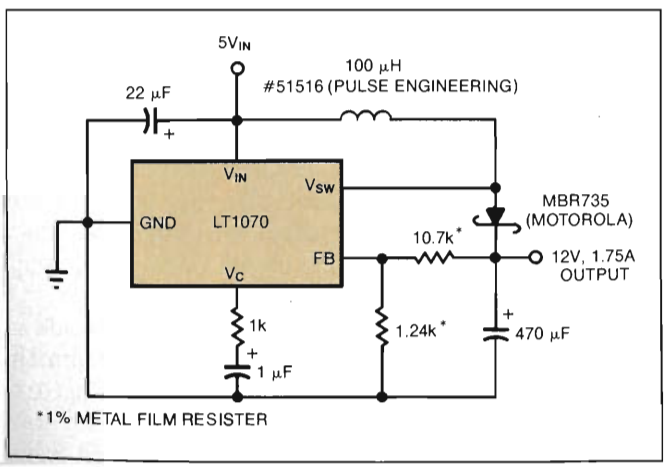


***Fig 1—This basic flyback supply converts** a 5V input to a 12V output.*

The applied voltage and the inductance of the wire limits the amount of energy that you can put into an inductor in a given time. The core characteristics limit the amount of energy that the inductor can store without saturating.

If the inductor is in a feedback loop, such as in **Fig 1,** then changing load demands will control the energy put into the inductor. **Fig 3** shows what happens when the

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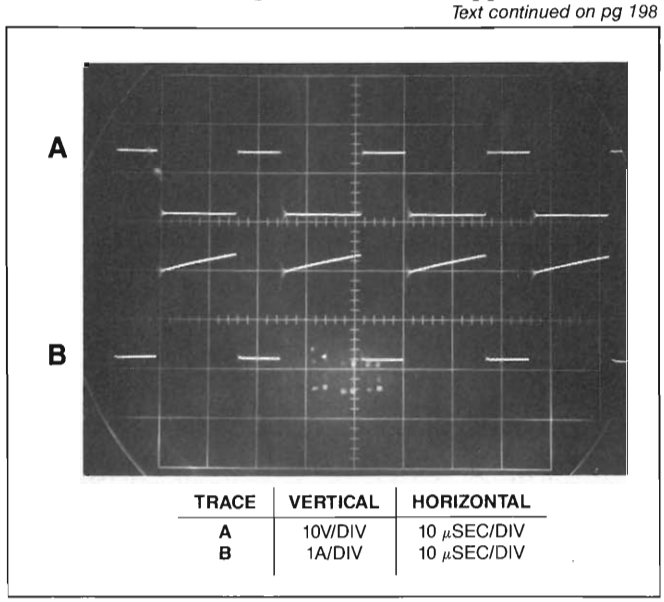
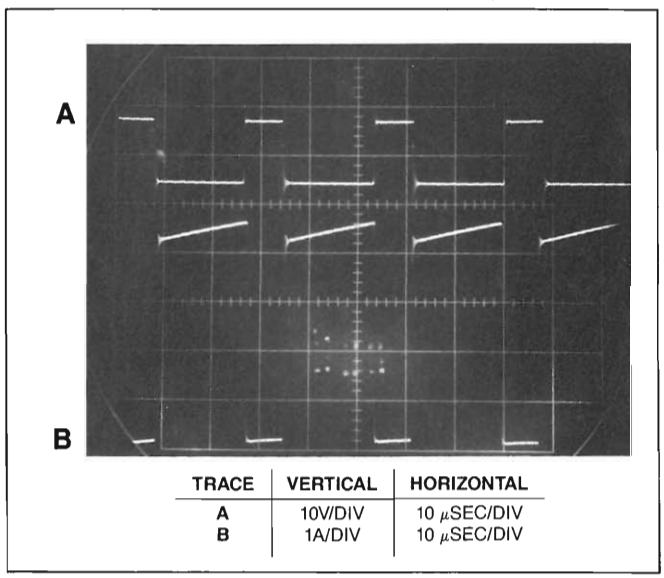


TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	10 μSEC/DIV
B	1A/DIV	10 μSEC/DIV

Fig 2—Trace A is the voltage,** and trace B is the current waveform at the V_{SW} pin of the IC in **Fig 1.



TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	10 μSEC/DIV
B	1A/DIV	10 μSEC/DIV

***Fig 3—This photo is the result of the same setup as Fig 2,** but shows what happens when the output demand doubles. In this case, the duty cycle doesn't change appreciably, but current doubles.*

Switching supply improves duty-cycle control

The LT1070 from Linear Technology (Milpitas, CA) is a current-mode switching supply, which means that the switch current, rather than the output voltage, directly controls the switch's duty cycle. The switch **(Fig A)** turns on at the start of each oscillator cycle, and turns off when the switch current reaches a predetermined level. A voltage-sensing error amplifier sets the current-trip level, which thereby controls the output voltage.

This technique has several advantages. First, it responds immediately to input-voltage variations, unlike ordinary switching power supplies, which have notoriously poor line-transient response. Second, it reduces the 90° phase shift at mid-frequencies in the energy-storage inductor. This lack of phase shift greatly simplifies closed-loop frequency compensation under widely varying input-voltage or output-load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output-overload or short-circuit conditions.

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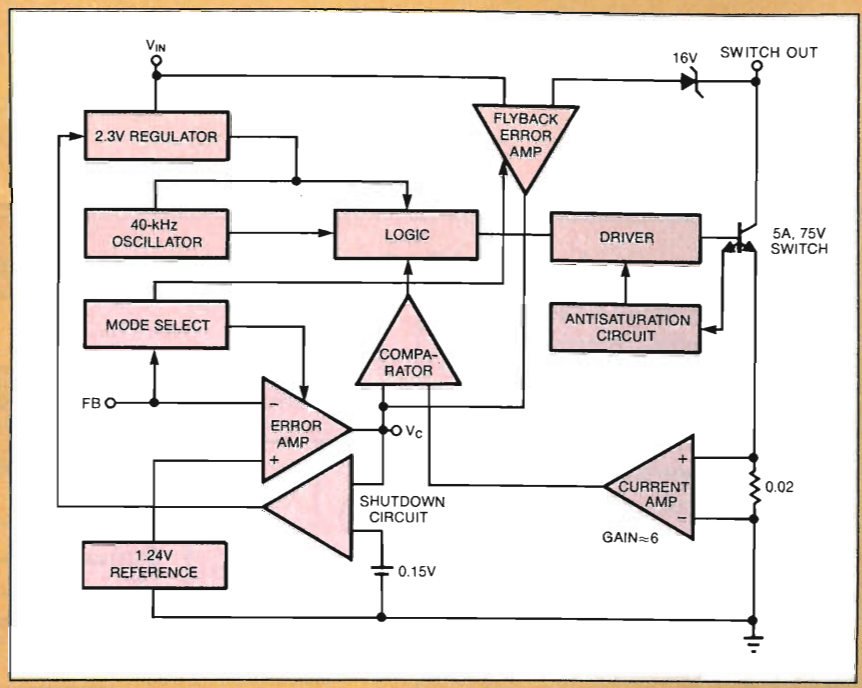

Fig A—The LT1070 is a current-mode, *switching-regulator IC in which the switch current directly controls the switch's duty cycle.*

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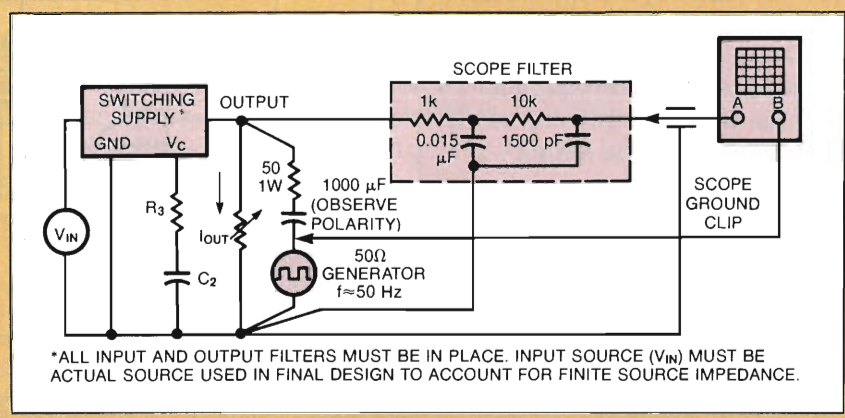

Fig A—You can use this setup *to couple a load variation into the output of a switching supply and to observe the waveform of the supply's response to the load variation. Typically you set the amplitude of the generator's output to 5V p-p to generate a 100-mA p-p load variation.*

You can inject a transient signal into a switching supply in many ways, but the preferred method is to ac-couple a load variation into the supply's output. This technique avoids the injection-point loading problems that arise if you try to inject a transient into some internal node of the supply, and it is applicable to all switching topologies. The only change necessary may be an amplitude adjustment to maintain small-signal conditions.

Fig A shows a setup using this technique and a function generator with a 50Ω output impedance, coupled through a 50Ω/1000-pF series RC network to the supply's output. The generator frequency is noncritical, but a good starting point is 50 Hz. Lower frequencies can cause an annoying, blinking scope display, and higher frequencies may not allow sufficient settling time for the output transient. Typically you set the amplitude of the generator's output to 5V p-p to generate a 100-mA p-p load variation.

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Once you've made the proper setup, finding the optimal value for the frequency-compensation network is fairly straightforward. Initially, you make C_2

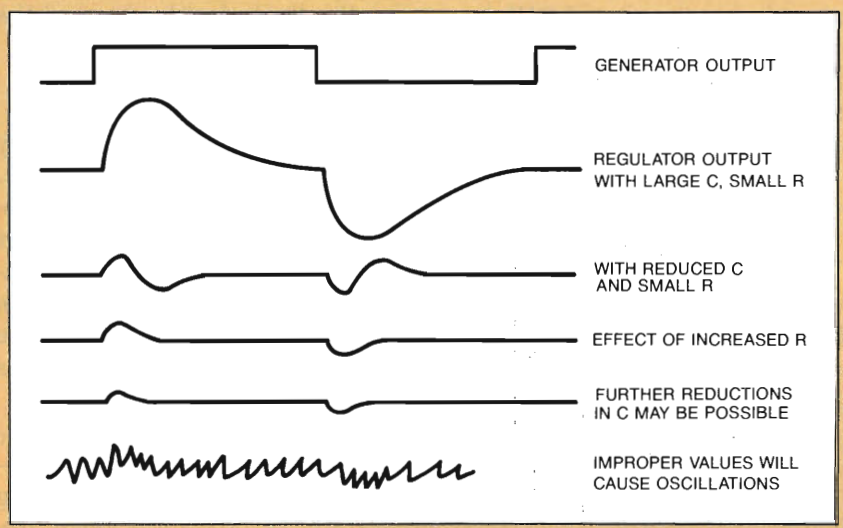

Fig B—Using the setup in Fig A, *you should be able to optimize the compensation-network component values in accordance with the wave shapes shown here.*

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Next, if the supply's output waveform is overdamped (see the waveforms in **Fig B**), you reduce the value of C_2 in steps of about 2:1 until the response becomes slightly underdamped. Next, you increase R_3 in steps of 2:1 to introduce a loop zero. This zero will normally improve damping and allow you to reduce the value of C_2 further. Shifting back and forth between R_3 and C_2 variations will allow you to quickly find the optimal values for these components.

If the supply's response is underdamped with the initial large value of C_2, you should increase R_3 immediately and try larger values for C_2. Increasing R_3 will normally bring about the overdamped starting condition for further iterations.

Just what do "optimal values" for R_3 and C_2 really mean? Normally they mean the smallest value for C_2 and the largest value for R_3 that will still guarantee no loop oscillations and that will result in loop settling that is as rapid as possible. The reason behind this criterion is that it minimizes the variations in output voltage due to input-ripple voltages and output-load transients.

A switching supply that is grossly overdamped will never oscillate, but it may have unacceptably large output transients following sudden changes in input voltage or output loading. It can also suffer from excessive overshoot problems during start-up or short-circuit recovery.

To guarantee acceptable loop stability under all conditions, you should check the final values chosen for R_3 and C_2 for all combinations of input voltage and load current. The simplest way to accomplish this goal is to apply minimum and maximum load currents—and several intermediate load currents. At each load-current level, vary the input voltage from minimum to maximum while observing the settling waveform.

These additional "worst-case" experiments are definitely necessary. Switching supplies, unlike linear supplies, have large shifts in loop gain and phase with changes in operating conditions. If you expect large temperature variations for the supply, you should also make stability checks at the temperature extremes. Significant temperature variations in any of several key component parameters can affect stability—in particular, input and output capacitor values, their ESRs, and inductor permeability.

The LT1070's parametric variations also require some consideration. The error amplifier g_M affects loop stability as does the transfer function of the V_C pin voltage vs switch current (listed as transconductance in the device's data sheet). For modest temperature variations, conservative overdamping under worst-case temperature conditions is usually sufficient to guarantee adequate stability at all temperatures. Note that, if you include external amplifiers or other active devices in the feedback loop, you must include their effects when stabilizing the loop.

The circuits employ a switching-regulator IC and only standard, off-the-shelf magnetics.

output demand doubles. In this case, the duty cycle doesn't change much, but current doubles.

This current doubling requires the inductor to store more energy. If it can't meet the storage requirement —that is, if it saturates and cannot hold any more magnetic flux—then it will cease to be inductive. At this point, the resistance of the wire is all that limits current flow. The current then rapidly builds to excessive and destructive values.

At the end of each inductor current-charge cycle, current flow in the inductor ceases, and the magnetic field around it abruptly collapses. The V_{SW} pin rises rapidly to a voltage higher than the 5V input. This "flyback" action gives the regulator both its voltage-boost characteristics and its name.

In this circuit, the flyback pulse's voltage clamps to a level just above the output voltage, because the flyback pulse gets steered through the Schottky diode to the output. The 470-μF capacitor integrates the repetitive flyback pulses, providing the circuit's dc output.

The feedback pin (FB) samples this output via the 10.7-kΩ/1.24-kΩ divider. The LT1070 compares the feedback-pin voltage to its internal 1.24V reference and controls the V_{SW} pin's duty cycle, closing the feedback loop. Because the LT1070 is trying to force its feedback pin to 1.24V, by varying the divider's values you set the circuit's output voltage.

Stability compensation is necessary

All feedback loops require some form of stability compensation (**Ref 2**), and the LT1070 is no exception. Its voltage-gain characteristic, combined with the substantial phase shift of the switching circuit, guarantees unwanted oscillation unless you provide for compensation. The large output capacitor smoothes the output to dc, but it also creates more phase shift. To complicate matters, the load, which can vary, further influences the phase characteristics.

In **Fig 1,** the 1-kΩ/1-μF combination at the V_C compensation pin provides roll-off of the circuit's response, furnishing stable compensation for all operating conditions. (See **box,** "Iterative procedure yields frequency compensation" for details and suggestions for achieving stability in switching-regulator loops.)

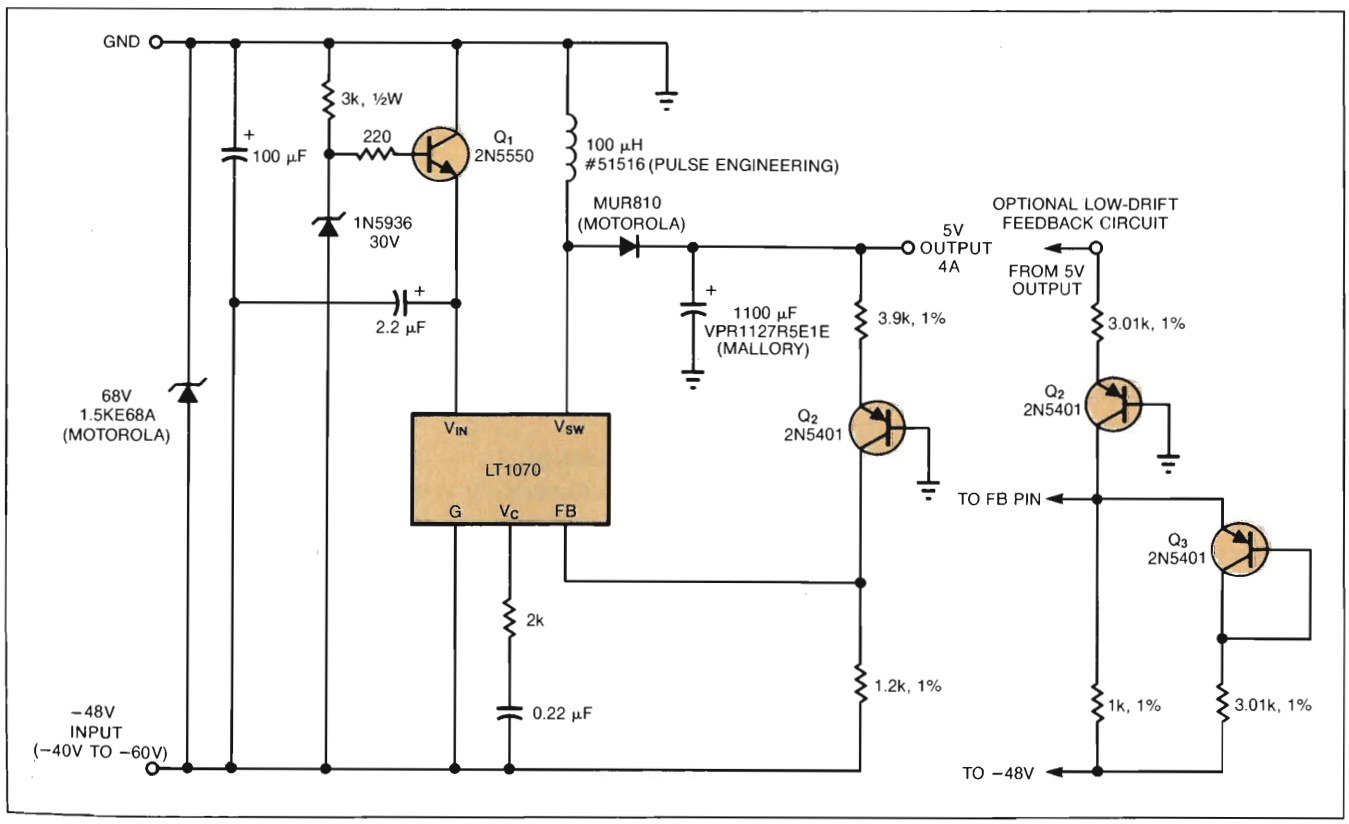


Fig 4—This circuit is similar to Fig 1's *but suits telecommunications applications. It works with raw telecommunications-supply levels, which are nominally −48V but can vary from −40 to −60V.*

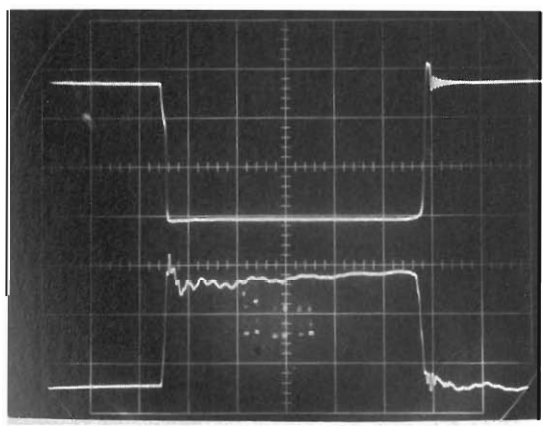
The majority of the problems you'll encounter with switching supplies involves their inductive components.

As innocent as **Fig 1** appears, odd and seemingly inexplicable problems will arise. Note that the ground connection appears at the ground pin, as opposed to its normal location at the bottom of the diagram. This unconventional location is deliberate because you must make the supply- and load-return connections at the GND pin. You musn't allow the high-speed, high-current returns from the output transistor's emitter (the "other end" of the V_{SW} pin) to mix with the small currents of the output divider or the V_C pin. Such mixing can promote poor regulation, unstable operation, or outright oscillation.

The 22-μF bypass capacitor ensures clean local power for the LT1070, even during the fast, high-current drain periods when V_{SW} turns on. The bypass capacitor should have good high-frequency characteristics (a tantalum or aluminum type, for example, paralleled by a disc-ceramic type).

Flyback supply for telecommunications

Fig 4's circuit is operationally similar to **Fig 1**'s, but is suitable for telecommunications applications. A raw telecommunications supply is nominally −48V, but can vary from −40 to −60V. Although the chip's V_{SW} pin can handle this voltage range, the V_{IN} pin requires protection (V_{MAX}=60V). Q_1 and the 30V zener diode serve this purpose, dropping the input voltage to about −17V at the V_{IN} pin under all line conditions.



TRACE	VERTICAL	HORIZONTAL
A	20V/DIV	500 nSEC/DIV
B	2A/DIV	500 nSEC/DIV

Fig 5—Trace A is the voltage, *and trace B is the current at the V_{SW} pin of the circuit in* ***Fig 4.*** *The ripples in the current trace are due to a nonoptimal breadboard layout. Inductor ringing during turn-off (trace A) is characteristic of flyback configurations.*

Here, the "top" of the inductor is at ground, and the ground pin is at −48V. The feedback pin senses with respect to the ground pin, so the circuit needs a level shift from the 5V output. Q_2 accomplishes this function and introduces only −2-mV/°C drift. This drift is normally not objectionable in a logic power supply, but you can compensate for it with an appropriately scaled diode-resistor combination across the 1.2-kΩ resistor.

Frequency compensation is similar to that of **Fig 1.** Note that a low ESR (equivalent series resistance) capacitor provides less phase shift, permitting faster loop response because of a reduced compensation time constant. The 68V zener diode clamps and absorbs excessive line transients that might otherwise damage the LT1070 (V_{SW} is 75V max).

Fig 5 shows operation waveforms for **Fig 4**'s V_{SW} pin. Trace A is the voltage, and trace B is the current. Switching characteristics are fast and clean. The ripples in the current trace are due to nonoptimal breadboard layout (ground as I say, not as I do). Inductor ringing during turn-off (trace A) is characteristic of flyback configurations. **EDN**

References

1. *AN-19, LT1070 Design Manual,* Linear Technology Corp, Milpitas, CA, June 1986.
2. *AN-18, The Oscillation Problem—Frequency Compensation Without Tears,* Linear Technology Corp, Milpitas, CA, March 1986.

Author's biography

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor Corp, Arthur D Little Inc, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art, and collecting antique scientific instruments.

Article Interest Quotient (Circle One)
High 479 Medium 480 Low 481

Designer's Guide to
Switching Power Supplies
Part 1

Regulator IC speeds design of switching power supplies

In part 1 of this 2-part series, you'll learn about simple switching regulators and a technique for stabilizing switching-supply feedback loops. Part 2, scheduled for the November 26th issue, will pick up where this article leaves off and delve into more complex, isolated switching power supplies.

Jim Williams, *Linear Technology Corp*

Switching power supplies are among the most difficult circuits to design. Mysterious operational modes; sudden, seemingly inexplicable failures; peculiar regulation characteristics; and just plain explosions are common occurrences. Diodes conduct the wrong way. Things get hot that shouldn't. Capacitors act like resistors, fuses don't blow, and transistors do. The output is at ground, and the ground terminal shows volts of noise.

In addition, there's the regulator's feedback loop, sampled in nature and replete with uncertain phase shifts. And of course everything varies with line and load conditions. A glance through conference proceedings and available literature yields either an undigestible store of mathematics or absurdly coy and simple little block diagrams that make everything look *so* easy.

Most engineers who need switching supplies don't require 98.2% efficiency or 100W/in^3. They aren't trying to get tenure, and they don't care about inventing a new type of circuit. What they do want are concepts directly applicable to the construction of working circuits that use readily available parts.

Standard parts ease startup

The circuits in this article employ standard, off-the-shelf magnetics exclusively, because most of the problems with switching power supplies center on the inductive components. The standard-magnetics approach almost certainly precludes precisely optimized performance and may horrify some veteran switching-supply designers, but it also eliminates inductor-construction uncertainties, saves time, and greatly increases your chances of getting a design running. A functional circuit is much easier to work with—and get enthusiastic about—than the smoking carcass of a decimated breadboard. Although the characteristics of standard inductors aren't optimal, it's easier to evaluate the performance of a working circuit on an oscilloscope than to guess why you don't see anything at all.

Also, once your circuit is running, you can obtain an optimized version of the standard product from the inductor manufacturer. Generally, the manufacturer can more easily modify its standard product than start from scratch. The process of communicating and translating circuit-performance requirements into inductor-construction details is tricky. Using standard products

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as a starting point accelerates the dialogue and minimizes the number of iterations required for satisfactory results. Besides, the standard product will often suffice.

Strictly speaking, it makes more sense to design an inductor to meet circuit requirements than to fashion a circuit around a standard inductor. Deliberately ignoring this point complicated the author's work considerably, but will hopefully simplify the reader's. (**Ref 1** discusses inductor design theory.)

Start with a basic flyback supply

Fig 1 shows a basic flyback supply using the LT1070 switching-regulator IC (see **box,** "Switching supply improves duty-cycle control" for details of the LT1070.) The circuit converts a 5V input to a 12V output. **Fig 2** shows the voltage (trace A) and current (trace B) waveforms at the IC's V_{SW} pin.

The V_{SW} output is the collector of a common-emitter npn transistor and pulls current through the 100-μH inductor. The LT1070's internal oscillator sets the circuit's 40-kHz repetition rate. During the time V_{SW} is low, the current flow through the inductor induces a magnetic field around the inductor. The amount of energy stored in this field is a function of the current level, how long the current flows, and the windings of the inductor and its core material. Control of the duty cycle of the V_{SW}'s base drive forces a constant 12V output.

It's useful to think of the inductor as a bucket and the current flow as water pouring into it. The bucket's capacity—corresponding to the inductor's saturation limitations—sets the ultimate limit on energy storage.

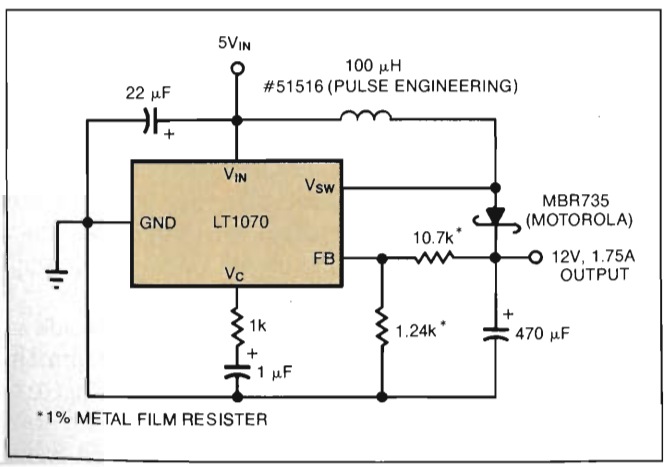

***Fig 1—This basic flyback supply converts** a 5V input to a 12V output.*

The applied voltage and the inductance of the wire limits the amount of energy that you can put into an inductor in a given time. The core characteristics limit the amount of energy that the inductor can store without saturating.

If the inductor is in a feedback loop, such as in **Fig 1,** then changing load demands will control the energy put into the inductor. **Fig 3** shows what happens when the

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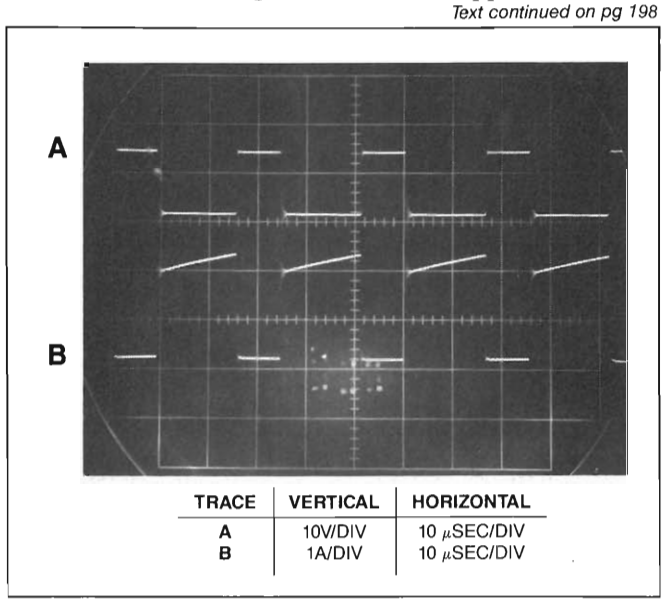

TRACE	VERTICAL	HORIZONTAL
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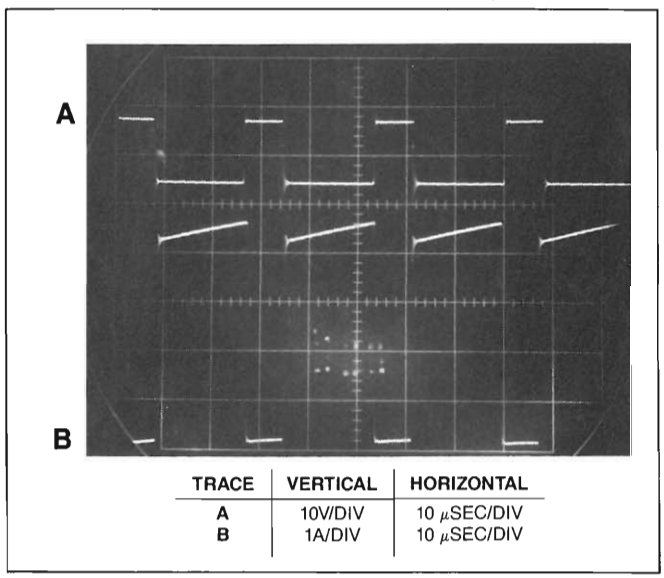
B	1A/DIV	10 μSEC/DIV

Fig 2—Trace A is the voltage,** and trace B is the current waveform at the V_{SW} pin of the IC in **Fig 1.



TRACE	VERTICAL	HORIZONTAL
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***Fig 3—This photo is the result of the same setup as Fig 2,** but shows what happens when the output demand doubles. In this case, the duty cycle doesn't change appreciably, but current doubles.*

Switching supply improves duty-cycle control

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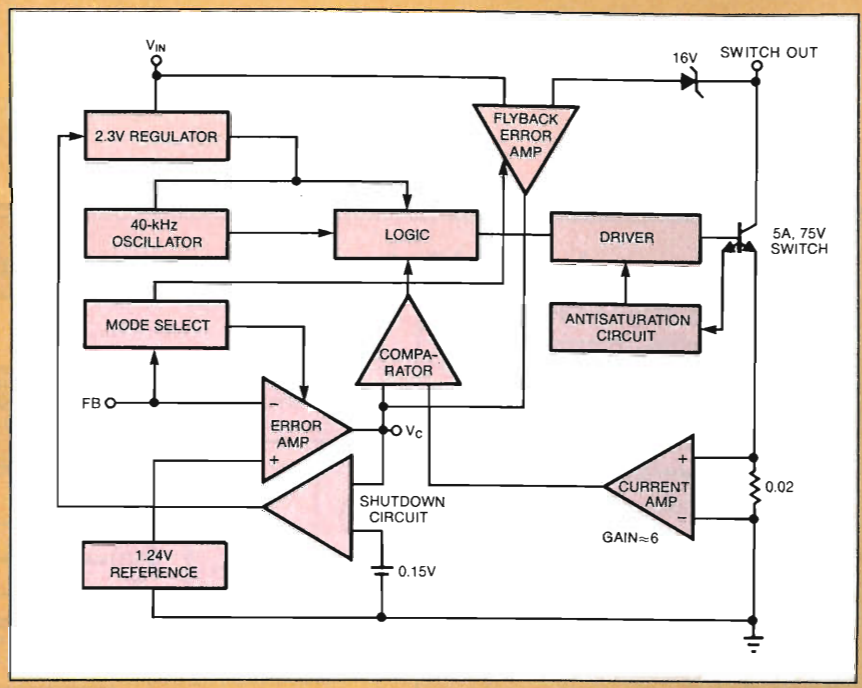

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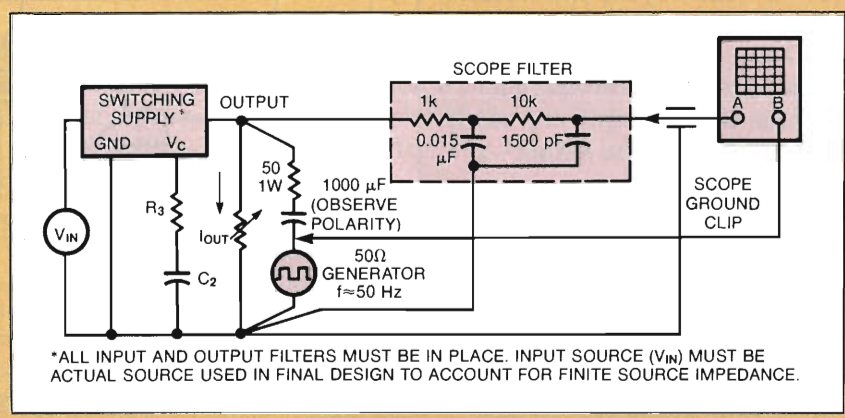

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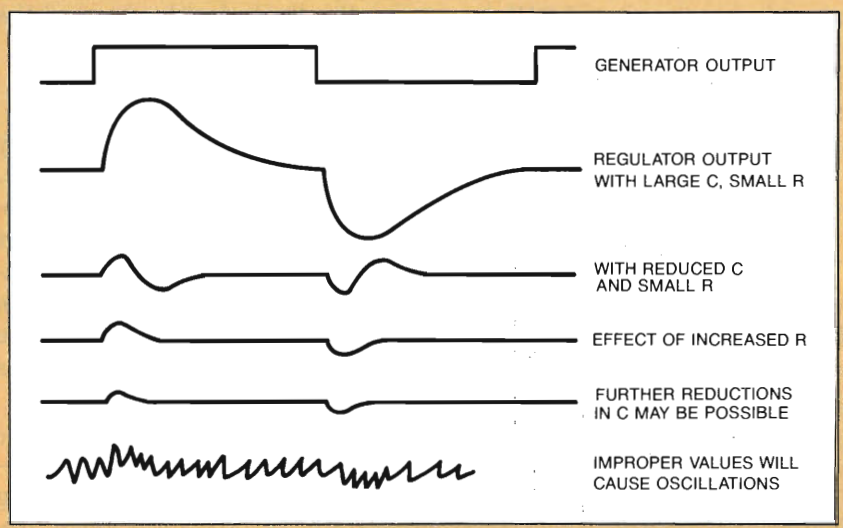

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large (≥2 μF), and R_3 small (~1 kΩ). This compensation nearly always ensures that the supply will be stable enough to begin working.

Next, if the supply's output waveform is overdamped (see the waveforms in **Fig B**), you reduce the value of C_2 in steps of about 2:1 until the response becomes slightly underdamped. Next, you increase R_3 in steps of 2:1 to introduce a loop zero. This zero will normally improve damping and allow you to reduce the value of C_2 further. Shifting back and forth between R_3 and C_2 variations will allow you to quickly find the optimal values for these components.

If the supply's response is underdamped with the initial large value of C_2, you should increase R_3 immediately and try larger values for C_2. Increasing R_3 will normally bring about the overdamped starting condition for further iterations.

Just what do "optimal values" for R_3 and C_2 really mean? Normally they mean the smallest value for C_2 and the largest value for R_3 that will still guarantee no loop oscillations and that will result in loop settling that is as rapid as possible. The reason behind this criterion is that it minimizes the variations in output voltage due to input-ripple voltages and output-load transients.

A switching supply that is grossly overdamped will never oscillate, but it may have unacceptably large output transients following sudden changes in input voltage or output loading. It can also suffer from excessive overshoot problems during start-up or short-circuit recovery.

To guarantee acceptable loop stability under all conditions, you should check the final values chosen for R_3 and C_2 for all combinations of input voltage and load current. The simplest way to accomplish this goal is to apply minimum and maximum load currents—and several intermediate load currents. At each load-current level, vary the input voltage from minimum to maximum while observing the settling waveform.

These additional "worst-case" experiments are definitely necessary. Switching supplies, unlike linear supplies, have large shifts in loop gain and phase with changes in operating conditions. If you expect large temperature variations for the supply, you should also make stability checks at the temperature extremes. Significant temperature variations in any of several key component parameters can affect stability—in particular, input and output capacitor values, their ESRs, and inductor permeability.

The LT1070's parametric variations also require some consideration. The error amplifier g_M affects loop stability as does the transfer function of the V_C pin voltage vs switch current (listed as transconductance in the device's data sheet). For modest temperature variations, conservative overdamping under worst-case temperature conditions is usually sufficient to guarantee adequate stability at all temperatures. Note that, if you include external amplifiers or other active devices in the feedback loop, you must include their effects when stabilizing the loop.

The circuits employ a switching-regulator IC and only standard, off-the-shelf magnetics.

output demand doubles. In this case, the duty cycle doesn't change much, but current doubles.

This current doubling requires the inductor to store more energy. If it can't meet the storage requirement —that is, if it saturates and cannot hold any more magnetic flux—then it will cease to be inductive. At this point, the resistance of the wire is all that limits current flow. The current then rapidly builds to excessive and destructive values.

At the end of each inductor current-charge cycle, current flow in the inductor ceases, and the magnetic field around it abruptly collapses. The V_{SW} pin rises rapidly to a voltage higher than the 5V input. This "flyback" action gives the regulator both its voltage-boost characteristics and its name.

In this circuit, the flyback pulse's voltage clamps to a level just above the output voltage, because the flyback pulse gets steered through the Schottky diode to the output. The 470-μF capacitor integrates the repetitive flyback pulses, providing the circuit's dc output.

The feedback pin (FB) samples this output via the 10.7-kΩ/1.24-kΩ divider. The LT1070 compares the feedback-pin voltage to its internal 1.24V reference and controls the V_{SW} pin's duty cycle, closing the feedback loop. Because the LT1070 is trying to force its feedback pin to 1.24V, by varying the divider's values you set the circuit's output voltage.

Stability compensation is necessary

All feedback loops require some form of stability compensation (**Ref 2**), and the LT1070 is no exception. Its voltage-gain characteristic, combined with the substantial phase shift of the switching circuit, guarantees unwanted oscillation unless you provide for compensation. The large output capacitor smoothes the output to dc, but it also creates more phase shift. To complicate matters, the load, which can vary, further influences the phase characteristics.

In **Fig 1,** the 1-kΩ/1-μF combination at the V_C compensation pin provides roll-off of the circuit's response, furnishing stable compensation for all operating conditions. (See **box,** "Iterative procedure yields frequency compensation" for details and suggestions for achieving stability in switching-regulator loops.)

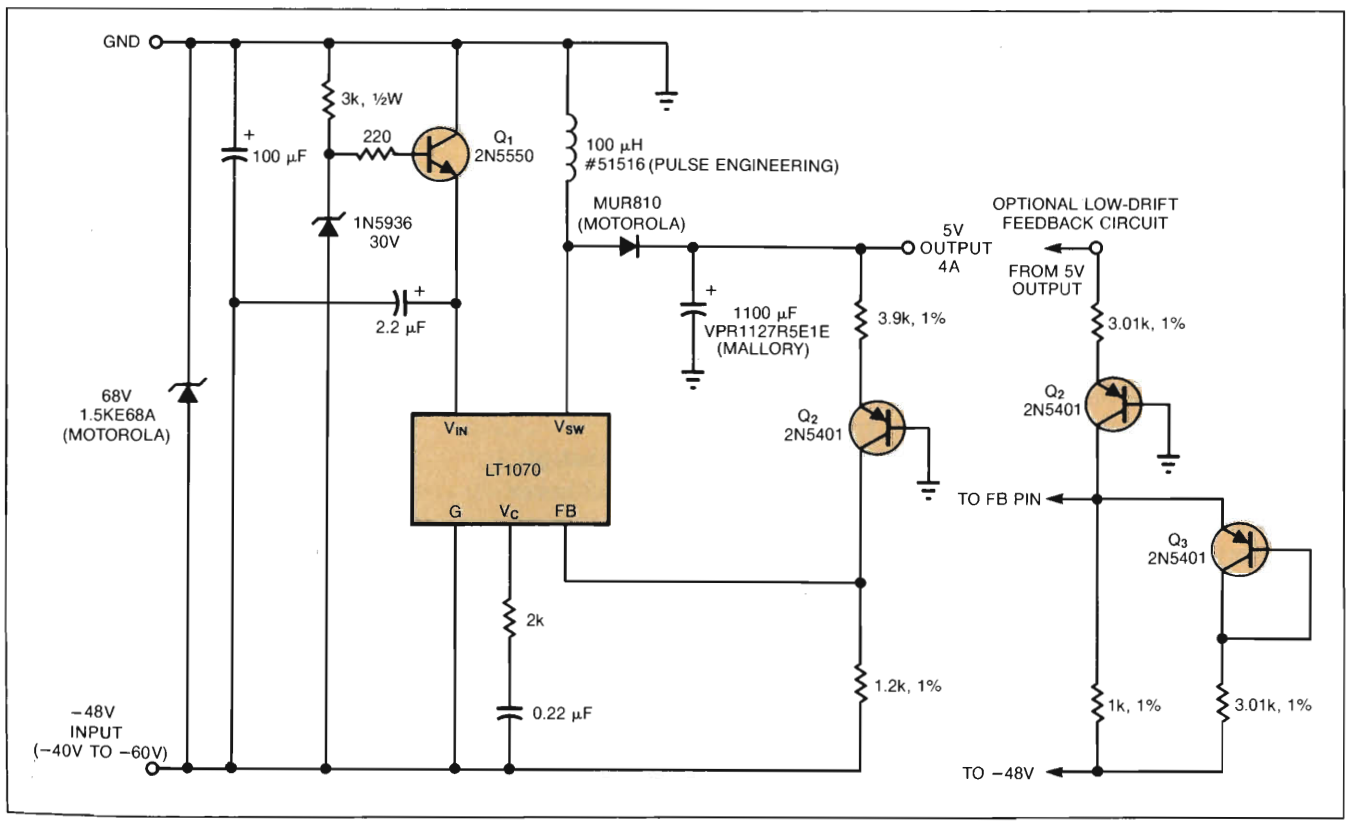


Fig 4—This circuit is similar to Fig 1's *but suits telecommunications applications. It works with raw telecommunications-supply levels, which are nominally −48V but can vary from −40 to −60V.*

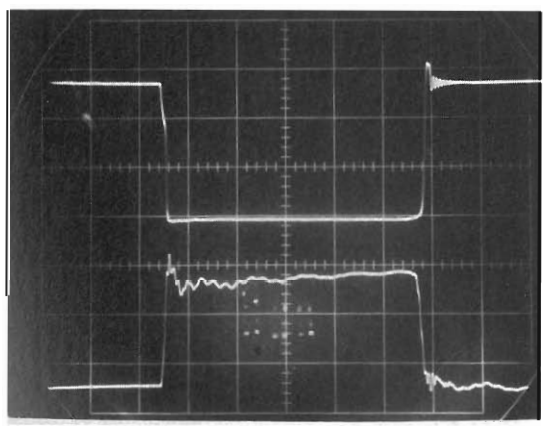
The majority of the problems you'll encounter with switching supplies involves their inductive components.

As innocent as **Fig 1** appears, odd and seemingly inexplicable problems will arise. Note that the ground connection appears at the ground pin, as opposed to its normal location at the bottom of the diagram. This unconventional location is deliberate because you must make the supply- and load-return connections at the GND pin. You musn't allow the high-speed, high-current returns from the output transistor's emitter (the "other end" of the V_{SW} pin) to mix with the small currents of the output divider or the V_C pin. Such mixing can promote poor regulation, unstable operation, or outright oscillation.

The 22-μF bypass capacitor ensures clean local power for the LT1070, even during the fast, high-current drain periods when V_{SW} turns on. The bypass capacitor should have good high-frequency characteristics (a tantalum or aluminum type, for example, paralleled by a disc-ceramic type).

Flyback supply for telecommunications

Fig 4's circuit is operationally similar to **Fig 1**'s, but is suitable for telecommunications applications. A raw telecommunications supply is nominally −48V, but can vary from −40 to −60V. Although the chip's V_{SW} pin can handle this voltage range, the V_{IN} pin requires protection (V_{MAX}=60V). Q_1 and the 30V zener diode serve this purpose, dropping the input voltage to about −17V at the V_{IN} pin under all line conditions.



TRACE	VERTICAL	HORIZONTAL
A	20V/DIV	500 nSEC/DIV
B	2A/DIV	500 nSEC/DIV

Fig 5—Trace A is the voltage, *and trace B is the current at the V_{SW} pin of the circuit in* ***Fig 4.*** *The ripples in the current trace are due to a nonoptimal breadboard layout. Inductor ringing during turn-off (trace A) is characteristic of flyback configurations.*

Here, the "top" of the inductor is at ground, and the ground pin is at −48V. The feedback pin senses with respect to the ground pin, so the circuit needs a level shift from the 5V output. Q_2 accomplishes this function and introduces only −2-mV/°C drift. This drift is normally not objectionable in a logic power supply, but you can compensate for it with an appropriately scaled diode-resistor combination across the 1.2-kΩ resistor.

Frequency compensation is similar to that of **Fig 1.** Note that a low ESR (equivalent series resistance) capacitor provides less phase shift, permitting faster loop response because of a reduced compensation time constant. The 68V zener diode clamps and absorbs excessive line transients that might otherwise damage the LT1070 (V_{SW} is 75V max).

Fig 5 shows operation waveforms for **Fig 4**'s V_{SW} pin. Trace A is the voltage, and trace B is the current. Switching characteristics are fast and clean. The ripples in the current trace are due to nonoptimal breadboard layout (ground as I say, not as I do). Inductor ringing during turn-off (trace A) is characteristic of flyback configurations. **EDN**

References

1. *AN-19, LT1070 Design Manual,* Linear Technology Corp, Milpitas, CA, June 1986.
2. *AN-18, The Oscillation Problem—Frequency Compensation Without Tears,* Linear Technology Corp, Milpitas, CA, March 1986.

Author's biography

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor Corp, Arthur D Little Inc, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art, and collecting antique scientific instruments.

Article Interest Quotient (Circle One)
High 479 Medium 480 Low 481

Designer's Guide to
Switching Power Supplies
Part 2

Galvanically isolated switching supplies provide high power

Part 1 of this 2-part series dealt with simple switching power supplies and described a "cut and try" approach for stabilizing a supply's feedback loop. The conclusion offers advice on designing more complicated switching supplies, ones with isolated outputs.

Jim Williams, *Linear Technology Corp*

The fundamental difference between the switching supply in **Fig 1** and the circuits presented in Part 1 **(Ref 1)** is that **Fig 1**'s output is galvanically isolated from its input—often a requirement for telecommunications equipment. Such isolation necessitates a transformer rather than a simple 2-terminal inductor, and also requires that feedback passes to the regulator across a nonconducting path. The requirement for a transformer complicates the circuit's start-up and switching characteristics, and the need for isolated feedback complicates frequency compensation.

In this circuit, the V_{IN} pin receives power from a transformer winding. Obviously, the winding can't supply power at start-up because the circuit isn't functioning. Q_1-Q_4 solves this power-up problem. When you apply power to the supply, Q_5 can't conduct because the LT1071 doesn't have any power going to it. Q_1, Q_2 (which functions as a zener diode in this circuit), and Q_3 are off. Under these conditions, Q_4 is on, pulling the V_C pin down and strobing off the LT1071. (The circuits in this article use the lower-current, lower-cost LT1071, rather than the LT1070 used in Part 1.)

The potential at Q_1's emitter slowly rises as the 10-kΩ/100-μF combination charges. When Q_1's emitter rises high enough, Q_1 turns on. Zener-connected Q_2 conducts when the voltage across it is about 7V, biasing Q_3 on. Q_1 then sees regenerative feedback, which turns on Q_3 harder. As Q_3 turns on, it cuts off Q_4, allowing the V_C pin to rise and turning on the LT1071.

Soft-start characteristic helps

The 10-μF/diode combination limits the rate of rise at the V_C pin and forces the V_C pin to come up slowly, providing a soft-start characteristic. This delay prevents start-up at starved or unstable V_{IN} voltages, which could cause erratic or destructive modes of operation. The 100Ω/diode string discharges the 10-μF capacitor on removal of circuit input power.

When start-up does occur, the transformer feeds the V_{IN} pin with dc via the 50Ω resistor and the MUR120 rectifier diode. The 50Ω resistor combines with the 100-μF capacitor to provide good ripple and transient filtering. This voltage is ample to run the LT1071 and reduces the current through the 10-kΩ resistor, saving power. Q_1, Q_2, and Q_3 remain on, biasing Q_4 to permit operation of the LT1071.

With transformers, unlike inductors, all of the flyback energy doesn't end up in the output capacitor.

In the flyback circuits described in the first part of this article, the V_{SW} pin drove the inductor directly. The output capacitor clamped the output voltage and dumped the flyback energy directly into the output capacitor; excessive voltages did not occur. In **Fig 1**, however, a transformer takes the place of the inductor, and its flyback characteristics are different from a simple 2-terminal inductor.

In the case of the transformer, all the flyback energy doesn't end up in the output capacitor. Substantial flyback-voltage spikes (>100V) appear across the transformer's primary.

Certain measures prevent these spikes from destroying the circuit. The 0.47-μF/2-kΩ/diode combination across the transformer's primary (a damper network) conducts during the flyback action, which loads the transformer's primary and minimizes flyback amplitude. You have to select the damper network's values empirically, and you have to weigh the damping effectiveness vs the power dissipation in the damper network. Very low resistance values markedly reduce flyback potential, but cause excessive dissipation. High damping-resistor values limit dissipation, but allow excessive flyback voltages. You should select the damp-

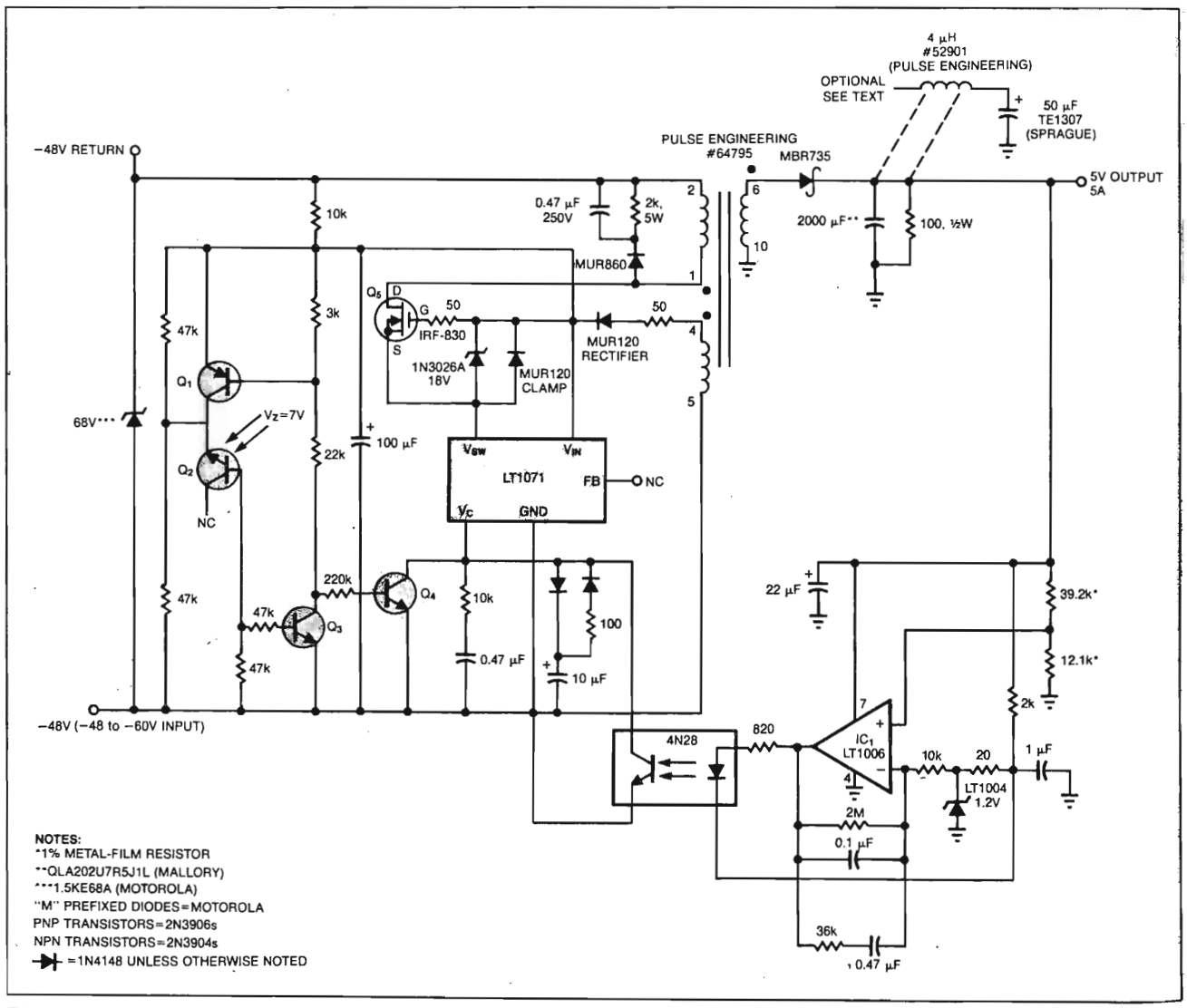


Fig 1—This telecommunications switching supply has its output *galvanically isolated from its input. This isolation necessitates a transformer, which complicates the circuit's start-up and switching characteristics.*

er values under fully loaded conditions because flyback energy is proportional to transformer power levels.

Even with the damper network, however, the flyback voltage is too high for the LT1071's output transistor. Q_5, in series with the LT1071's output transistor, prevents the LT1071 from seeing the high voltage. In this configuration, sometimes called a cascode, Q_5's high standoff rating blocks the high voltage and lets the LT1071 operate well within its breakdown limits.

Parasitics pass spikes

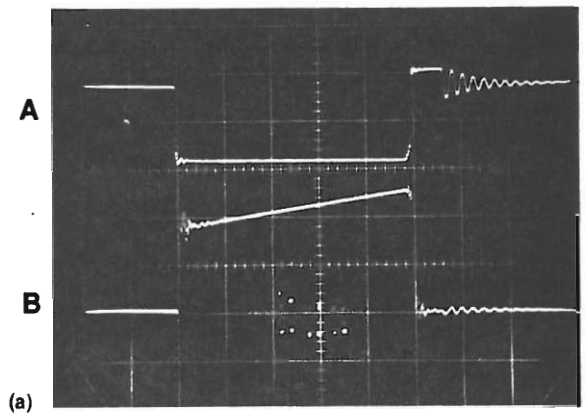
Q_5 confers mixed blessings, though. Large parasitic capacitances are associated with all its terminals and during switching, these capacitances can allow excessive transient voltages to appear in unexpected places. The 18V zener diode guarantees against gate-source breakdown (V_{GS} max=20V), and the MUR120 diode clamps the V_{SW} pin to the V_{IN} potential.

The transformer's secondary gets rectified and filtered to produce the 5V output. This output is galvanically isolated from the circuit's input. To preserve isolation, the feedback path must also be galvanically isolated. IC_1, the optoisolator (4N28), and associated components serve this purpose. IC_1, powered by the 5V output, compares a resistively sampled portion of the output with the LT1004 1.2V reference. Operating at a gain of 200, it drives the optoisolator's LED.

The optoisolator's output transistor, in turn, biases the LT1071's V_C pin, closing the regulation loop. The IC_1/optoisolator combination essentially bypasses the feedback amplifier inside the LT1071. Normally, the drift of the optoisolator's transmission characteristics over time and temperature would result in unstable feedback. Here, IC_1's gain comes ahead of the optoisolator, which attenuates the uncertainties and provides a stable loop. The ground return for the optoisolator goes through a zener diode having the same voltage as V_{REF} instead of directly to ground. This routing forces the op amp to bias well above ground, minimizing saturation effects during output transients.

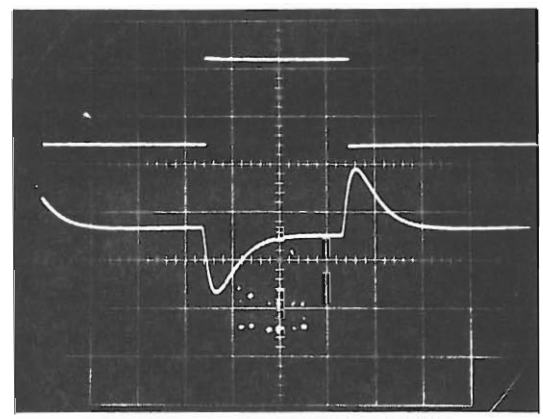
Compensation is more complex

As stated earlier, frequency compensation is somewhat involved. The 0.1-μF capacitor rolls off IC_1's gain. This roll-off keeps the gain low at high frequencies, preventing amplified ripple and noise from feeding back to the LT1071. The 36-kΩ/0.47-μF combination gives significant gain reduction under transient conditions. Local compensation at the LT1071's V_C pin stabilizes the loop. The 100Ω resistor at the 5V output, a deliberate path for sinking current, ensures loop stability for a light load or for no load. The 50Ω resistor at Q_5 combines with the gate's capacitance to slightly slow FET switching, reducing high-frequency harmonics.



(a)

TRACE	VERTICAL	HORIZONTAL
A	50V/DIV	2 μSEC/DIV
B	0.5A/DIV	2 μSEC/DIV



(b)

TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	5 mSEC/DIV (3-kHz BANDPASS FILTER)
B	100 mV/DIV (AC-COUPLED ON 5V OUTPUT)	5 mSEC/DIV (3-kHz BANDPASS FILTER)

***Fig 2—In a, trace A shows Fig 1's Q_5 drain voltage** and trace B shows the drain current. Trace A indicates that, due to flyback effects, the MOSFET sees about 100V. The ringing upon turn-off is normal. Trace B shows that the current is fast, clean, and controlled. In **b**, trace B is **Fig 1's** transient response for a 1A step added to a 2.5A output. When trace A goes high, the step occurs. Trace B indicates that output sag is corrected in about 8 msec.*

Circuit waveforms appear in **Fig 2.** Trace A in **Fig 2a** is Q_5's drain voltage, and trace B shows the drain current. Trace A shows that the MOSFET sees about 100V because of the flyback effects, but this voltage level is well within the transistor's rating. The ringing at turn-off is normal. Trace B shows that the current flow is fast, clean, and controlled. **Fig 2b** shows the transient response for a 1A step added to a 2.5A output. When trace A goes high, the step occurs. Trace B shows that output sag is corrected in about 8 msec.

You have to weigh the damping effectiveness vs the power dissipation in the damper network.

When trace A returns low, the 1A load is removed and recovery is similar to the positive step. The optional output filter (Pulse Engineering part #52901, San Diego, CA) in **Fig 1** will reduce broadband output noise to about 75 mV p-p.

One of the most desirable switching-supply circuits is also one of the most difficult to design. **Fig 3**'s circuit exhibits many similarities to **Fig 1**, but derives its power directly from the 115V ac line. Off-line operation is preferable because it eliminates large, heavy, and inefficient 60-Hz magnetic components and filter capacitors. This particular circuit provides an isolated 5V,

Choosing a diode can be surprisingly tough

"Simple" diodes furnish a good example of how carefully you must consider a switching supply's operating conditions while designing. Switching diodes have two important transient characteristics: reverse-recovery time and forward turn-on time.

Reverse-recovery time occurs because the diode stores charge during its forward-conducting cycle. This stored charge causes the diode to act as a low-impedance conductive element for a short period of time after reverse drive gets applied. You measure reverse-recovery time by forward-biasing the diode with a specified current, then forcing a second, specified current backwards through the diode. The time required for the diode to change from a reverse-conducting state to its normal reverse-nonconducting state is the reverse-recovery time.

Hard turn-off diodes switch abruptly from one state to the other following reverse-recovery time. They therefore dissipate very little power even with only moderately short reverse-recovery times. Soft turn-off diodes have a gradual turn-off characteristic that can cause considerable power dissipation in a diode during its turn-off interval.

Fig Aa shows typical current and voltage waveforms for three common diode types (fast, ultrafast, and Schottky) used in flyback converters and when V_{IN}=10V and V_{OUT}=20V, 2A. Long reverse-recovery times can cause significant extra heating in the diode or the power switch. The total power dissipation during the reverse-recovery time is

$$P_{tRR}=V\times f\times t_{RR}\times I_F,$$

where V=diode reverse voltage, f=switching frequency, t_{RR}=reverse-recovery time, and I_F=diode forward current just prior to turn-off.

For a boost-configuration switching supply where I_F=4A, V=20V, and f=40 kHz, for example, the diode's on current is twice the output current. A diode with t_{RR}=300 nsec creates a power loss of

$$P_{tRR}=20(40\times10^3)(300\times10^{-8})4=0.96W.$$

If this same diode has a forward voltage of 0.8V at 4A, its forward loss will be 1.6W. Reverse-recovery losses in this example are nearly as large as forward losses. You must realize, however, that reverse losses don't necessarily result in significant increases in diode dissipation. A hard turn-off diode will shift much of the power dissipation to the power switch, which will see high current and high voltage during the reverse-recovery time. This stress need not be harmful to a properly selected power switch, though the power loss remains.

The effects associated with diode turn-on time can potentially be more harmful than reverse turn-off effects. Consider that the output diode clamps the inductor's or transformer's output connection and prevents it from rising higher than the output voltage. A diode that turns on slowly can have a very high forward voltage impressed across it for the duration of the turn-on time.

The problem is that this increased voltage appears across the power switch. The graphs in **Fig Ab** show diode turn-on spikes for the three types. The actual height of the spike will depend on the rate of the current rise and the initial current value; nonetheless, the graphs emphasize the need for fast turn-on characteristics in applications that strain the limits of the switch-voltage ratings.

Fast diodes can prove useless if your circuit has excessive stray inductance in the diode, output capacitor, or regulator

20A output as well as isolated ±12V, 1A outputs. It operates over a 90 to 140V ac input range, includes ac line-surge suppression and soft-start capability, and promises loop stability under all conditions. Efficiency exceeds 75%.

Before describing this circuit's construction, it's vital that you're aware of the need for extreme caution during testing or use: AC line-connected, high-voltage potentials are present.

The diode-bridge/470-μF-capacitor combination rectifies and filters the ac-line power. The metal-oxide varistor (MOV) device provides surge suppression, and

loop. For instance, 20-gauge hook-up wire has 30 nH/in. of inductance. The current-fall rate of the LT1070 switching-regulator IC's (Linear Technology Corp, Milpitas, CA) power switch is 10^8A/sec. This rate generates a voltage of $(10^8)(30\times10^{-9})$=3V/in. in the stray wiring. Keep the diode, capacitor, and ground and switch lead lengths short.

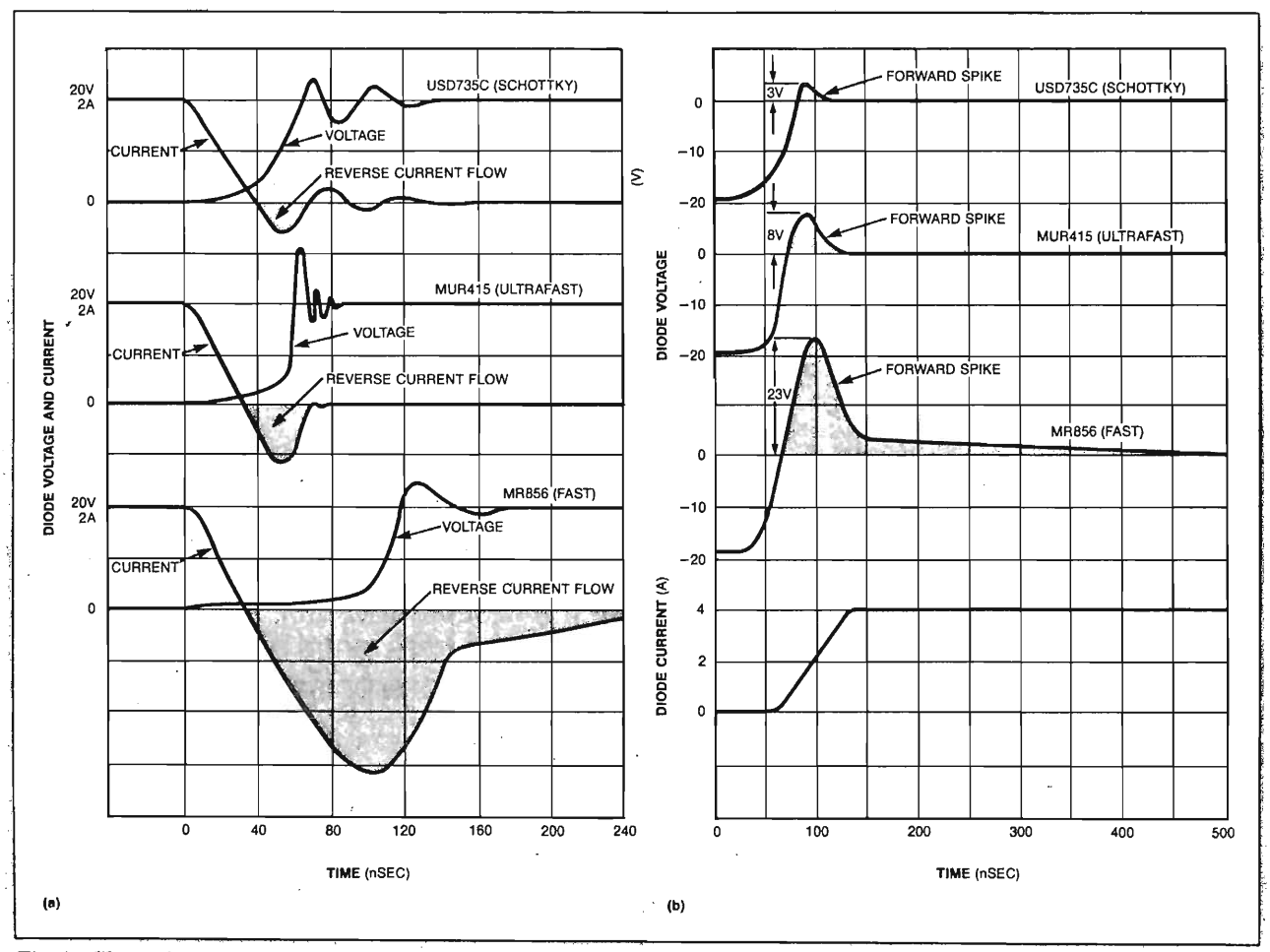


***Fig A—Shown here are typical current and voltage waveforms** for three common diode types (a) (V_{IN}=10V, V_{OUT}=20V, 2A). Long reverse-recovery times can cause significant additional heating in the diode or the power switch. The graphs of the diodes' turn-on spikes (b) emphasize the need for fast turn-on characteristics in applications that push the limits of switch-voltage ratings.*

Power-switching parasitics can allow excessive transient voltages to appear in unexpected places.

the thermistor limits turn-on in-rush current. Start-up and soft-start circuitry are similar to that of **Fig 1**'s, with some changes necessitated by the higher input voltage. The 220-kΩ/1.24-kΩ divider prevents erratic operation at extremely low ac-line voltages (70V ac); at such levels, the divider forces the LT1071's feedback pin to a low state, shutting down the circuit.

The high input voltage, typically 160V dc, means that the LT1071's internal current limit is set too high to protect the regulator if the circuit's output gets shorted. Q_6 and associated components provide about 2 amps of current limiting. The LT1071's ground-pin current doesn't go directly to ground; instead, it flows through the 0.3Ω resistor, turning on Q_6 if current is too high. The 22-kΩ/50-pF RC network filters noise, preventing erratic Q_6 operation.

Q_5, a power MOSFET, is in a cascode configuration with the LT1071 to withstand the necessary high-voltage switching. Q_5 has a 500V voltage-breakdown rating. The switch circuit is similar to that of the one in **Fig 1**. The 50Ω resistor in the gate circuit combines with the gate capacitance to slow Q_5's transitions slightly, thus reducing high-frequency harmonics. Reducing the harmonics eases layout considerations. The transformer's damper network is borrowed from **Fig 1**; only the component values are refigured.

The IC_1/optoisolator feedback loop preserves the transformer's galvanic isolation and is also similar to

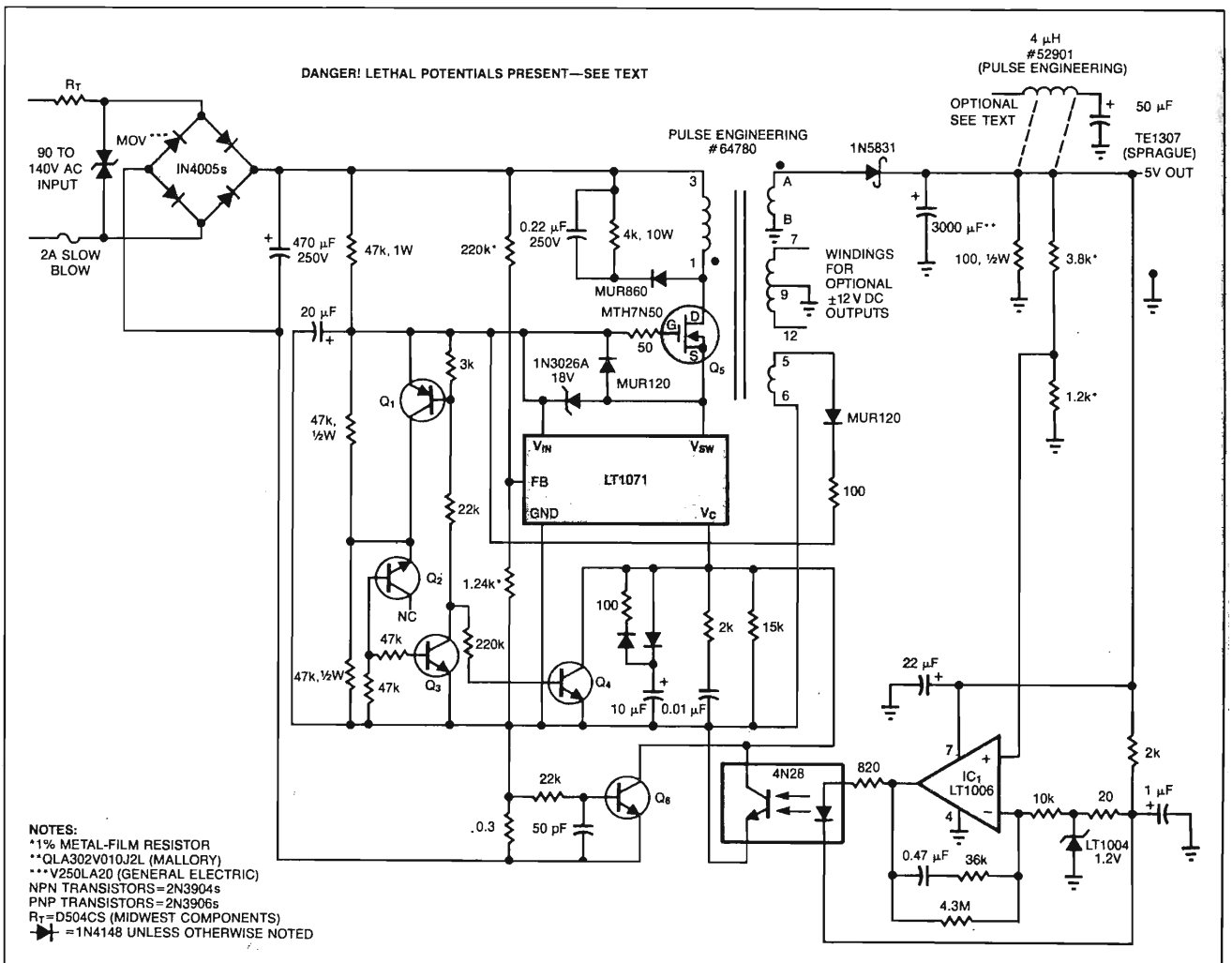


***Fig 3—This switching supply operates directly from the** 115V ac line. Off-line operation is desirable because it obviates the need for large, inefficient 60-Hz magnetic components and filter capacitors.*

Off-line operation is desirable because it eliminates large, heavy, and inefficient 60-Hz magnetic components and filter capacitors.

that of the one in **Fig 1.** Compensation values for IC_1 and the LT1071 are different, reflecting this circuit's different gain-phase characteristics.

Checklist will help

In conclusion, no matter whether you need to design a simple switching supply like those delineated in Part 1 or an isolated one like the supplies described here, your design will proceed more smoothly if you remember the following advice.

- Always consider inductive flyback effects. Are semiconductor-breakdown ratings adequate to withstand them? Will you need a snubber (damper) network? Consider all possible voltages and current paths, including the transient ones via semiconductor-junction capacitances.
- Account for all of the capacitors' operating conditions. Voltage ratings are the most obvious consideration, but remember to plan for the effects of ESR and inductance. These specifications can have a significant impact on circuit performance. In particular, an output capacitor with high ESR can make loop compensation difficult.
- Keep in mind that layout is vital. Don't mix signal, frequency compensation, and feedback returns with high-current returns. Arrange the grounding scheme to achieve the best compromise between ac and dc performance. In many cases, a ground plane may help. Account for the possible effects of stray inductor-generated flux on other components, and plan your layout accordingly.
- Analyze the semiconductor-breakdown ratings thoroughly, and allow for all conditions. Transient events usually cause the most trouble because they introduce stresses that are often hard to predict. Watch for the effects of feedthrough via semiconductor-junction capacitances. Such capacitances can permit excessive voltages for brief intervals at what is nominally a low-voltage node. Carefully study the breakdown, current-capacity, and switching-speed ratings on the data sheets. Ask yourself if the test conditions match your application; if you have any doubts, consult the manufacturer.
- Don't forget that the most common problem area with switching-supply designs is the inductor or transformer and that the most common difficulty involves saturation. Saturation can often result in destructive failures. An inductor or transformer becomes saturated when it can't hold any more

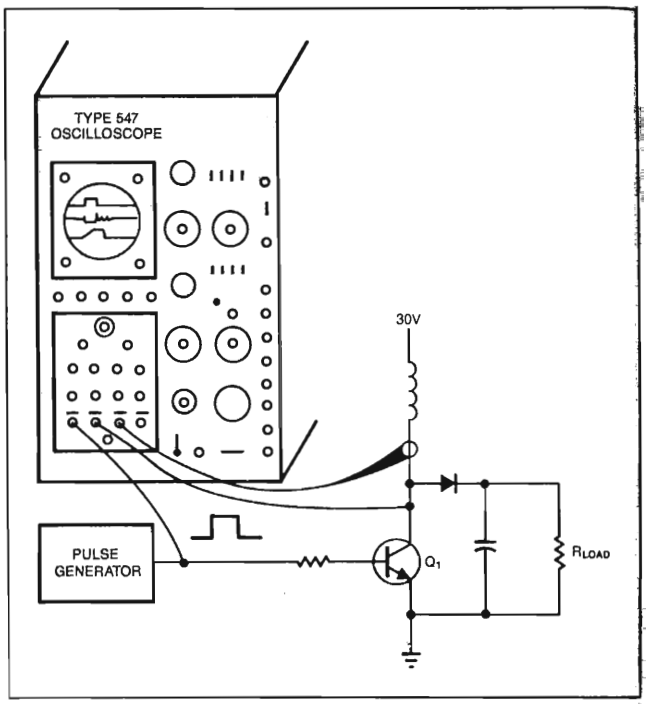
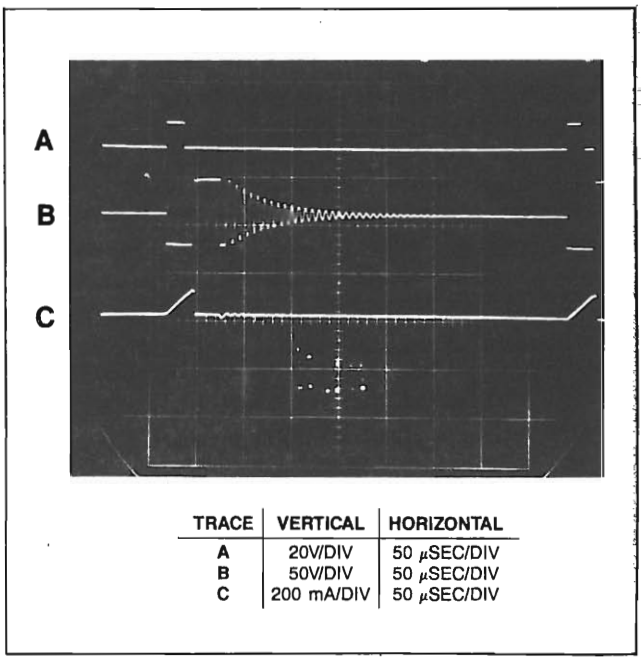


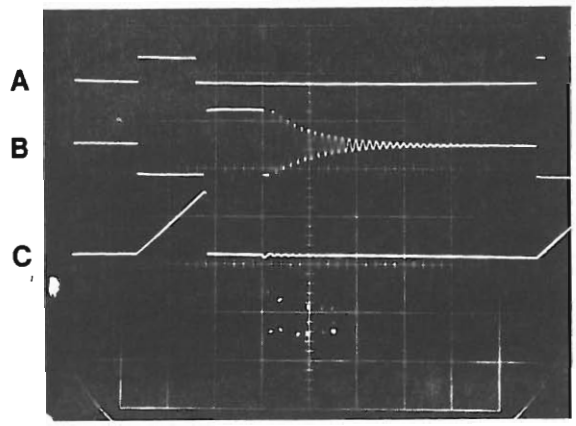
Fig 4—Using this test setup, *you can observe the effects of saturation. The pulse generator drives Q_1, forcing current into the inductor. The diode/RC combination forms a typical load.*



TRACE	VERTICAL	HORIZONTAL
A	20V/DIV	50 μSEC/DIV
B	50V/DIV	50 μSEC/DIV
C	200 mA/DIV	50 μSEC/DIV

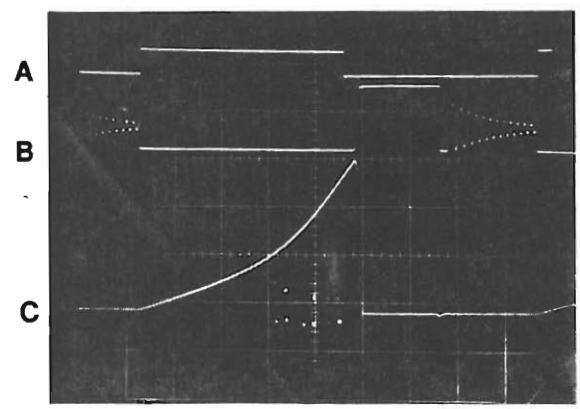
Fig 5—The voltage at Q_1's collector in Fig 4 *falls when it turns on. (Trace A is the pulse-generator output, and trace B is Q_1's collector.) Trace C, the inductor current, ramps up in a controlled fashion. When Q_1 goes off, the current falls and the inductor rings off.*

Layout is vital. Don't mix signal, frequency-compensation, and feedback returns with high-current returns.



TRACE	VERTICAL	HORIZONTAL
A	20V/DIV	50 μSEC/DIV
B	50V/DIV	50 μSEC/DIV
C	500 mA/DIV	50 μSEC/DIV

***Fig 6—Compared with Fig 5, this scope photo** shows a longer drive pulse, allowing more inductor current buildup. The current-ramp waveform is clean and controlled, meaning that the inductor has enough capacity.*



TRACE	VERTICAL	HORIZONTAL
A	20V/DIV	50 μSEC/DIV
B	50V/DIV	50 μSEC/DIV
C	500 mA/DIV	50 μSEC/DIV

***Fig 7—Longer drive pulses engender** some unpleasant results. The inductor current changes from the linear ramp shape of **Fig 6** to a nonlinear slope. This curve shows rapidly increasing current, which indicates that the inductor is reaching saturation.*

magnetic flux. As it arrives at saturation, begins to look more resistive and less inductive Under these conditions, only its dc copper resistance and the source's capacity limit the current flow.

Taking a look at the test circuit in **Fig 4** will help to illustrate the importance of the previous advice. The pulse generator drives Q_1, forcing current into the inductor. The diode/RC combination forms a typical load. In **Fig 5,** the voltage at Q_1's collector falls when it turns on (trace A is the pulse-generator output, and trace B is Q_1's collector). Trace C, the inductor current, ramps up in a controlled fashion. When Q_1 goes off, the current falls and the inductor rings off.

In **Fig 6,** the drive pulse is longer, allowing more inductor-current buildup. This buildup requires that the inductor store more magnetic flux, but the ramp waveform is clean and controlled, indicating that the inductor has the necessary capacity.

Fig 7 shows some unpleasant surprises. The drive pulse is longer still, and the inductor current departs from its linear ramp shape and changes to a nonlinear slope. The nonlinear behavior starts between the third and fourth vertical divisions, and the curve shows rapidly increasing current. The inductor is becoming saturated. If the pulse width increases much more, the current will rise to a destructive level. You should be aware that some inductors saturate much more abruptly than this one. **EDN**

Reference

1. Williams, Jim, "Regulator IC speeds design of switching power supplies," *EDN*, November 12, 1987, pg 193.

Author's biography

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor Corp, Arthur D Little Inc, and the Instrumentation Development Lab at MIT. A former student of psychology at Wayne State University, Jim enjoys tennis, art, and collecting antique scientific instruments.

Article Interest Quotient (Circle One)
High 494 Medium 495 Low 496

GUEST EDITORIAL

BY JIM WILLIAMS, STAFF SCIENTIST, LINEAR TECHNOLOGY CORP

Should Ohm's law be repealed?

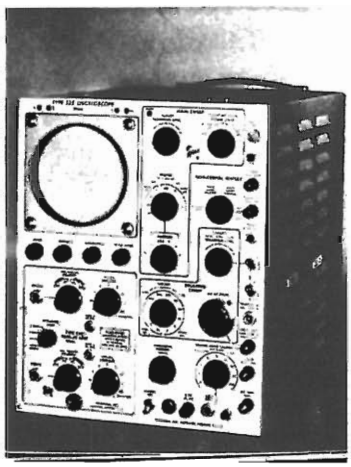
When I was a kid, I lived near the Stearn family. They had a pool, shuffleboard and tennis courts, dogs, and a horse. They also had billiard tables, a pinball machine, and a darkroom. But what interested me most was what Dr Stearn had in the basement. There, sitting on a "scopemobile," next to his workbench, was a Tektronix 535 oscilloscope. To say that I loved that oscilloscope is an understatement.

The pure, unbounded lust I spent towards this machine probably retarded the onset of my puberty, delaying sexual nascency by at least a year. It also destroyed my school performance. I read the mainframe manual instead of doing homework, and studied the small, easily hidden plug-in book in English class. I knew every 535 specification and all its operating modes. I lived for the 535, and I studied it. But, best of all, I used it.

Dr Stearn shared his electronics hobby—and his 535—with me. Oscillators, amplifiers, flip-flops, modulators, filters, RF stages—we circuit-hacked them all with ferocious intensity. And with the scope you could *see* what was going on. You shared the excitement Leeuwenhoek felt when he looked into his microscope.

The Tektronix 535 was a sublime masterpiece. In 1956, it was vastly superior to its competition. The triggered sweep worked unbelievably well, and the calibrated vertical and horizontal amplifiers really were calibrated. The scope had an astounding 15 megacycles (it was "cycles" then) of bandwidth, and it had something called "delayed sweep." The plug-in vertical preamplifiers greatly increased the measurement capability. Using that scope inspired confidence that bordered on arrogance. It would make my circuits work, or so I thought.

One afternoon I couldn't get a circuit to operate properly. The signals looked about right, but the performance was shaky, and odd effects abounded. I tested everything, but got nowhere. When Dr Stearn came by he listened, looked, and thought for a while. Then he moistened two fingers, and moved his hand around the circuit, lightly touching points as he watched the scope. He noticed effects and correlated them to his hand movements. When the scope's display looked good he soldered a small capacitor between the last two points his fingers touched. To my amazement, the circuit now worked properly. I was dumbfounded and, probably because of my frustration and embarrassment, even a little angry.



The Tektronix 535. *Introduced in 1954, this vastly superior masterpiece made a mockery of competing oscilloscopes. I knew it would make my breadboard circuits work—or so I thought.*

Dr Stearn explained that my circuit was oscillating at perhaps a hundred megacycles, and he suspected he'd damped it by loading the right points. His finger dance had surveyed suspect points; the capacitor was his equivalent of the finger-loading capacitance. "That's not fair!" I protested, "You can't see 100 megacycles on the scope." He looked right at me and spoke slowly. "The circuit doesn't care about 'fair,' and it doesn't know what the scope can't see. The scope doesn't lie, but it doesn't always tell the truth." He then gave me a little lecture that has served me well, except when I'm foolish or frustrated enough to ignore it:

"Don't ever get too attached to a way of solving problems. Don't confuse a tool, even a very good one, with knowledge. Concentrate on understanding the problem, not applying the tool. Use any tool that will help move your thinking along, know how these tools work, and keep their limitations in mind—it's part of the responsibility of using them. If you stop thinking and stop asking questions and simply believe what the scope says, you're done for. When you do that, you're not listening to the problem, and you're no longer designing that circuit. When you substitute faith in an instrument, no matter how good it is, for your judgment, you're in trouble.

"It's a tricky trap; sometimes you don't even know you're falling into it. People are very clever at fooling themselves that way. We all want things to be simple and to go smoothly, but the circuit doesn't know that and it doesn't care." That lecture took place 32 years ago, and I'm still absorbing the advice.

Lately, I've been hearing a lot about CAD systems, computer-based workstations, and powerful software-modeling techniques. At Linear Technology, we have CAD systems, and they save tremendous amounts of time. They're very powerful tools, and we're learning to use them efficiently. It's a tough process, but the rewards are worth the effort.

Unfortunately, there are substantive and disturbing differences between what these tools are, and what some purport them to be. Promotional materials, which are admittedly suspect, boast of speed, ease of use, and the elimination of mundane and odious design tasks. Advertising explains the ease of generating ICs, ASICs, board functions, and entire systems in weeks, even hours. Reading further reveals the paths to this design nirvana—databases, expert systems, models, simulators, compilers, emulators, and a lot of other intellectual frou-frou.

Somewhere, such technological manna must coalesce to eliminate messy labs, pesky nuts and bolts, and, above all, those awful breadboards. Headaches vanish, fingers and the lab remain clean, the boss is thrilled, and you have time to go fishing. Well, such silliness is all part of the marketing game, and it's well known wherever money changes hands. Perhaps my acerbic musings are simply the fears of a bench hacker or a

***Advertising for CAD tools** assures you that you can achieve high productivity with a minimum amount of effort. Becoming the next Thomas Edison is only a keystroke away.*

cantankerous computer technopeasant who is confronting the Computer Age. But I don't think so, because what I see doesn't stop at fast-talking ad copy.

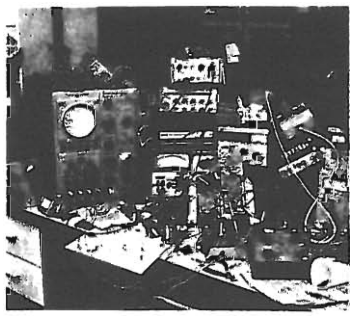
Some universities are enthusiastically emphasizing "software-based" design and "automatic-design" procedures. Students and professors have shown me circuits they designed on their computers. Some of the assumptions and simplifications the design software makes are unusual. Some of the circuits are unusual, too.

Such excessively spirited CAD advocacy is also found in industry trade journals that have become enamored of CAD methods to the point of being cavalier. Articles tell readers how easy it is to use CAD tools. At times, you can't distinguish editorial copy from advertising. For example, a recent editorial entitled "Electronic design is now computer design" informs me that:

> *"For the most part, the electronic details—the concerns of yesteryear about Ohm's law and Kirchhoff's law, transconductance or other device parameters—have been worked out by a very select few and embedded in the software of a CAE workstation or buried deep within the functionality of an IC. Today's mainstream designers, whether they're designing a complex board-level product or an IC, don't need to fuss with electronics. They're mostly logic and system designers—computer designers—not electronics designers"* ***(Ref 1).***

Those ideas pave the road to intellectual bankruptcy, and they display the kind of arrogance Dr Stearn warned me about. CAD is being oversold, and it shouldn't be, because it's one of the most powerful tools ever developed for solving problems. But if too many users are led astray and disappointed—as some already have been—CAD-system purchases, acceptance, and use will slow. Thus, the irresponsible, self-serving advisories of some CAD vendors and enthusiasts may be partially self-defeating.

The associations being made between CAD tools and the actual generation of *ideas* based on knowledge and thought are specious, arrogant, and dangerous. They're arrogant because in their determination to streamline technology they simplify it, and Mother Nature loves to throw a surprise party. Technologically driven arrogance can be hazardous, as any Titanic passenger would tell you. They're dangerous because it's easy to confuse faith in tools with the true thinking and simple sweat that are integral to design. In our rush to design



***The best circuits** result from a combination of traditional breadboard techniques, experience, and CAD.*

circuits and systems efficiently, we will cede the judgmental, inspirational, and even accidental processes that constitute much of engineering. At the same time, we'll eliminate excellence.

Most good designs are characterized by how the designer deals with the exceptions and imperfections. In my field, linear circuits, just about everything is an exception. You know about—or think you know about—a lot of the exceptions, but you're constantly learning about new ones. Unfortunately, you can get circuits to work properly without even realizing the exceptions and imperfections that are present. How sad it is that you could do better if only you knew what those exceptions and imperfections were. The linear-circuit designers I admire are those most adept at recognizing and negotiating with the exceptions and imperfections. Often they're not sure just what the specific design issues will be, but they have a marvelous sense of balance. They know when to be wary, when to use finesse, when to hack, and when to use computers. These people use CAD tools to produce superior work more efficiently, while others may be tricked into using CAD to produce mediocre designs efficiently.

CAD tools and techniques, although in their infancy, will indeed prove to be some of the most useful electrical-engineering tools ever developed. Although their usefulness in linear-circuit design is limited at present, they have had an impact on digital-IC and -system designs. For now, the best analog simulator we have is a breadboard. If you're listening, the answer, or at least the truth, is there.

I'm reasonably certain that breadboardless linear-circuit design is a long way off. I suspect the situation is similar for most engineering disciplines. The uncertainties, the surprises, and the accidents that yield fruitful results require sweat and laboratories. CAD saves time and eliminates drudgery. It can increase efficiency, but it does not eliminate the cold realities involved in making something work.

Where I work we bank on our ability to ship products that work properly. We believe in CAD as a tool, and we use it. We also use decade-resistor boxes, breadboards, oscilloscopes, pulse generators, alligator clips, screwdrivers, Ohm's law, and moistened fingertips. Like Dr Stearn back in 1956, we concentrate on solving the problem, not on simply using a tool.

Reference

1. Williams, Tom, "Electronic design is now computer design," *Editorial I/O* (a *Computer Design* newsletter), January 1988, pg 1.

CAD systems can't replace breadboards

Thanks for printing Jim Williams's timely guest editorial ("Should Ohm's law be repealed?" EDN, March 3, 1988, pg 47). CAD systems certainly save time, especially when they're used for digital design. But claiming that a CAD system can eliminate the need for breadboarding analog circuits is like claiming that a text-processing package can produce a finished manuscript without any editing.

I would very much like to see EDN further explore the current status of analog circuit design. The gradual demise of analog courses in engineering schools is an important area of concern. Another is the replacement of simple analog circuits with complex programmable logic. Still another is the shunning, by digital-computer designers, of the analog computer, which is a well-established, real-time, parallel processor.

Forrest M Mims III
Seguin, TX

Circuits cannot live by breadboarding alone

I must take issue with the impression created by both Jim Williams's guest editorial "Should Ohm's law be repealed?" (EDN, March 3, 1988, pg 47) and Forrest M Mims III's supporting letter "CAD systems can't replace breadboards" (EDN, May 12, 1988, pg 32). Both Williams and Mims seem to long for a return to pre-CAE days.

Analog-circuit simulation must be used in conjunction with breadboarding. Neither is sufficient on its own. How many times has an engineering breadboard functioned correctly, meeting all performance specifications (even over temperature), and then a team of engineers has had to "live" in the assembly line because the first production boards couldn't be built? CAE is simply the only viable method we have of performing worst-case, tolerance, and stability analysis in an economic and timely fashion. Sometimes the wrapped up in the requirement that we must always have the slickest, best, fastest, and most state-of-the-art tools to get the job done. Sometimes I wonder how anything was ever designed before we had HP calculators, personal computers, and engineering workstations. Many designs have been done without the aid of any of these tools, and hopefully many more will be in the future.

I am not a Luddite when it comes to using tools to do a better job. However, I think that our colleges are turning out students that need the latest equipment to get the job done. This situation has been caused in part by employers who expect engineers fresh out of school to be versed in the latest equipment and ready for design work. The end result is that the education the students receive is leaning more toward practical skills and less toward theoretical skills and a broad education. I believe that in the long run this situation will be detrimental to the engineer's ability to keep up with technology or adapt to a different technology should the job require it.

Let's not forget that you can accomplish a lot by using the best computer available (the one between your ears), a little common sense, and a logical approach to a problem. Sometimes the simplest solution is the best solution.

Joe Blaschka, Jr, P E
President
Adcomm Engineering Co
Kirland, WA

Clever techniques improve thermocouple measurements

Thermocouple (TC) measurements require linear-circuit proficiency. To ensure accurate results, you should understand the need to compensate for parasitic junctions, the importance of certain characteristics of the op amps and associated components, and the ways to otherwise condition and linearize the TC's low-level output signals.

Jim Williams, *Linear Technology Corp*

Thermocouples are inexpensive, but achieving reasonable accuracy—say ±0.5°C—requires careful signal conditioning and cold-junction compensation. Although thermocouples don't require any external excitation, and their small size and low output impedance produces wideband, low-noise output signals, their nonlinear, millivolt-level outputs degrade measurement sensitivity.

A TC senses ambient temperature by producing, across the junction, a small voltage proportional to temperature. To measure that voltage, you must connect the TC wires to an amplifier or voltmeter, creating two unwanted parasitic junctions that produce error voltages in series with the desired signal (**Fig 1**). These parasitic junctions must have the same temperature. To interpret the TC voltage as an absolute-temperature signal, you must either maintain these parasitic junctions at a known temperature or compensate for their effect electronically. The TC, in effect, measures temperature at its "hot" junction with respect to temperature at the two parasitic junctions—historically called the "cold junction."

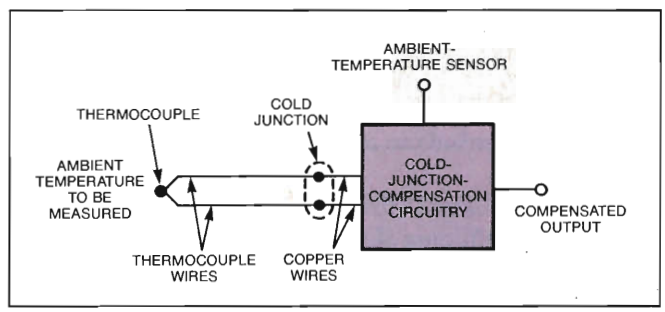


Fig 1—For accurate thermocouple measurements, *the thermocouple's cold junction and the compensation circuit's temperature sensor must be isothermal.*

Cold junctions generate spurious voltage

The term "cold junction" derives from the practice of maintaining the parasitic junctions at 0°C by immersing them in a mixture of ice and water. Although very accurate, this approach is impractical for most applications. As another option, you can simulate the ice bath by servo-controlling a Peltier cooler, but again this approach is too complex and bulky for most applications.

Thermocouples are by far the most widespread contact-type temperature transducers in use today.

A better technique (**Fig 2a**) employs an electronic-compensation circuit, which tracks the cold-junction temperature instead of maintaining the junction at a constant temperature. The circuit offers the same result as an ice bath, but is simpler to implement. It produces 0V at 0°C, and its slope of output voltage vs temperature is the same as that of the thermocouple, over the expected range of cold-junction temperatures. For proper operation, the compensator's temperature sensor must be isothermal with the cold junction.

The cold-junction compensator, IC_1, measures the cold-junction's ambient temperature and generates output voltages that are scaled for use with E-, J-, K-, R-, S-, and T-type thermocouples. Low supply current in

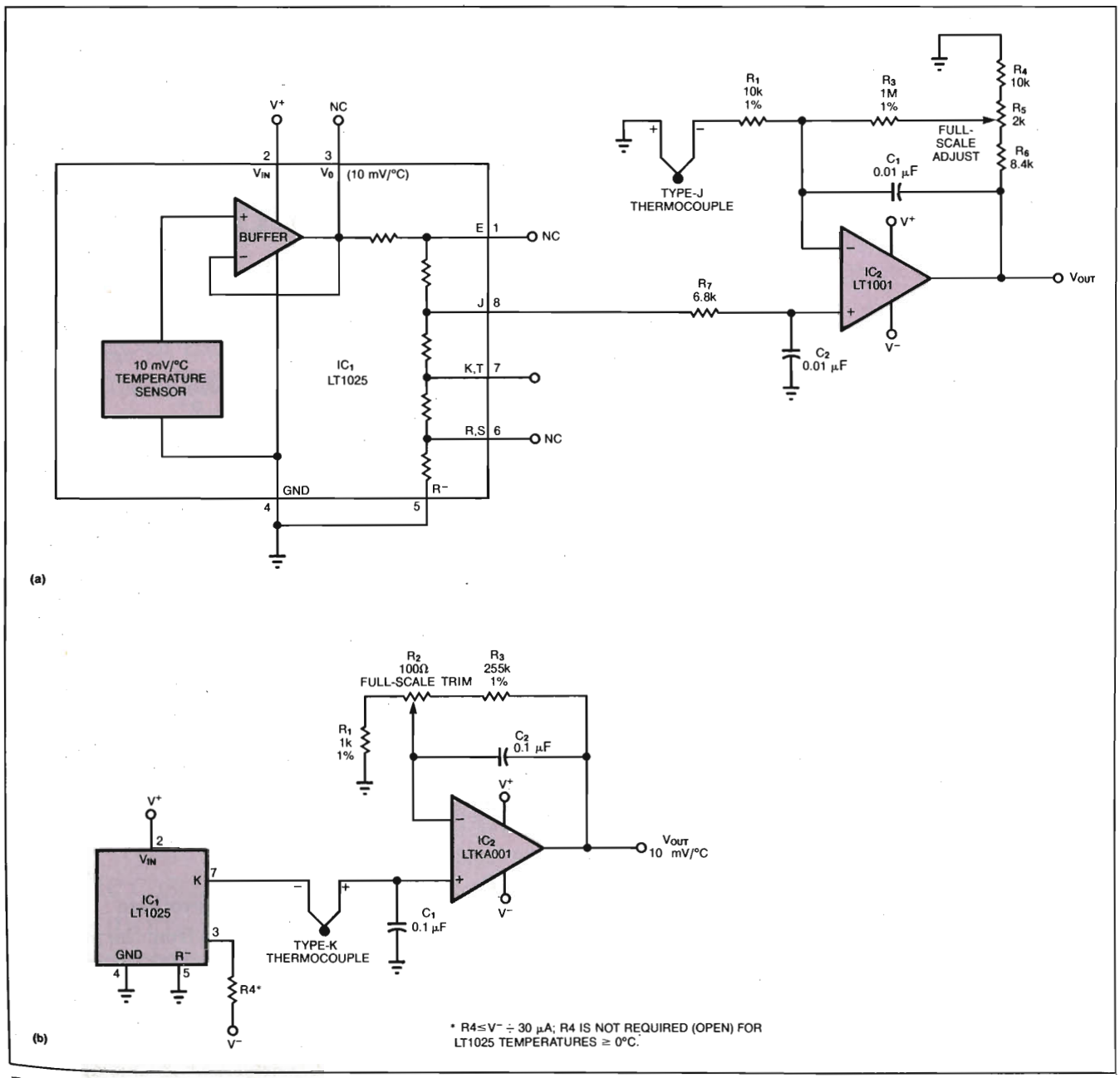


Fig 2—Each of these circuits combines the thermocouple's output *with the electronic cold-junction compensation of IC_1. Circuit* ***a*** *subtracts these voltages; circuit* ***b*** *arranges the voltages in a series-opposed fashion and amplifies the difference.*

IC_1 minimizes the self-heating that would otherwise degrade isothermal operation with the cold junction; low power consumption also supports battery operation. The chip's ±0.5% accuracy is compatible with the overall accuracy achievable in a thermocouple-based system.

Subzero temperature swings V_{OUT} negative

The op amp in **Fig 2a** amplifies the difference between the thermocouple voltage and the cold-junction-compensation voltage from IC_1. C_1 and C_2 provide filtering, and potentiometer R_5 trims the signal gain. R_6 has a typical value; another value may better accommodate the desired trim range. Reducing R_6 and increasing R_5, for example, will provide higher gain with lower trim resolution. **Fig 2b** shows a similar circuit, for a type-K thermocouple, which combines the TC and compensation voltages in series-opposed fashion. The optional pulldown resistor (R_4) allows V_{OUT} to swing negative, thereby representing sub-0°C temperatures.

Low bias current in IC_2 is important to avoid offset errors due to the op amp's input filter (R_7, C_2) and the output impedance of IC_1. Type-J, -K, -E, and -T thermocouples, which have Seebeck coefficients of 40 to 60 μV/°C, require high-grade precision bipolar amplifiers such as **Fig 2b**'s LTKA001. (This device provides 30-μV offset voltage, 1.5-μV/°C drift, and 1-nA input bias current.)

Particularly critical applications call for a chopper-stabilized amplifier such as **Fig 2b**'s LTC1052 (5-μV offset, 0.05-μV/°C drift, 30-pA input bias current, and 30×10^6 open-loop gain). This amplifier is appropriate for use with type-R and -S thermocouples (whose Seebeck coefficients range from 6 to 15 μV/°C), especially if the application covers a large swing in ambient temperature or does not allow offset adjustments.

Another source of error in thermocouple amplifiers is inadequate open-loop gain. An amplifier for type-K thermocouples, for instance, which produces 100 mV/°C, must have a closed-loop gain of 2500. In this application, an ordinary op amp that specs a minimum open-loop gain of 50×10^3 would produce a (2500/50,000)×100=5% gain error! Although normally you would calibrate the closed-loop gain by trimming, temperature drift in the open-loop gain can still degrade the output accuracy. The minimum recommended open-loop gain for use with type-E, -J, -K, and -T thermocouples is 250,000. This value is also adequate for use with type-R and -S thermocouples, if the amplifier's output produces 10 mV/°C or less.

Eschew kovar package leads

Regardless of the type of op amp that you choose, a dual-in-line package is preferable to a TO-5 metal can, especially if the op amp's supply current exceeds 500 μA. The TO-5's kovar leads introduce thermocouple effects that can generate ac and dc offsets in the presence of external air motion or thermal gradients in the package.

You should also be aware of considerations related to, but external to the thermocouple amplifier itself. These include overvoltage protection, common-mode voltage, and noise. Protection is necessary because thermocouple wires often pick up static voltages or make contact with high voltage that can damage the amplifier circuit.

The R_{LIMIT} resistor in **Fig 3a,** for instance, attenuates

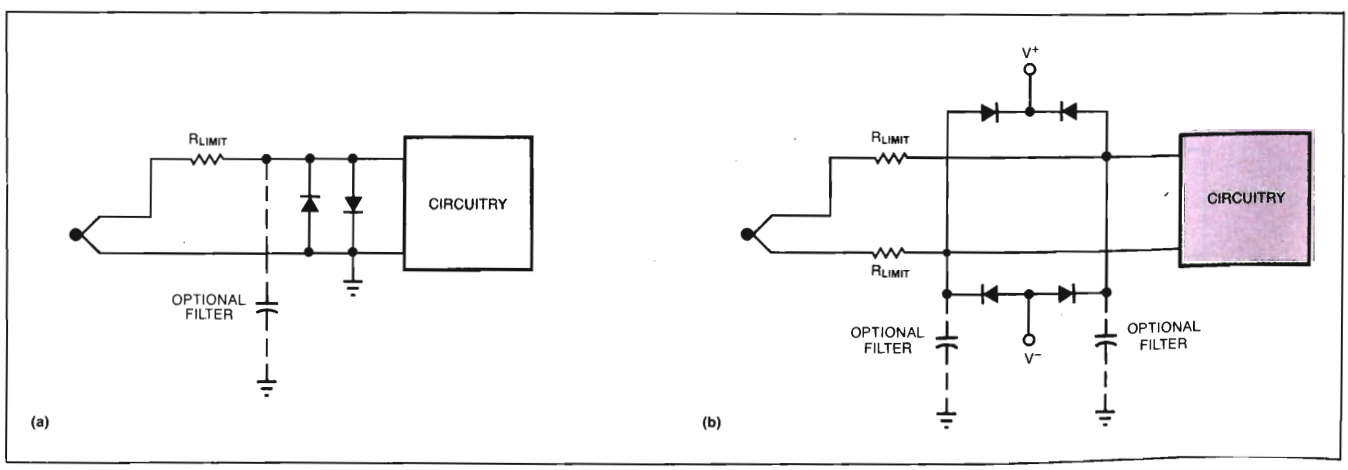


Fig 3—The resistors you see here protect the circuits *from overvoltage on the thermocouple lines. The optional capacitors provide signal filtering for grounded or battery-operated systems* ***(a)****, or for systems* ***(b)*** *subject to open ground connections or open thermocouple lines.*

Electronic cold-junction compensation tracks the junction temperature instead of maintaining the junction at a constant temperature.

fault voltages. And, by adding a capacitor (shown as dashed lines), you can obtain signal filtering as well. **Fig 3b**'s circuit shows balanced protection for a differential input. Again, connecting the optional capacitors provides lowpass signal filtering in addition to overvoltage protection. The diodes are effective in clamping the signal path to the supply voltages, but you must evaluate the effect of diode-leakage currents, especially if the limit resistors have high values. Similarly, bias currents flowing into the amplifier circuitry through high-value limit resistors can generate measurement errors. In some cases you must compromise accuracy to meet a system's requirements for voltage protection and noise rejection.

The amplifier circuit of **Fig 4** combines filtering with full differential sensing of the thermocouple voltage. If all signals remain within the supply-voltage range of the switched-capacitor building block (IC_1), the circuit provides 120 dB of common-mode rejection. (If the signals exceed this range, the circuit may require protection networks as discussed with regard to **Fig 3**.) Switch action within IC_1 transfers charge from the external "flying capacitor" C_1 to the external output capacitor, C_2. You can vary this rate of transfer, and hence the overall bandwidth, by controlling the chip's commutating frequency. Resistor R_1 provides a bias-current path for IC_1's floating inputs, and the pulldown resistor (shown as dotted lines) enables subzero-temperature readings.

Protection networks and differential operation may not suffice in thermocouple applications that have high levels of noise and common-mode voltage. Industrial

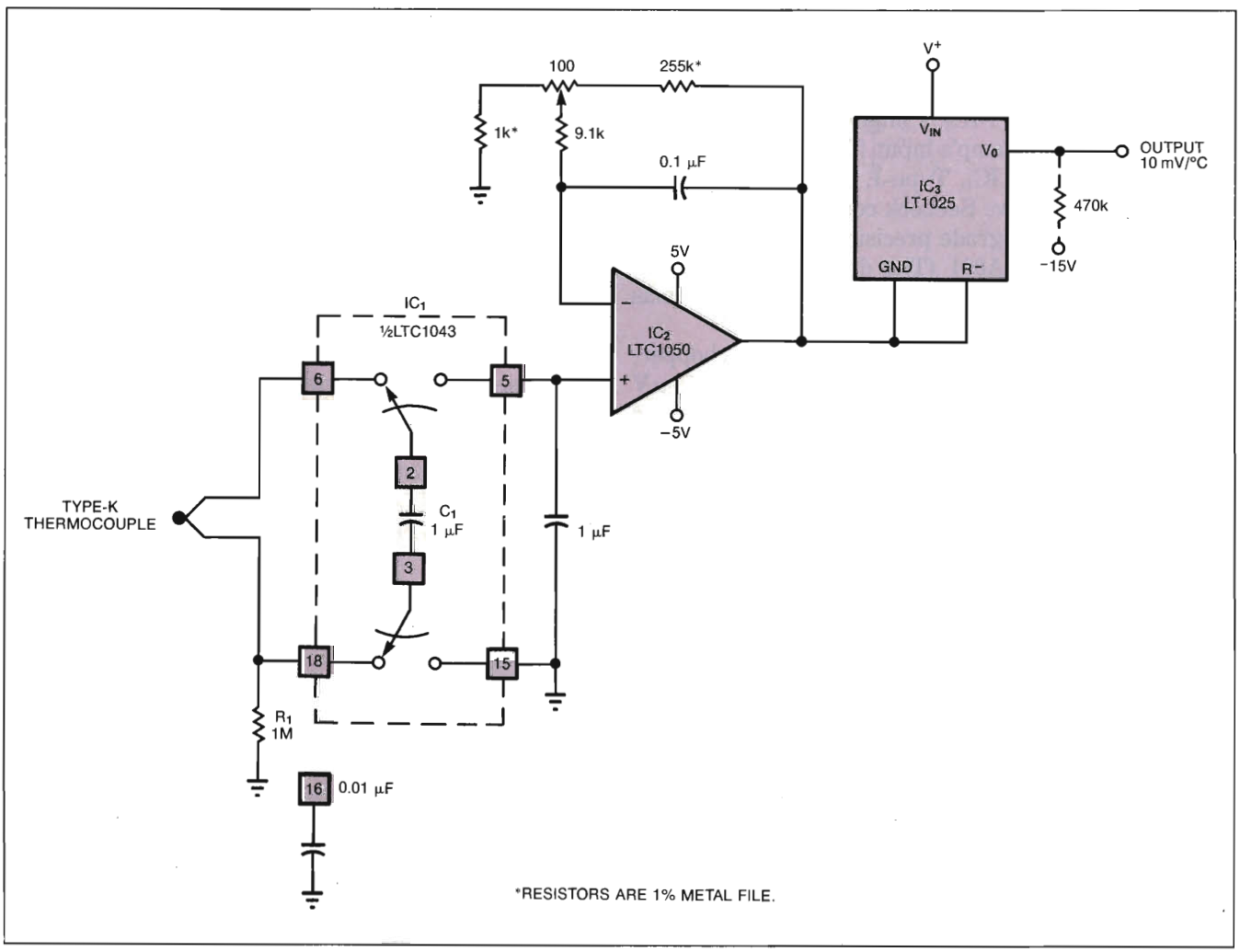
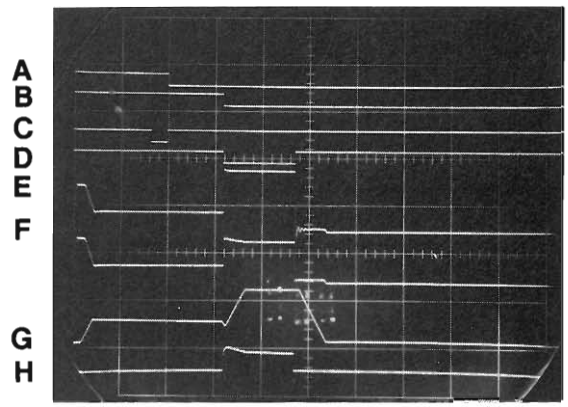


Fig 4—This differential-input thermocouple amplifier *implements "flying capacitor" isolation with a switched-capacitor circuit (IC_1).*

environments, for example, can generate ground-potential differences of 100V or more. For these conditions, you must galvanically isolate the thermocouple and its signal-conditioning circuitry from ground. The circuit requires a fully isolated power source and an isolated signal-transmission path that is referred to ground at the output. Careful design allows a single path to transfer both the floating power and the isolated signals. What's more, thermocouples allow you to trade bandwidth for dc accuracy.

One transformer isolates signal and power

The isolated signal conditioner of **Fig 5** provides ±0.25% accuracy in the presence of 175V common-mode voltages. A single transformer, T_1, transmits the isolated power and data. First of all, take note of the oscillator circuit consisting of inverter IC_{1A} and associated components, which generates the clock signal shown in **Fig 6,** trace A. Inverters IC_{1B}, IC_{1C}, and associated components stretch the positive pulses in this signal (trace B), and apply them to the 2.2-kΩ resistor, R_1. The pulse amplitudes are stable because the inverters obtain a stable supply voltage from the (approximate) 10.7V regulator consisting of IC_2 and IC_3.



TRACE	VERTICAL	HORIZONTAL
A	50V/DIV	50 μSEC/DIV
B	50V/DIV	50 μSEC/DIV
C	50V/DIV	50 μSEC/DIV
D	50V/DIV	50 μSEC/DIV
E	10V/DIV	50 μSEC/DIV
F	10V/DIV	50 μSEC/DIV
G	10V/DIV	50 μSEC/DIV
H	50 mA/DIV	50 μSEC/DIV

Fig 6—These waveforms depict selected signals from Fig 5's circuit. *The negative-pulse level in trace E, for example, represents the desired thermocouple temperature.*

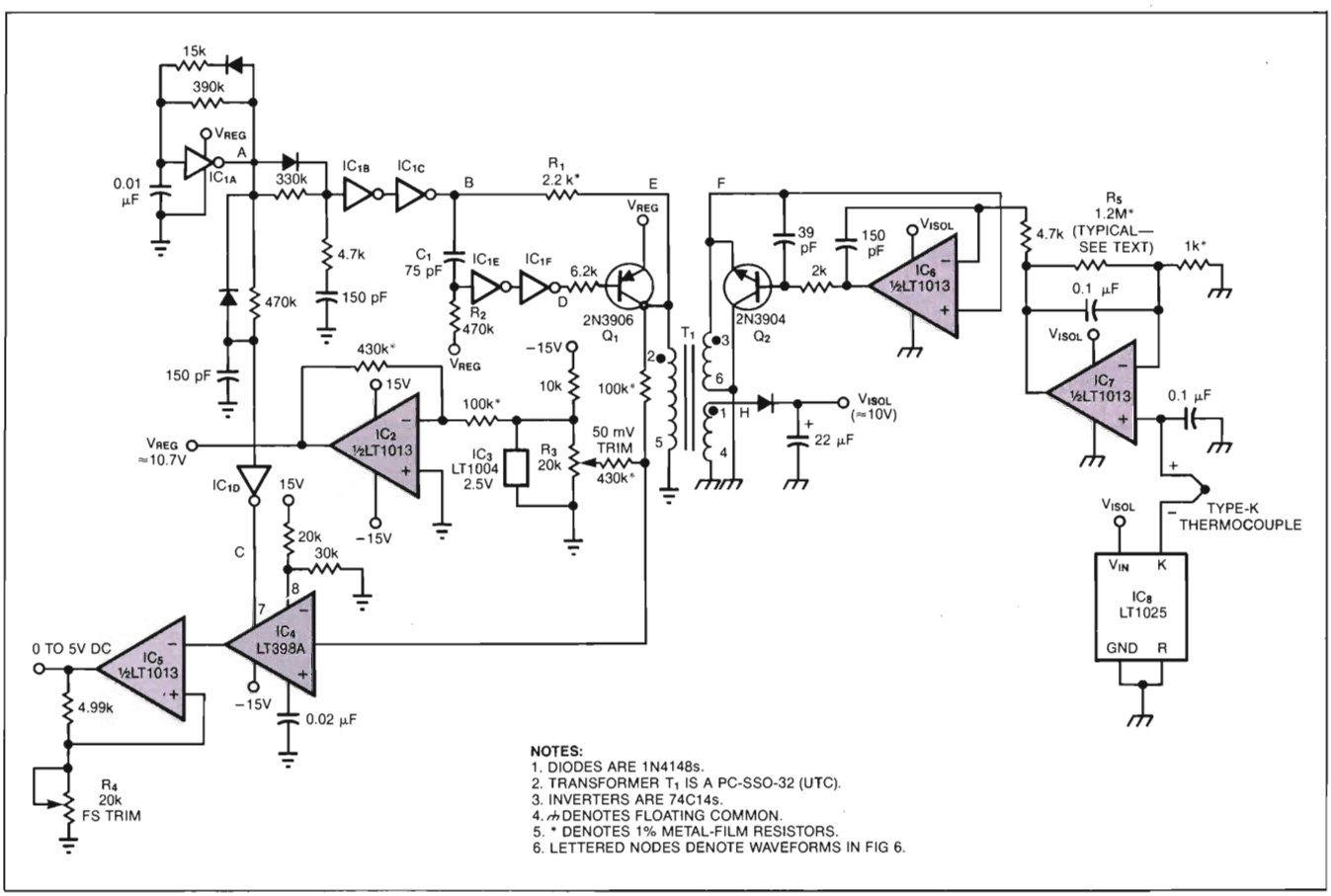


Fig 5—Transformer T_1 provides 175V isolation *for the power and signals of this thermocouple-signal conditioner. Accuracy is ±0.25%.*

Protection networks and differential operation may not suffice in thermocouple applications that have high levels of noise and common-mode voltage.

Current pulses in R_1 drive the primary of T_1 (trace E), producing voltage pulses in the secondary (the emitter of Q_2, trace F). Op amp IC_6 compares this signal with the conditioned thermocouple voltage that op amp IC_7 produces. By driving the base of Q_2, IC_6's output (trace G) forces the transformer's secondary voltage (pin 3) to clamp at the level of IC_7's output. The clamping action is active for low output voltages because Q_2 operates in the inverted mode.

T_1's primary voltage clamps in response to a clamp on the secondary voltage. After IC_6's output settles, the stable, clamped primary voltage represents the thermocouple's output signal. Meanwhile, a delayed clock signal (trace C) from inverter IC_{1D} controls the sample/hold amplifier, IC_4, causing that device to sample the T_1 primary voltage. IC_4 returns to the hold mode when the clock waveform (trace A) goes low. Potentiometer R_3 adjusts the sample/hold signal's offset, and potentiometer R_4 adjusts the gain.

When IC_{1C}'s output (trace B) makes a high-to-low transition, the differentiator action of C_1 and R_2 causes IC_{1F}'s output (trace D) to temporarily go low. Q_1 turns on, forcing substantial energy into the primary of T_1. The resulting flux through T_1's secondary (pins 3, 6) disrupts the equilibrium of IC_6's feedback loop, causing the output to saturate (trace G). The excess flux energy then dumps into the other secondary (pins 1, 4), forcing a surge of current into the storage capacitor, C_3. Each clock cycle generates such a current pulse, producing an isolated, dc supply voltage, V_{ISOL}.

You should be aware of several factors that affect the operation of **Fig 5**'s circuit. Transformer characteristics, for example, form the primary limit on achievable accuracy. The clamping scheme relies on avoiding saturation of the transformer's core. The clamp interval must be short, and T_1's primary current during this interval should remain extremely low with respect to the core-saturation value. The power-refresh pulse occurs immediately after the data transfer rather than before, to allow a pause for the transformer's core to recover from saturation. The low clock frequency (350 Hz) ensures adequate time intervals for this purpose; the resulting low bandwidth is not of consequence in most thermocouple applications.

To trim the circuit's gain, select R_5 (IC_7's feedback resistor) according to the desired maximum temperature and the thermocouple type. You should set IC_7's output to 50 mV before adjusting the offset trim (R_3); the circuit cannot read IC_7 outputs below 20 mV because of saturation in Q_2. The drift of the output voltage vs temperature depends on constant-magnitude current pulses into the primary winding of T_1, which in turn depends on the temperature coefficient of the copper used in the winding. R_1, however, swamps this effect by acting as a current source for the winding, leaving a residual temperature coefficient of about 60 ppm/°C. IC_{1C}'s saturation resistance, fortunately, has an opposite-polarity temperature coefficient that partially compensates for the residue. The overall temperature coefficient, including that of IC_3, is about 100 ppm/°C.

Although more complex than its **Fig 5** counterpart, the isolation amplifier of **Fig 7** offers 0.01% accuracy and a typical drift of 10 ppm/°C—performance that is suitable for servo systems and high-resolution applications. As in **Fig 5**, a single transformer transfers the

In case you don't remember Dr Seebeck

Thermocouples are by far the most widespread temperature sensors in use today. Their principle of operation, however, dates back to 1822, when an Estonian physician discovered the thermocouple effect by accident. While studying the effects of heat on galvanic connections, Thomas Seebeck joined a piece of copper to a piece of bismuth, forming a loop. He then noted that a nearby compass was indicating a magnetic disturbance. Not realizing that electric current was flowing, Seebeck labeled the effect "thermomagnetism."

He went on to experiment with different combinations of metals and eventually published the results of his work **(Ref 1)**. Further investigations, of course, have established that "thermomagnetism," now known as the "Seebeck effect," is a reliable and repeatable electrical phenomenon.

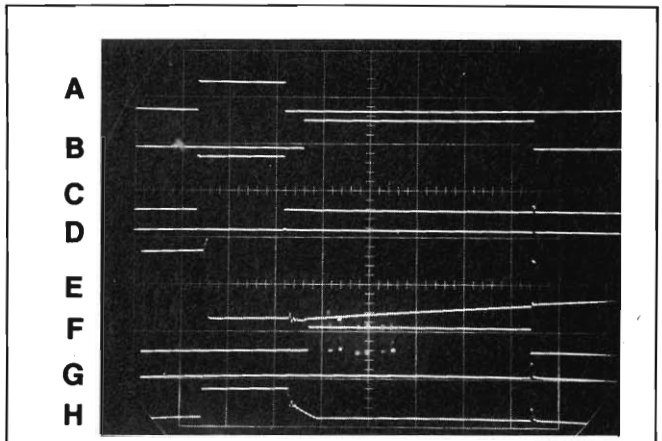
Reference

1. Seebeck, Thomas, *Magnetische polarisation der metalle und erze durch temperatur-differenz*, Abhaandlungen der Preussischen Akademic der Wissenschaften, 1823, pg 265-373.

isolated data and power. The thermocouple voltage, however, undergoes pulse-width modulation before coupling across the transformer. The circuit then demodulates this signal back to dc.

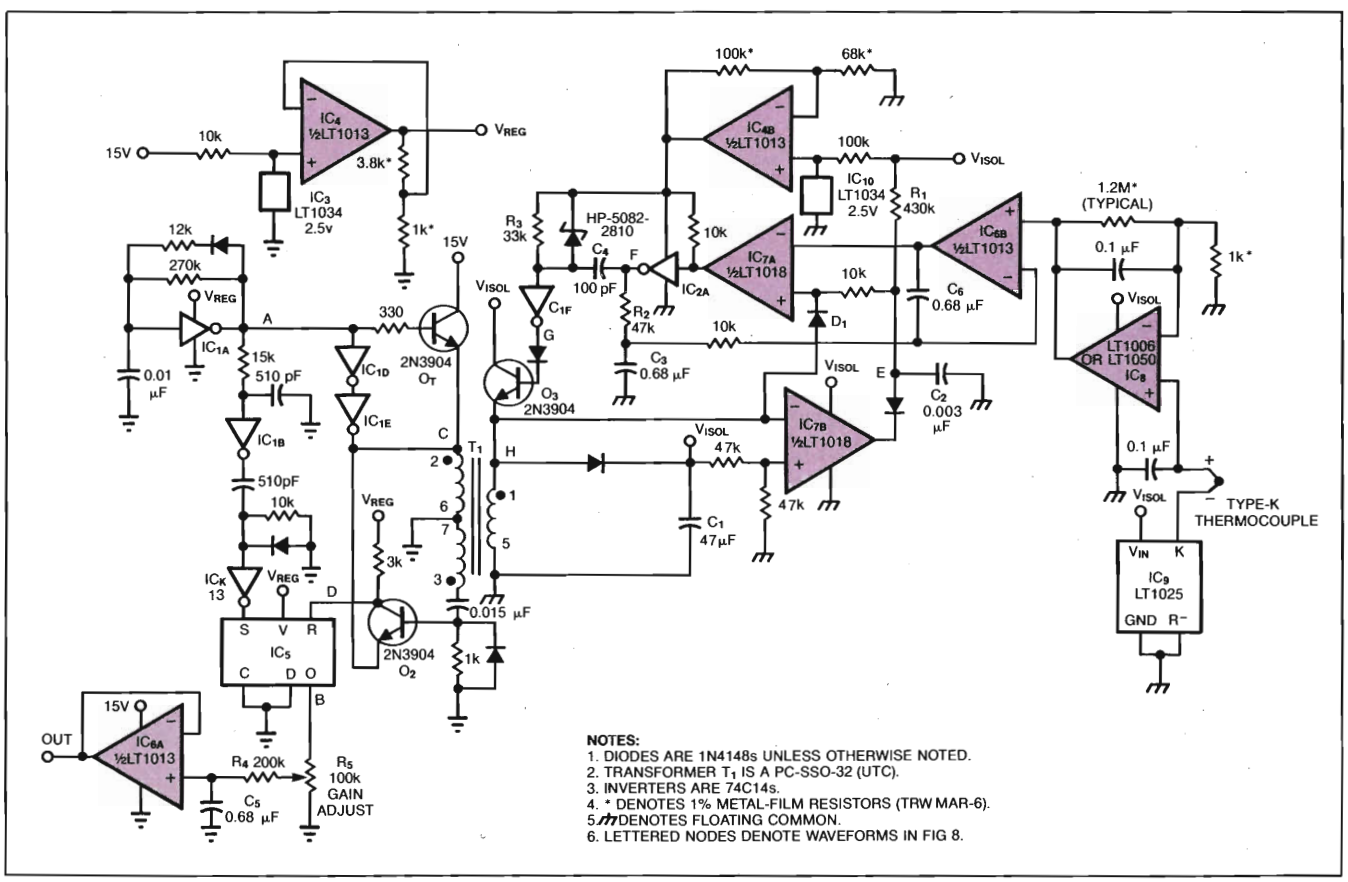
Again, inverter IC_{1A} generates the clock waveform (**Fig 8**, trace A). This waveform's high-to-low transition sets flip-flop IC_2 (trace B), after a small delay introduced by inverters IC_{1B}, IC_{1C}, and associated components. The clock signal, buffered by inverters IC_{1D} and IC_{1E}, also drives the primary of T_1 (trace C). As a result, the T_1 secondary receives energy and delivers it to the storage capacitor, C_1, creating V_{ISOL}, the isolated supply voltage for that side of the circuit.

Besides generating V_{ISOL}, pulses in the T_1 secondary clock the pulse-width modulator, a closed-loop circuit that includes IC_{4B}, IC_{6B}, IC_{7A}, and IC_{7B}. Op amp IC_8 amplifies the thermocouple signal and applies it to the noninverting input of IC_{6B}, which in turn servo-biases comparator IC_{7A}. Each time that IC_{7B} allows C_2 (trace E) to receive charge via resistor R_1, IC_{7A} produces a pulse whose duration is proportional to the thermocouple voltage. After inversion by IC_{2A}, these pulses also drive the R_2/C_3 integrator, which delivers a dc voltage to the inverting input of IC_{6B}. C_6 provides compensation for the feedback loop.



TRACE	VERTICAL	HORIZONTAL
A	20V/DIV	50 μSEC/DIV
B	20V/DIV	50 μSEC/DIV
C	10V/DIV	50 μSEC/DIV
D	20V/DIV	50 μSEC/DIV
E	2V/DIV	50 μSEC/DIV
F	10V/DIV	50 μSEC/DIV
G	10V/DIV	50 μSEC/DIV
H	20V/DIV	50 μSEC/DIV

***Fig 8—The positive pulse width in trace B of the Fig 7 circuit** corresponds to the thermocouple's temperature.*



NOTES:
1. DIODES ARE 1N4148s UNLESS OTHERWISE NOTED.
2. TRANSFORMER T_1 IS A PC-SSO-32 (UTC).
3. INVERTERS ARE 74C14s.
4. * DENOTES 1% METAL-FILM RESISTORS (TRW MAR-6).
5. DENOTES FLOATING COMMON.
6. LETTERED NODES DENOTE WAVEFORMS IN FIG 8.

***Fig 7—In this isolation circuit,** pulse-width modulated thermocouple signals are transferred across the transformer barrier. Accuracy is ±0.01%.*

Variations in ambient temperature, supply voltage, and clock frequency have little effect on the PWM isolation amplifier's signal output.

Circuit accuracy demands stable pulse widths at the output of IC_{2A}. IC_{2A}'s low-loss, MOS switching characteristics contribute to the precise timing necessary, as does the stabilized supply voltage that IC_{4B} provides. The stability of the operating frequency (set by inverter IC_{1A}) has little effect on the pulse widths because this frequency is common to the primary-side demodulation scheme.

Demodulation proceeds as follows: C_4 and R_3 differentiate the negative-going edge of IC_{2A}'s output, causing IC_{1F} to deliver a pulse (trace G) to the base of Q_3. In response, Q_3 delivers a fast spike to T_1's secondary (trace H). (Diode D_1 at IC_{7A}'s noninverting input breaks a regenerative loop that could cause oscillation.) T_1's primary section between pins 7 and 3 receives the spike, which then drives the base of Q_2. Q_2 behaves as a clocked demodulator, pulling its collector low (trace D) only when its base is high and its emitter is low—when T_1 is transferring data rather than power.

The collector spike from Q_2 resets flip-flop IC_5. Like IC_{2A}, this flip-flop is an MOS device powered by a stable supply (obtained from IC_4), and clocked by the same frequency as the pulse-width modulator. As a result, the flip-flop's Q output signal has a dc-average value that depends primarily on the desired thermocouple signal at IC_8's output. Variations in the ambient temperature, supply voltage, and clock frequency have little effect.

Delay translates to offset error

Filter components R_4 and C_5 extract the signal's dc value; R_5 permits adjustment of the overall gain. The voltage follower, IC_{6A}, produces the circuit's output. Because this scheme depends on the accurate timing of edge signals at the flip-flop, you must account for the small delay in discharging C_2 (trace E) to avoid a small offset error. The delay in IC_5's S (set) line compensates for this error by setting the rising edge of trace B coincident with that of trace F. Trace B's falling edge requires no such compensation because wideband cir-

Additional error sources in thermocouple systems

You must exercise care in processing the low-level signals that thermocouples produce. In general, thermocouple *system* accuracies greater than 0.5°C are difficult to achieve. Besides the major sources of error that the accompanying article discusses in detail, you should be aware of the effects that the connection wires, cold-junction uncertainties, and the faulty placement of sensors can have.

The wires that you use to connect a thermocouple and its conditioning circuitry form additional, unwanted thermocouple junctions. You should maintain these junctions at the same temperature to minimize their effect, which you can usually do by mounting them close togther. In some cases, you can eliminate a junction by selecting appropriate connecting wires and other accessories; consult **Ref 1**, for example.

The joining of dissimilar metals always produces a thermocouple junction. Such dissimilar metals include the leads of IC packages (kovar in TO-5 cans; alloy 42 or copper in DIPs), and a variety of other metals found in plating finishes and solders. The net effect of all these thermocouple junctions will be zero if they all have the same temperature, but power dissipation usually causes temperature gradients within an IC package or a pc board. Accordingly, you should use extreme care to ensure an absence of temperature gradients, in the vicinity of the thermocouple terminations, in the cold-junction compensator, and in the thermocouple amplifier.

If you can't eliminate a given temperature gradient, then position the sensitive leads isothermally. In the schematics in the accompanying article, sensitive leads include the LT1025's R^- and output pins, the amplifier-input pins, and leads for the gain-setting resistors. One effect to watch for is the apparent drift in an amplifier's offset voltage during warmup. Such an error can amount to tens of microvolts, especially in TO-5 cans with kovar leads—even if drift measures zero for the chip itself.

Junctions infest IC package

The culprit, of course, is mismatched thermocouple materials within the package, in the path from lead frame to bonding wire to IC metallization to silicon. (Lead frame to bonding wire is the dominant junction.) The effect is proportional to power dis-

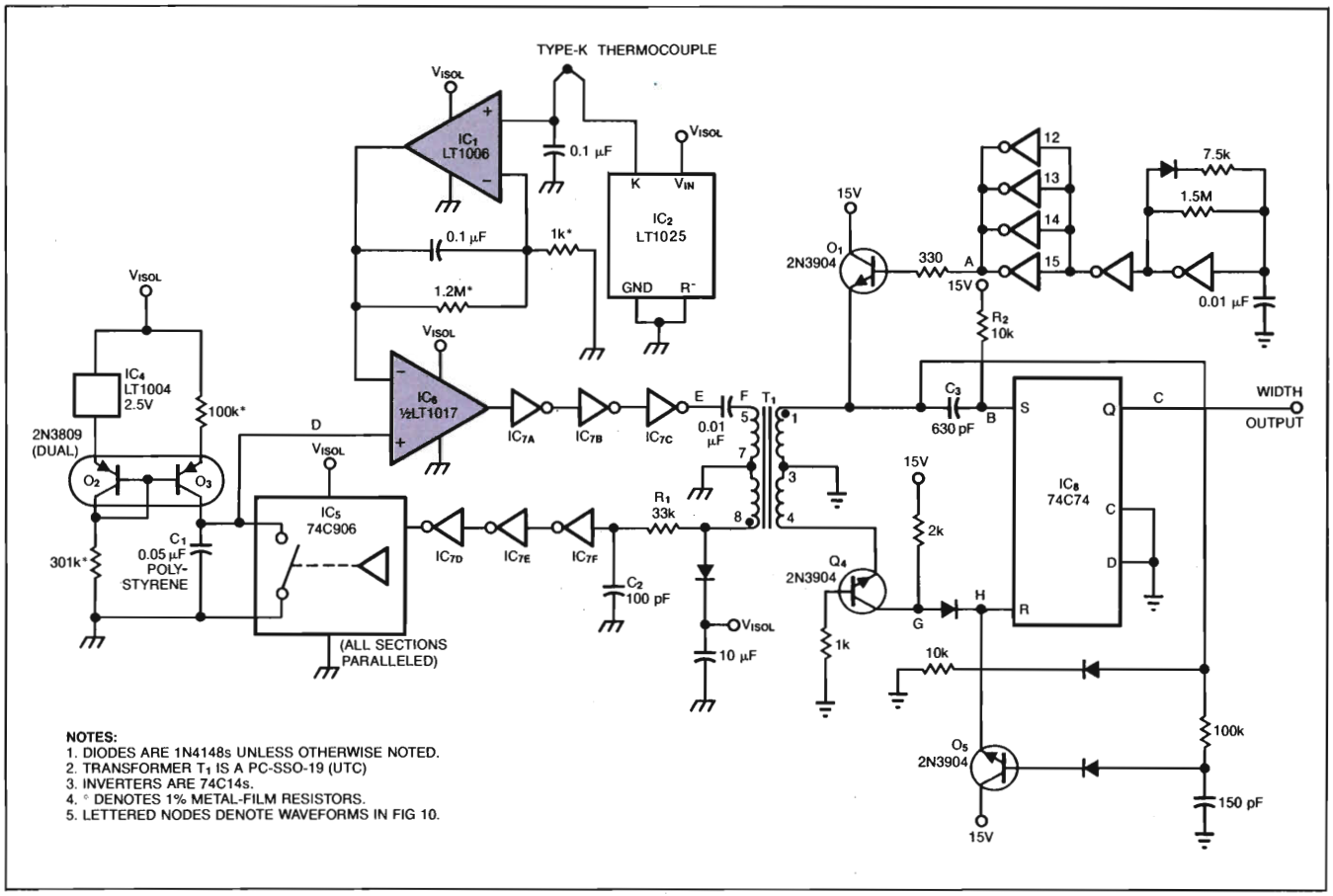


***Fig 9—This thermocouple amplifier** provides signal conditioning, isolation, and a pulse-width modulated output.*

sipation, and you can minimize it by choosing ICs that draw low supply current, by operating them at low supply voltages, and by avoiding TO-5 cans. You can accommodate the remaining drift by specifying a 5-minute warmup before calibrating the system or measuring its performance.

The thermocouple's cold junction is another significant source of error. A true cold junction (ice-bath reference) will contribute error according to slight deviations from the desired temperature, but an active-compensator IC makes errors in the process of sensing and tracking the ambient temperature. You must take measures to ensure accurate tracking by maintaining the cold junction and the IC at the same temperature. These measures include the use of high-thermal-capacity blocks and thermal shrouds.

Because a thermocouple measures its own temperature, the placement of the thermocouple can also be a source of error. In fluid systems, for instance, eddy currents or the effects of laminar flow around the thermocouple can cause remarkably large errors. Even a simple surface measurement can be inaccurate because of poor thermal conductivity between the surface and the sensor.

Silicone thermal grease can ease this problem, and you should mate as much of the sensor surface as possible to the measured surface. (Ideally, the thermocouple should lodge tightly in a hole drilled in the surface.)

Keep in mind that thermocouple leads act as heat pipes that provide direct thermal paths to the sensor. This isn't a problem if the surface has a large thermal capacity, but other situations may require some thought. For example, you might thermally mate the lead wires to the surface. Also, coiling the wires within the ambient temperature of interest will minimize their heat-pipe effects. You should be skeptical of results, even for applications that are apparently simple. Experiment with several sensor positions and mounting options, and if the results agree you are probably on the right track.

Reference

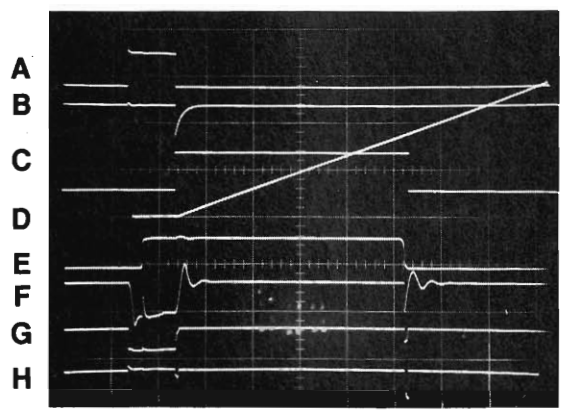
1. *Omega temperature measurement handbook*, Omega Engineering, Stamford, Connecticut, 1987.

Linearizing a thermocouple's signal voltage simplifies further signal processing in many applications.

cuit elements make up that signal path (IC_{1F}, Q_3, T_1, and Q_2). Again, you can obtain 10-ppm/°C overall drift and 0.01% linearity by using the resistors specified and by matching the voltage references, IC_3 and IC_{10}, for drift.

Using similar techniques, you can construct a 0.25%-accurate, isolated, thermocouple-signal conditioner that provides a digital PWM output (**Fig 9**). The inverters of IC_3 produce a buffered clock signal (**Fig 10**, trace A). Q_1 drives T_1. Concurrently, the R_2/C_3 differentiator provides a spike (trace B) that sets flip-flop IC_8 (trace C). The clock pulse applied to T_1's primary appears at the secondary (pin 8), where it drives the V_{ISOL} supply. The pulse also causes the paralleled, open-drain switches within IC_5 to close, which discharges C_1. (The R_1/C_2 filter prevents oscillation due to regenerative feedback.)

Current from the Q_2/Q_3 current source begins to recharge C_1 when the pulse ends. The resulting voltage ramp (trace D) drives one input of comparator IC_5; the signal related to the thermocouple voltage drives the other input. The comparator switches high when these voltages reach equality, causing a pulse to ripple down the IC_{7A}, IC_{7B}, IC_{7C} inverter chain (trace E) and drive T_1's secondary. (Three inverters serve to sharpen the signal's low-to-high transitions.) As a result, T_1's primary produces a negative spike (pin 4) that biases Q_4, causing its collector to go low (trace G).



TRACE	VERTICAL	HORIZONTAL
A	20V/DIV	50 μSEC/DIV
B	20V/DIV	50 μSEC/DIV
C	20V/DIV	50 μSEC/DIV
D	0.05V/DIV	50 μSEC/DIV
E	20V/DIV	50 μSEC/DIV
F	20V/DIV	50 μSEC/DIV
G	50V/DIV	50 μSEC/DIV
H	20V/DIV	50 μSEC/DIV

***Fig 10—Of particular interest in these waveforms of the Fig 9 circuit** is the pulse-width-modulated output (trace C).*

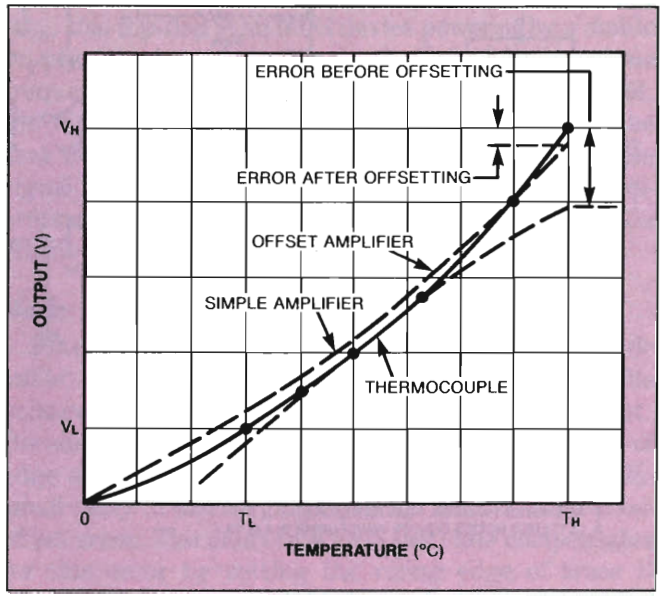


***Fig 11—By introducing an offset voltage and shifting the gain of a simple amplifier,** you obtain an output that more closely matches the thermocouple characteristic.*

Transistors Q_4 and Q_5 form a clocked, synchronous demodulator that pulls IC_8's R (reset) pin low only when the clock signal (the emitter of Q_1) is low; this condition occurs during data transfer but not during power transfer. The demodulated output (trace H) contains a single negative spike that resets the flip-flop. Because this spike is synchronous with the high-to-low transition of trace E, IC_8's output-pulse duration (trace C) is proportional to the thermocouple temperature.

Four techniques linearize TC signal

Because a thermocouple's response to temperature is nonlinear, its signal-conditioning circuit produces a nonlinear signal. By linearizing this signal, however, you can simplify further signal processing in many applications. Offset addition, breakpoints, analog computation, and digital correction are four techniques useful for this purpose.

Offset-addition schemes rely on biasing the nonlinear "bow" with a constant term. The resulting output voltage is high at the low end and low at the high end, but errors between these two extremes are reduced (**Fig 11**): The compromise reduces overall error. This approach is suitable for applications in which nonlinearity is either slight over a wide range or great over a narrow range.

Type-S thermocouples are relatively nonlinear—they generate 6 μV/°C at 25°C and 11 μV/°C at 1000°C. **Fig 12** shows an offset-addition linearizing circuit for such a thermocouple. This circuit is similar to that of **Fig 2b,** except for the offset term derived from IC_2 and applied through R_4. IC_3 is a chopper-stabilized op amp, useful for minimizing drift. Circuit accuracy is ±3°C for the range of 800 to 1200°C. To calibrate the circuit, set V_T=0.0000V and trim R_5 so that V_{OUT}=1.669V. Then, set V_T=9.585V (T=1000°C) and trim R_2 so that V_{OUT}=9.998V.

The **Fig 13** circuit is an adaptation of a configuration **(Ref 1)** that uses breakpoints to change circuit gain as the input signal varies. This method requires that you scale the input and feedback resistors associated with amplifiers $IC_{4A\text{-}4D}$, IC_{3B}, and IC_{3D}. Current summation at IC_{3C}'s inverting input produces an output voltage that is linear with the thermocouple temperature. Different-value input resistors cause each of the amplifiers, IC_{3D}, IC_{4A}, IC_{4B}, and IC_{4C}, to begin contributing current at a

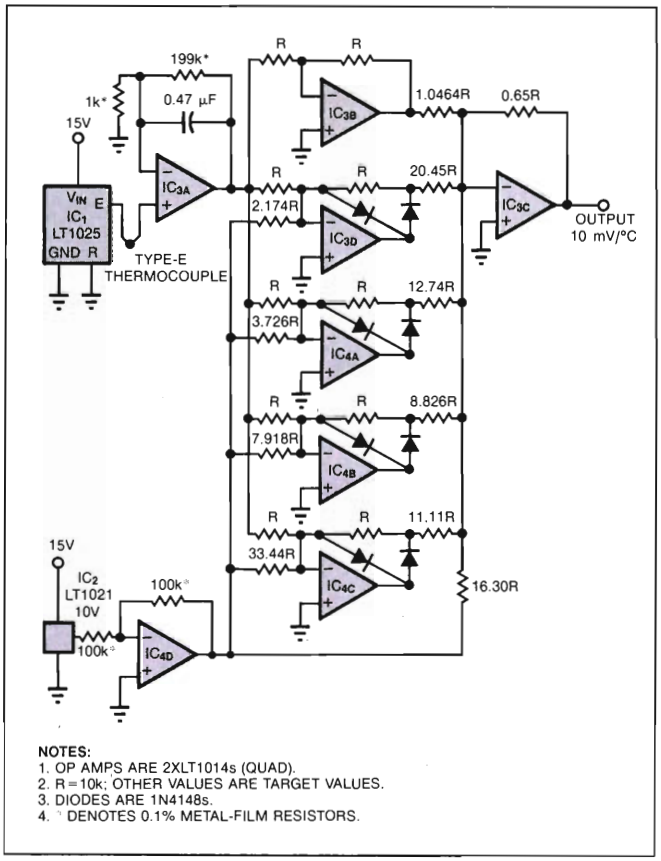


Fig 13—The thermocouple's output is linearized *thanks to the introduction of discrete breakpoints (amplifiers IC_{3D}, IC_{4A}, IC_{4B}, and IC_{4C}), which become active at different signal levels.*

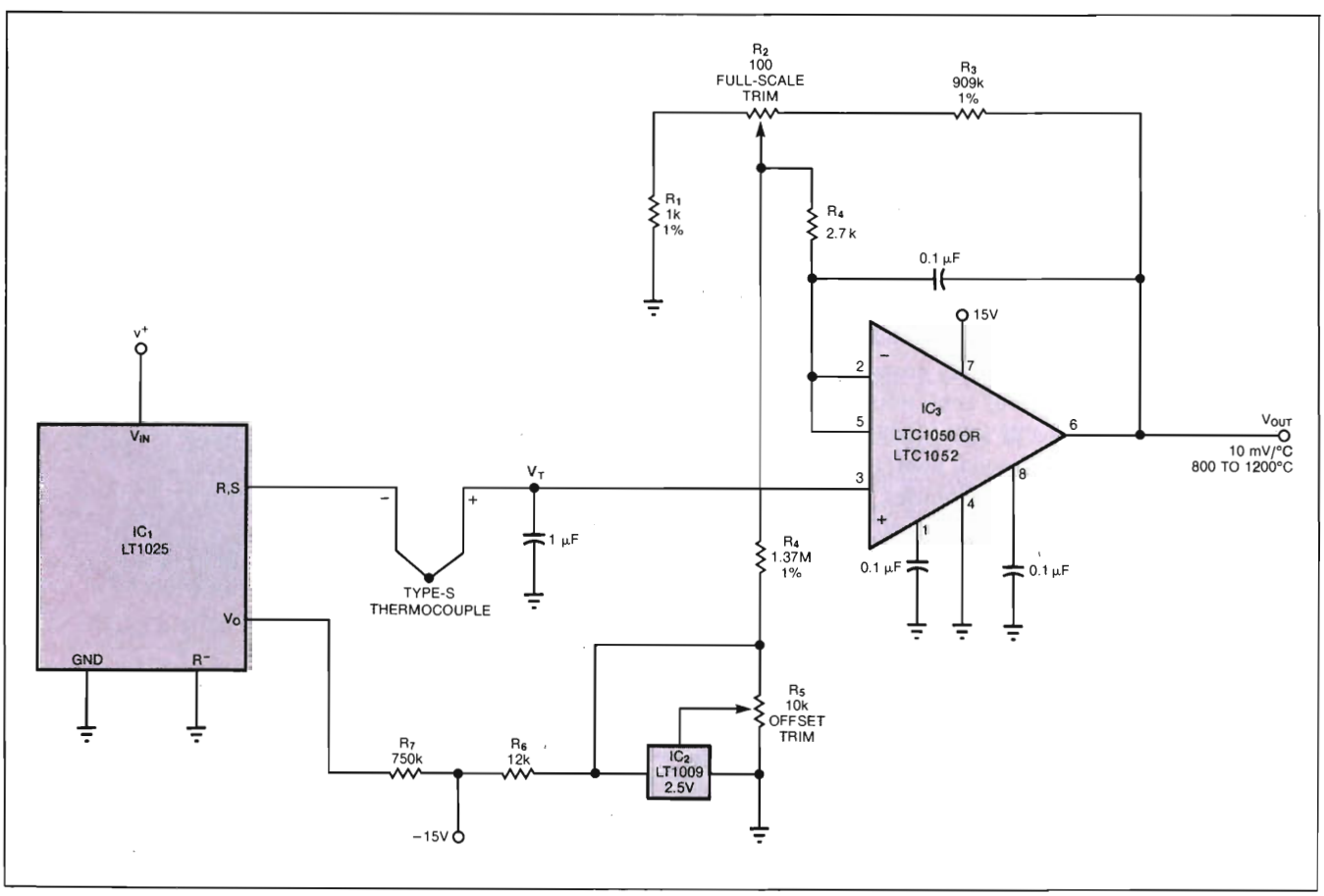


Fig 12—This circuit derives its offset term *from the 2.5V reference (IC_2) and uses it to help linearize the type-S thermocouple's output.*

Because they eliminate calibration trimming, digital techniques have become a popular method for linearizing thermocouple signals.

different level of input signal, and the switching diodes produce a piecewise-linear response from each amplifier. For the range of 0 to 650°C, typical circuit accuracy is ±1%.

Fig 14's circuit (**Ref 1**) replaces the breakpoints with continuous analog-computer functions, uses fewer amplifiers and resistors, and offers similar performance. The multifunction converter, IC_4, linearizes the response by combining a single breakpoint with appropriate scaling.

Implement breakpoints in software

Digital techniques have become popular for linearizing thermocouple signals because they eliminate calibration trimming. For instance, the **Fig 15** circuit—which Guy M Hoover of Linear Technology Corp developed—feeds a digitized thermocouple voltage to a μP that implements a large number of breakpoints in software. To use the circuit, you simply load the software and apply power; the μP then linearizes the digitized thermocouple signal and stores the result. *(Ed Note: The listing that provides all the necessary code for this application is available by sending a self-addressed, stamped envelope ($0.39 postage) to Software Listings Editor, EDN, 275 Washington St, Newton, MA 02158).*

IC_4 is a 10-bit A/D converter that gives 0.5°C resolution over the 0 to 500°C range. IC_2 amplifies and filters the thermocouple signal; IC_1 provides cold-junction compensation; and IC_3 provides an accurate reference voltage. (To maintain accuracy, the reference requires a minimum 6.5V supply; the A/D converter monitors this voltage via the R_1-R_2 divider.) The 1024-step resolution that IC_4 provides (24 more than the required 1000) ensures 0.5°C of temperature resolution, even for the nonlinear thermocouple characteristic. Linear interpolation between temperature-data points spaced 30°C apart, for example, introduces less than 0.1°C of error.

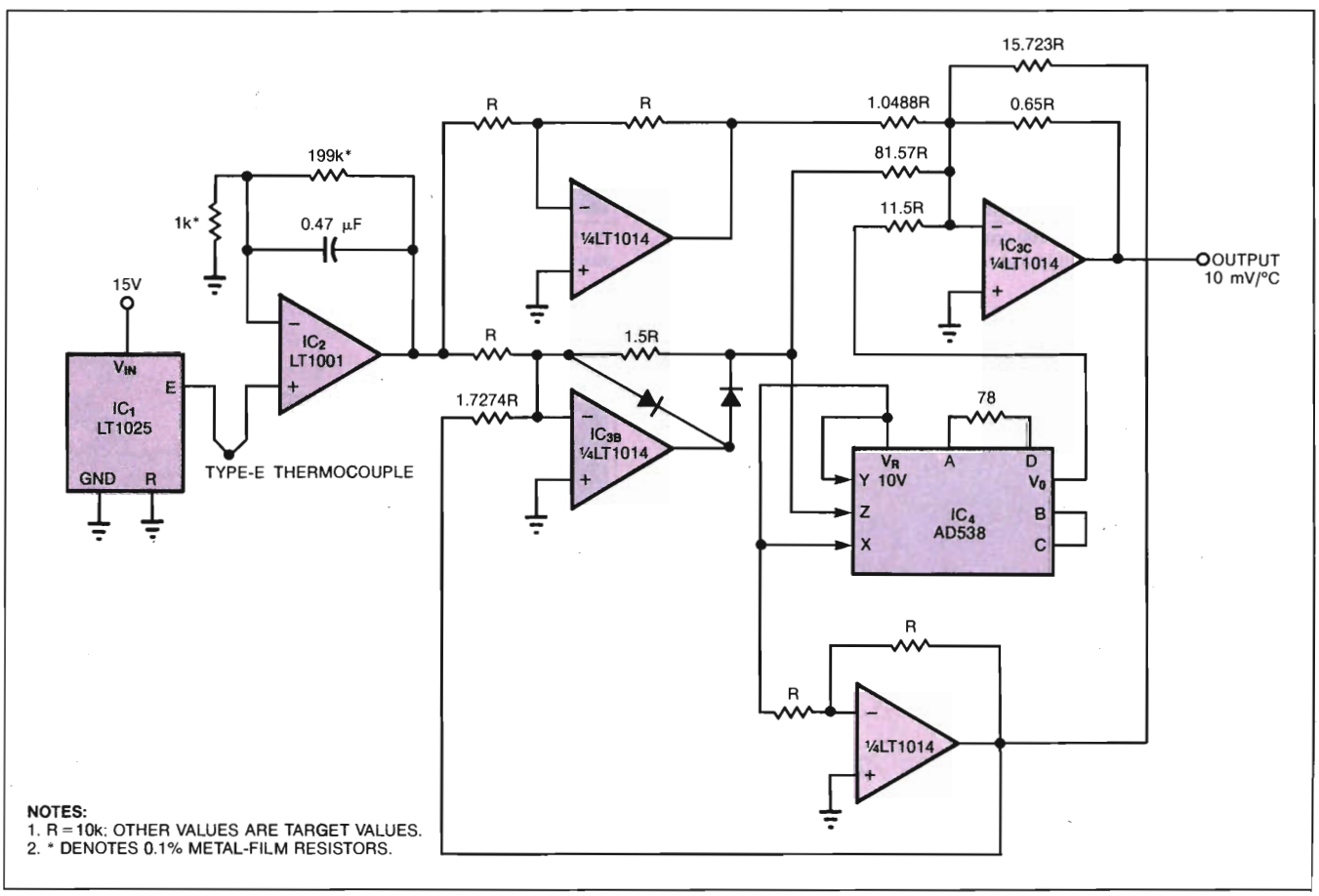


Fig 14—Offering performance comparable to that of Fig 13, *this linearizing circuit uses analog-computer functions in place of breakpoints.*

Eddy currents and the effects of laminar flow around a thermocouple can cause remarkably large measurement errors.

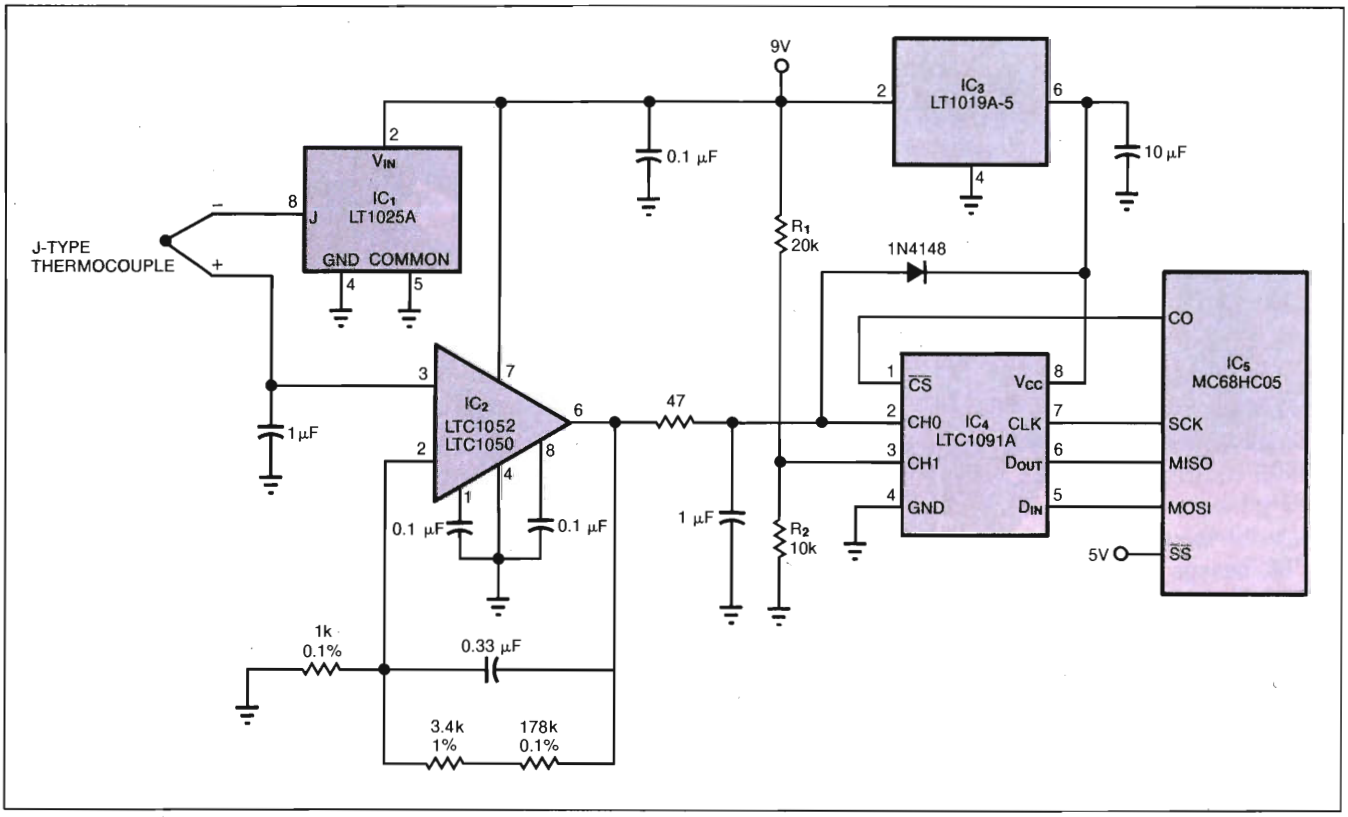


Fig 15—By introducing a microcomputer (IC_5) to implement breakpoints in software, *this thermocouple-linearizing circuit eliminates calibration trimming. The software listing is available from EDN; see text for details.*

The cold-junction compensator, IC_1, dominates the offset-error budget by contributing errors as high as 0.5°C. (IC_4's 5-µV offset contributes no more than 0.1°C.) The gain error is 0.75°C max, due primarily to the use of gain resistors with 0.1% tolerance values. IC_3's output-voltage tolerance and IC_4's gain error also contribute to the overall gain error; you can reduce this figure by trimming IC_3's gain resistors. The A/D converter maintains a linearity error below 0.15°C. Typically, these errors combine to produce an overall value of 0.5°C or less, exclusive of the thermocouple itself. Additional wire-connection errors of 0.5 to 1.0°C are not uncommon in practice, but with care you can keep these errors below 0.5°C. **EDN**

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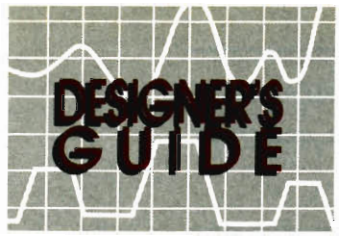
5. *Manual on the use of thermocouples in temperature measurement*, ASTM special publication #470A, American Society for Testing of Materials, Philadelphia, PA, 1974.

Author's biography

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art, and collecting antique scientific instruments.

Article Interest Quotient (Circle One)
High 488 Medium 489 Low 490



dc/dc converters
Part 1

Precise converter designs enhance system performance

DC/DC converters find application in a wide range of systems, from battery-driven circuitry to ac-line-powered systems. This article, part 1 of a 4-part series, demonstrates the design of the ubiquitous 5- to ±15V dc/dc converter. Parts 2 through 4, respectively, will show how to use instrumentation to design micropower quiescent-current converters, how to design dc/dc converters for power conservation, and how to replace inductors with switched-capacitor approaches in dc/dc-converter designs.

Jim Williams and Brian Huffman,
Linear Technology Corp

When evaluating dc/dc converters, designers often place far too much emphasis on efficiency and size. Although these parameters are significant, they are often of secondary importance. Other system-oriented requirements—low quiescent current, wide allowable-input ranges, reduced wideband output noise, and cost effectiveness—are more urgent. With the procedures presented here, you can design cost-effective 5 to ±15V dc/dc converters that have low current drain and low noise.

The case for 5 to ±15V converters

Logic supplies (5V outputs) have been popular since the introduction of diode transistor logic (DTL) over 20 years ago. Preceding, and during, DTL's infancy, modular-amplifier manufacturers made ±15V rails standard. Following tradition, early monolithic amplifiers also ran from ±15V rails. The 5V supply offers process, speed, and density advantages for digital ICs; the ±15V rails provide a wide signal-processing range for the analog components. Because of these divergent needs, 5 and ±15V supplies have also become standard for mixed digital-analog systems.

In systems with large analog-component populations, the ±15V supply was, and still is, usually derived from the ac line. This scheme, however, is definitely undesirable in predominantly digital systems. The inconvenience, difficulty, and cost of distributing analog rails in such systems makes local power generation attractive. The 5 to ±15V dc/dc converter fills this need.

Fig 1a is a conceptual schematic of a typical converter. The 5V input provides the source for a self-oscillating configuration made up of transistors, a transformer, and a biasing network. The transistors conduct out of phase, switching each time the transformer saturates. The transformer saturation develops a fast, high-current spike at the transformer's base-drive winding, which switches the transistors. The transformer current drops abruptly and then rises slowly until saturation again forces the transistors to switch. This alternating operating sets the transformer's duty cycle at 50%. The transformer's secondary signal is rectified, filtered, and regulated to produce the ±15V outputs.

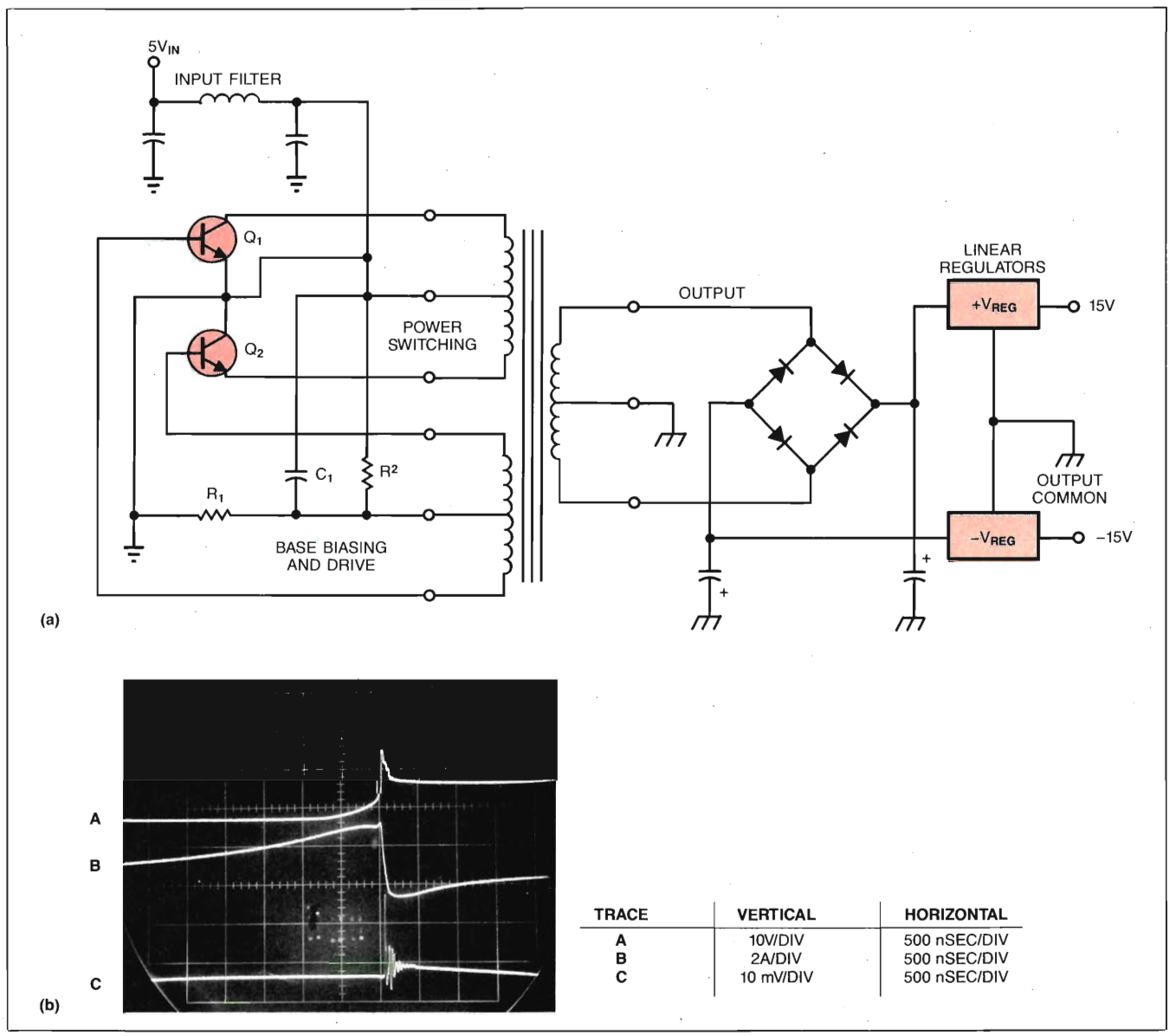
This configuration has a number of desirable features. The complementary, high-frequency (typically 20 kHz) square-wave drive makes efficient use of the

In systems that are heavily populated with digital circuitry, it makes sense to generate ±15V for analog circuits locally.

transformer and reduces the size of the filter capacitors. The self-oscillating primary drive tends to collapse under overload, providing desirable short-circuit characteristics. The transistors switch in a saturated mode, improving efficiency.

This scheme of hard switching, in combination with deliberate transformer saturation, does have one drawback, however. The significant, high-frequency current spike developed during the saturation interval develops noise at the converter outputs. The spike also draws significant current from the 5V supply—a minor disturbance, because the converters' input filter partially smooths the transient, and because 5V supplies are typically noisy anyway. The noise spikes at the output (typically 20 mV high) are a more serious problem. **Fig 1b** clearly shows the relationship among the transformer current (trace B), the transistor collector current (trace A), and the output spike (trace C).

As the transformer current rises, the transistor begins to come out of saturation. When the current



TRACE	VERTICAL	HORIZONTAL
A	10V/DIV	500 nSEC/DIV
B	2A/DIV	500 nSEC/DIV
C	10 mV/DIV	500 nSEC/DIV

Fig 1—Although its efficiency and short-circuit characteristics are good, *this converter* ***(a)*** *suffers from poor noise performance. The waveforms* ***(b)*** *show that a current spike (trace C) generated during the switching sequence is the problem source.*

reaches a high enough level, the circuit switches and generates the characteristic noise spike. The second transistor's concurrent switching complicates the problem, causing both ends of the transformer to conduct current to ground. You can use certain design techniques, including the proper selection of transistors and output filters, to reduce spike amplitude, but this converter's output is inherently noisy.

Spike-related noise troubles analog systems

Such noisy operation can cause difficulties in precision analog systems. IC power-supply rejection at the high-harmonic spike frequency is low, and it frequently causes analog-system errors. A 12-bit successive-approximation A/D converter is a good candidate for spike-related noise problems. Sampled-data ICs (such as switched-capacitor filters and chopper amplifiers) often show apparent errors that are induced by spikes. Even simple dc circuits can exhibit baffling instabilities that are actually spike-related problems masquerading as dc shifts.

The drive scheme creates another problem—high quiescent-current consumption. Base biasing always supplies full drive, ensuring that the transistors will saturate under heavy loads, but wasting power at lighter loads. Adaptive bias schemes can minimize this problem, but they increase circuit complexity, and this type of converter rarely employs them.

The noise problem is the main drawback in this approach to 5 to ±15V conversion. Careful design techniques can minimize the converters' noise problem, but they can't eliminate it. One technique (**Fig 2**), for example, uses a bracket pulse to warn the host system when a noise spike is about to occur. The host system ceases any noise-sensitive operations during the bracket-pulse interval. The bracket pulse drives a delayed-pulse generator, which triggers the flip-flop. The flip-flop's output biases the switching transistors in such a way that the noise spike occurs during the bracket-pulse interval. Clocked operation can also prevent transformer saturation, thereby reducing noise even further. This scheme works well, but presumes that the host can tolerate periodic intervals of inactivity when it is performing critical operations.

Low noise is important for analog circuits

The converter in **Fig 3** supplies a ±15V output from a 5V input. Its wideband noise measures 200 μV p-p—a 100% reduction over that of typical designs—and its efficiency for a 250-mA output equals 60%. The circuit achieves its low-noise performance by minimizing high-speed harmonic content in the power-switching stage. This result requires that you make the tradeoff in efficiency noted earlier, but the penalty is small in comparison with the benefit.

The 74C74 flip-flop divides the 74C14-based, 30-kHz oscillator into a 15-kHz, 2-phase clock. The 74C02 gates and the 10k/0.001-μF delay networks condition this 2-phase clock into a nonoverlapping, 2-phase drive at the emitters of Q_1 and Q_2 (traces A and B, respectively, in **Fig 3b**). These transistors act as level shifters to drive emitter followers Q_3 and Q_4. The 100Ω/0.003-μF filters loading the emitters of Q_3 and Q_4 slow the drive to output MOSFETs Q_5 and Q_6. The filter's effects appear at the gates of Q_5 and Q_6 (traces C and D, respectively).

Q_5 and Q_6 are configured as source followers. Therefore, the gate terminal's filtered slew rate limits the transformer's rise time, resulting in well-controlled waveforms at the sources of Q_5 and Q_6 (traces E and F, respectively.) The complementary, slew-limited drive source for T_1 eliminates the high-speed harmonics normally associated with this type of converter. After rectification, filtering, and regulation, T_1's output be-

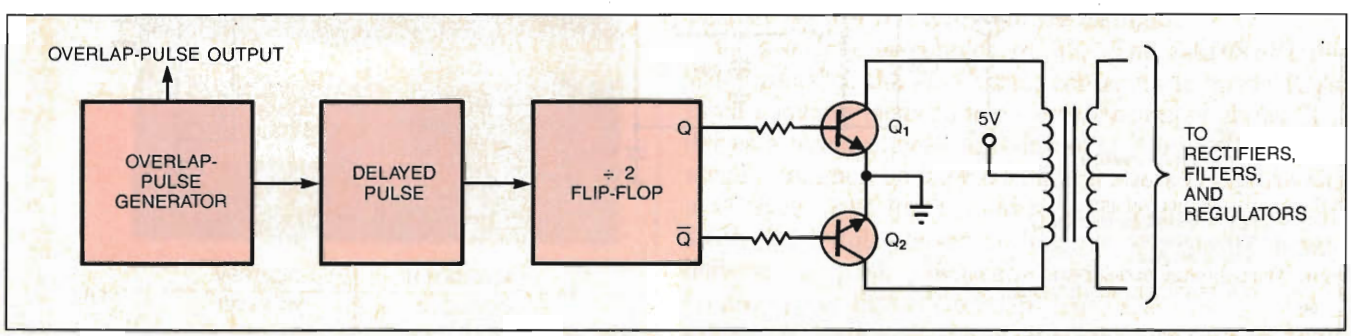


Fig 2—By sending an overlap pulse to indicate an impending noise pulse, *this circuit allows the system being powered to stop any critical operations, avoiding converter noise-related problems.*

Quiescent current, allowable input range, wideband output noise, and cost are important issues in converter design.

comes the converter's final output. The 470Ω/0.001-μF damper in T_1's secondary winding maintains loading during switching to enhance low-noise performance. The ferrite beads in the gate leads of Q_5 and Q_6 eliminate the parasitic RF oscillations associated with follower configurations.

The source-follower configuration makes it easy to control T_1's edge rise times, but complicates gate biasing. You'll require special design steps to turn the MOSFETs fully on and off. Source followers Q_5 and Q_6 require voltage overdrive at the gates, because the 5V primary supply can't provide the 10V gate-channel bias necessary for saturation. Similarly, you must pull the gates well below ground to turn the MOSFETs off, because T_1's behavior pulls the sources negative when the devices turn off.

The negative side of Q_6's source waveform provides turn-off bias. Q_3 and Q_4 pull down to the −4V level developed by D_1 and the 22-μF capacitor. A 2-stage boost loop generates the turn-on bias. The 5V supply feeds to the LT1054 switched-capacitor voltage converter via D_3. The LT1054, configured as a voltage doubler, initially provides about a 9V boost to point A at turn-on. When the converter begins operating,

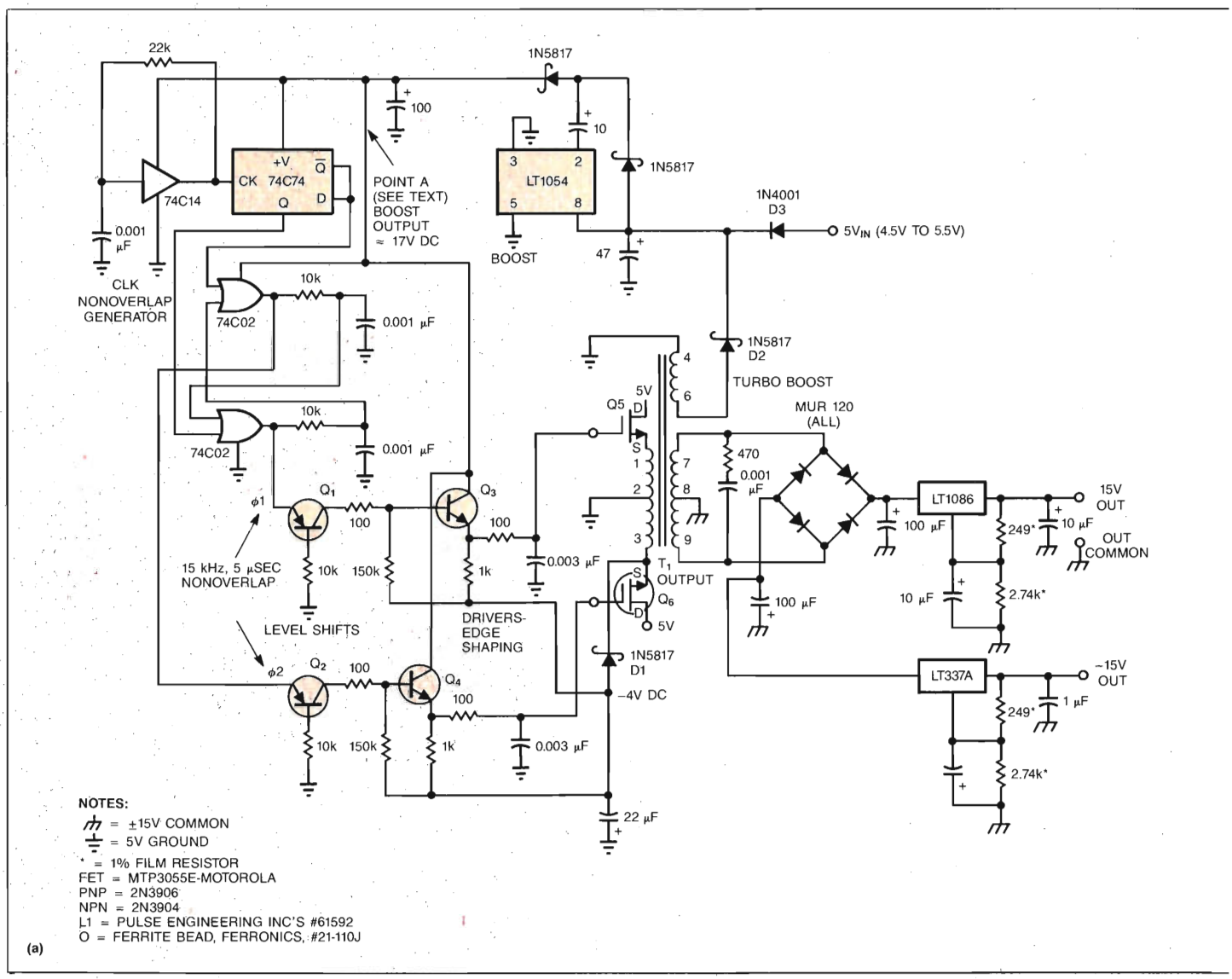
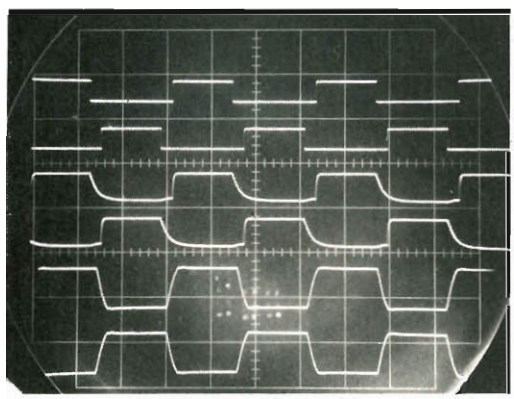


Fig 3—By minimizing high-speed harmonic content in the power-switching stage, *this converter design* ***(a)*** *achieves a 100× reduction in wideband output noise. As the waveforms* ***(b)*** *show, all the switching transitions are clean. The output noise* ***(c)*** *is only 200 μV p-p.*

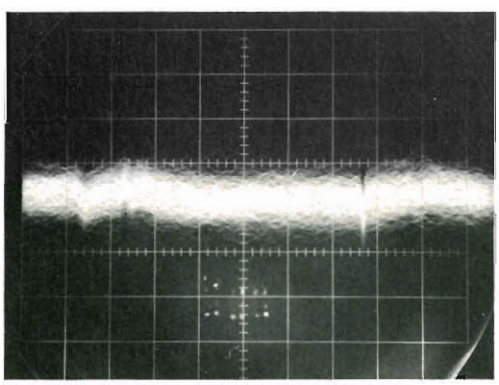
T_1 produces a turbo-boost output at pins 4 and 6. D_2 rectifies this output, which raises the LT1054's input voltage and further increases the boost at point A to approximately 17V.

These internally generated voltages allow Q_5 and Q_6 to receive the proper drive, minimizing losses despite the source-follower connection. An ac-coupled trace of the converter's 15V output (**Fig 3c**) shows 200-μV p-p noise at full power (250-mA output). The converter's switching characteristics compare in amplitude to the noise characteristics of linear regulators. You can reduce switching-related noise even further by slowing the rise times of Q_5 and Q_6. To slow the rise times, however, you must reduce the clock rate and increase nonoverlap time to maintain available power and efficiency. The arrangement shown in **Fig 3** represents a favorable compromise among output noise, available power output, and efficiency.



(b)

TRACE	VERTICAL	HORIZONTAL
A	20V/DIV	20 μSEC/DIV
B	20V/DIV	20 μSEC/DIV
C	20V/DIV	20 μSEC/DIV
D	20V/DIV	20 μSEC/DIV
E	10V/DIV	20 μSEC/DIV
F	10V/DIV	20 μSEC/DIV



(c)

VERTICAL	HORIZONTAL
100 μV/DIV	5 μSEC/DIV

Satisfy high-resolution circuits' needs

Residual switching components and regulator noise set the performance limits for the converter in **Fig 3.** Analog circuitry operating at the very highest resolution and sensitivity levels may require a converter with even less noise. **Fig 4's** converter uses a sine-wave transformer drive to reduce harmonics to negligible levels. The transformer drive combines with special output regulators to produce less than 30 μV of output noise. This value is also seven times lower than that of the previous circuit, and, in comparison with conventional designs, it approaches a 1000× improvement. If you use this circuit, you'll have to make a couple of tradeoffs, however: In comparison with **Fig 3**'s circuit, **Fig 4**'s circuit will be more complex and will sacrifice some efficiency.

IC_1 of **Fig 4** is configured as a 16-kHz Wien-bridge oscillator. The design uses a special bias level to prevent IC_1's output from saturating at the ground rail. Returning the undriven end of the Wien network to a dc potential derived from the LT1009 reference establishes this bias. IC_1's output is a pure sine wave (trace A in **Fig 4b**) biased off ground. To maintain the sine-wave output, IC_2 compares IC_1's rectified and filtered positive output peaks with an LT1009-derived dc reference. IC_2's output biases IC_1 and servocontrols its gain. The 0.22-μF capacitor provides temperature compensation for the loop, and the thermally mated diodes minimize errors caused by rectifier temperature drift. These provisions stabilize IC_1's ac and dc output terms against supply and temperature changes.

IC_1's output ac-couples to IC_3. The 2-kΩ/820Ω divider rebiases the sine wave, centering it inside IC_3's input common-mode range even with supply shifts. IC_3 drives a power stage consisting of Q_2 through Q_5. This stage's common emitter outputs are biased to provide a 1V rms drive for T_3—even for a supply voltage of 4.5V. With full converter loading, the power stage delivers 3A peaks, but the waveform is clean (trace B) and shows little distortion (trace C).

The 330-μF coupling capacitor strips dc voltage from the power-stage output, so T_3 has a pure ac input. The Q_4 and Q_5 collectors provide a feedback signal for IC_3.

Analog circuitry operating at very high levels of resolution and sensitivity may require the lowest possible converter-noise levels.

The 0.1-μF capacitor at the feedback source point suppresses local oscillations, and the RC network in T_3's secondary winding adds additional high-frequency damping.

Without quiescent-current control, the power stage will experience thermal runaway and destroy itself. IC_4 measures the dc output current across Q_5's emitter resistor and servocontrols Q_6 to establish quiescent current. A divided portion of the LT1009 reference sets the servo point at IC_4's negative input, and the 0.33-μF feedback capacitor stabilizes the loop.

T_3's rectified and filtered outputs drive regulators designed for low-noise operation. IC_5 and IC_7 amplify the LT1021's filtered 10V output to 15V, and IC_6 and IC_8 provide the −15V output. The LT1021/amplifier combination provides better noise performance than do 3-terminal regulators. The zener diode eliminates overvoltages caused by start-up transients. L_1 and L_2 combine with their respective output capacitors to minimize noise problems. These inductors are outside the feedback loop, but their low copper resistance doesn't significantly degrade regulation. Trace D, the 15V output at full load, shows less than 30 μV (2 ppm) of noise. The most significant tradeoff in this design is efficiency. The sine-wave transformer drive exacts a substantial power loss. At full output (75 mA), the

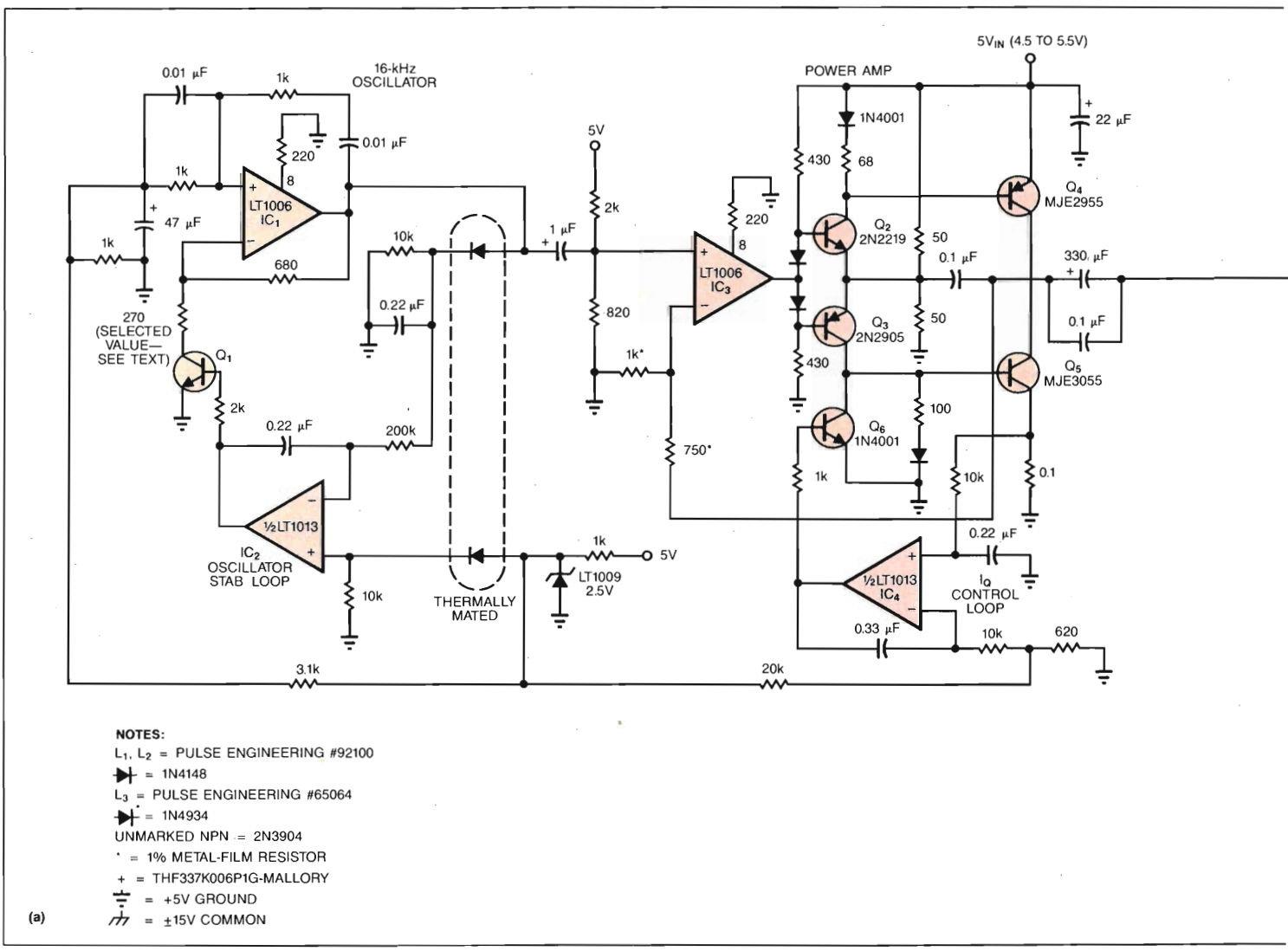


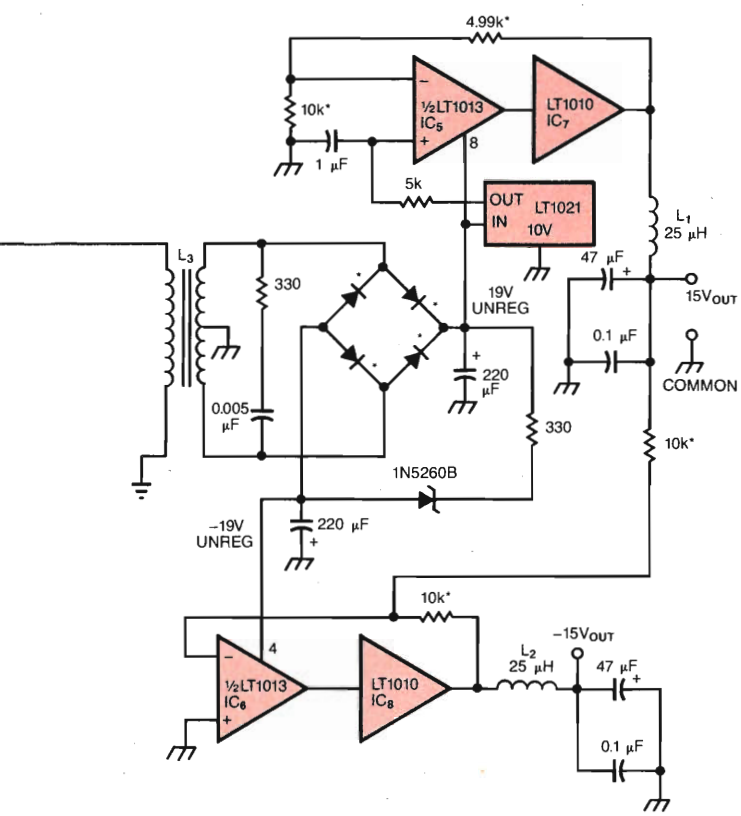
***Fig 4—To improve noise performance by 1000×** over that of conventional designs, this converter **(a)** uses sine-wave transformer drive to reduce harmonics to negligible levels. As the waveforms show **(b)**, the 15V output (trace D) has less than 30 μV of noise at full load.*

efficiency is only 30%.

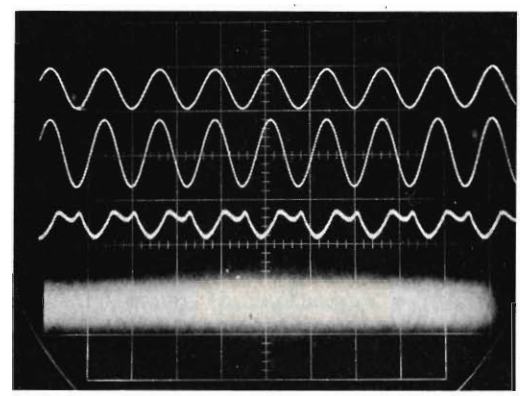
Before operating the converter, you should trim the circuit for lowest distortion (typically 1%) in the sine wave at the input of T_3. You can perform this trimming by selecting the resistance value indicated at IC_1's negative input. The 270Ω value shown is nominal and can vary by ±25%. The sine wave's 16-kHz frequency represents a compromise between the op amp's available gain/bandwidth, magnetics size, audible noise, and wideband harmonic levels.

Simplicity and economy are other important considerations in 5 to ±15V converter designs. In these converters, the transformer is usually the most expensive component. The unusual drive scheme in **Fig 5**'s converter leads to significant cost savings—it uses a simple 2-terminal inductor in place of the usual transformer. The design tradeoffs are the loss of input-to-output galvanic isolation and lower power output. In addition, this circuit's isolation technique develops about 50 mV of clock-related output ripple.

Fig 5's circuit operates by periodically and alternately allowing each end of the inductor to fly back. The resulting positive and negative peaks are rectified and filtered. Controlling the number of flyback events during the respective output's flyback interval regulates the converter.



(b)



TRACE	VERTICAL	HORIZONTAL
A	2V/DIV	50 µSEC/DIV
B	2V/DIV	50 µSEC/DIV
C	1% DISTORTION	50 µSEC/DIV
D	20 µV/DIV	50 µSEC/DIV

Simplicity and economy are important converter-design goals; you can achieve both by using a simple inductor to replace the transformer.

Inverter IC_{2A} develops a 20-kHz clock signal (trace A in **Fig 5b**), which feeds a logic network composed of additional inverters, diodes, and the 74C90 decade counter. The counter output (trace B) combines with the logic network to present alternately phased clock bursts (traces C and D) to the base resistors of Q_1 and Q_2. When ϕ_1 (trace B) is inactive, it resides in its high state, and it biases Q_2 and Q_4 on. Q_4's collector effectively grounds the bottom of L_1 (trace H). During this interval, ϕ_2 (trace A) sends clock bursts into Q_1's base resistor. If the -15V output is too low, servocomparator IC_{1A}'s output (trace E) is high and Q_1's base can receive pulsed bias current.

If the converse is true, the comparator's output will be low and will gate the bias away through Q_1's base diode. When Q_1 is open to a bias input, Q_3 switches and produces a negative-going flyback event at the top of L_1 (trace G). The flyback event is rectified and filtered to develop the -15V output. IC_{1A} regulates the number of clock pulses that switch the Q_1/Q_3 pair. The LT1004 serves as a reference.

The ac-coupled -15V output (trace J) shows the effect of IC_{1A}'s regulating action. The output stays within a small error window set by IC_{1A}'s switched control loop. As input-voltage and loading conditions change, IC_{1A} adjusts the number of permissible clock pulses to bias Q_1/Q_3 and maintain loop control.

When the ϕ_1 and ϕ_2 signals reverse state, the operational sequence reverses. Q_3's collector (trace G) pulls high, and IC_{1B}'s servo action controls Q_2/Q_4's switching

LT1070: The inside story

The LT1070 is a current-mode switcher whose duty cycle is controlled directly by switch current rather than output voltage (**Fig A**). The switch turns on at the start of each oscillator cycle and turns off when the switch current reaches a predetermined level. The output of a voltage-sensing error amplifier sets the current trip level to control the output voltage.

This technique has several advantages. First, unlike ordinary switchers, which have notoriously poor line transient response, the LT1070 responds immediately to input-voltage vari-

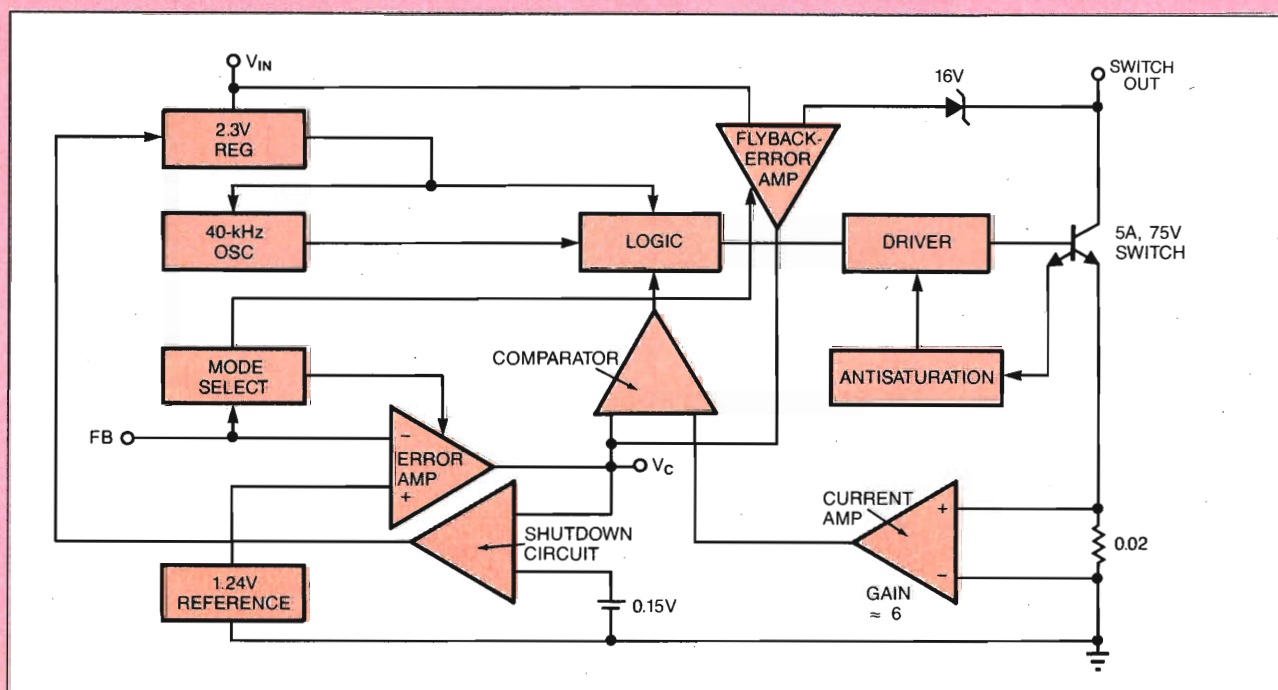


***Fig A—The LT1070 is a current-mode switcher** whose duty cycle is controlled directly by switch current rather than output voltage. Unlike ordinary switchers, which have notoriously poor line transient response, it responds to input-voltage variations immediately.*

to produce similar output waveforms. Traces F, H, and I illustrate IC_{1B}'s output, Q_4's collector signal (L_1's bottom), and the ac-coupled 15V output, respectively.

Although the two regulating loops share the same inductor, they operate independently, so no performance degradation is caused by asymmetrical output loading. The inductor sees irregularly spaced shots of current (trace K), but is unaffected by this multiplexed operation. Clamp diodes prevent Q_3 and Q_4 from reverse-biasing during transient conditions. The circuit provides ±25 mA of regulated current at 60% efficiency.

Reduced quiescent current is another aspect of 5 to ±15V converter design. Typical coverters draw 100 to 150 mA of quiescent current—a value that's unacceptably high for many low-power systems. **Fig 6's** converter design supplies ±15V at 100-mA outputs while consuming only 10 mA of quiescent current. The LT1070 switching regulator (see **box,** "LT1070: The inside story") drives T_1 in a flyback mode; the damper network clamps excessive flyback voltages. Half-wave rectification and filtering of T_1's secondary signals produces positive and negative output across the 47-μF capacitors.

A simple loop regulates the positive 16V output. Comparator IC_{1A} balances a sample of the positive output with a 2.5V reference voltage from the LT1020. When the 16V output (trace A in **Fig 6b**) is too low, IC_{1A} switches high (trace B) and turns off the 4N46 optoisolator. Q_1 turns off, and the LT1070's control pin

ations. Second, the current-mode configuration reduces the 90° phase shift in the energy-storage inductor at middle frequencies. This reduction greatly simplifies closed-loop frequency-compensation tasks under widely varying input-voltage or output-load conditions. Finally, the current-mode technique can use simple pulse-by-pulse current limiting to provide maximum protection for the switch under output-overload or short-circuit conditions.

A low-dropout internal regulator provides a 2.3V supply voltage for all of the LT1070's internal circuitry. Because of this low-dropout design, input-voltage variations from 3 to 60V have virtually no effect on the LT1070's performance.

A 40-kHz oscillator serves as the basic clock for all the switcher's internal timing. The oscillator uses the logic and driver circuitry to turn on the output switch. Special adaptive circuitry monitors the output switch and instantaneously adjusts the driver current to limit switch saturation.

A 1.2V bandgap reference biases the error amplifier's positive input. The amplifier's negative input is available at a pin on the package, so you can use it for output-voltage sensing. This feedback pin has a second function: When it's pulled low by an external resistor, the pin programs the LT1070 to disconnect the main error-amplifier output and connects the flyback amplifier's output to the comparator input. The LT1070 then regulates the value of the flyback pulse with respect to the supply voltage.

This flyback pulse is directly proportional to the output voltage in the traditional transformer-coupled, flyback-topology regulator. By regulating the flyback pulse amplitude, you can regulate the regulator's output voltage with no need for a direct connection between the input and the output. The output is fully floating for values as high as the breakdown voltage of the transformer windings. A special delay network in the LT1070 improves output regulation by ignoring the leakage-inductance spike at the leading edge of the flyback pulse.

The error signal developed at the comparator input comes out to an LT1070 terminal. This V_C pin provides four different functions—frequency compensation, current-limiting adjustment, soft-starting, and total regulator shutdown. During normal regulator operation, the V_C pin sits at a voltage between 0.9V (low output current) and 2V (high output current). Since the error amplifiers are current-output types, you can clamp V_C externally to adjust the current limiting. A capacitor-coupled external clamp will provide a soft-start capability.

If you pull the V_C pin to ground through a diode, the switch duty cycle will go to zero and put the LT1070 in an idle mode. Pulling the V_C pin below 0.15V causes total regulator shutdown.

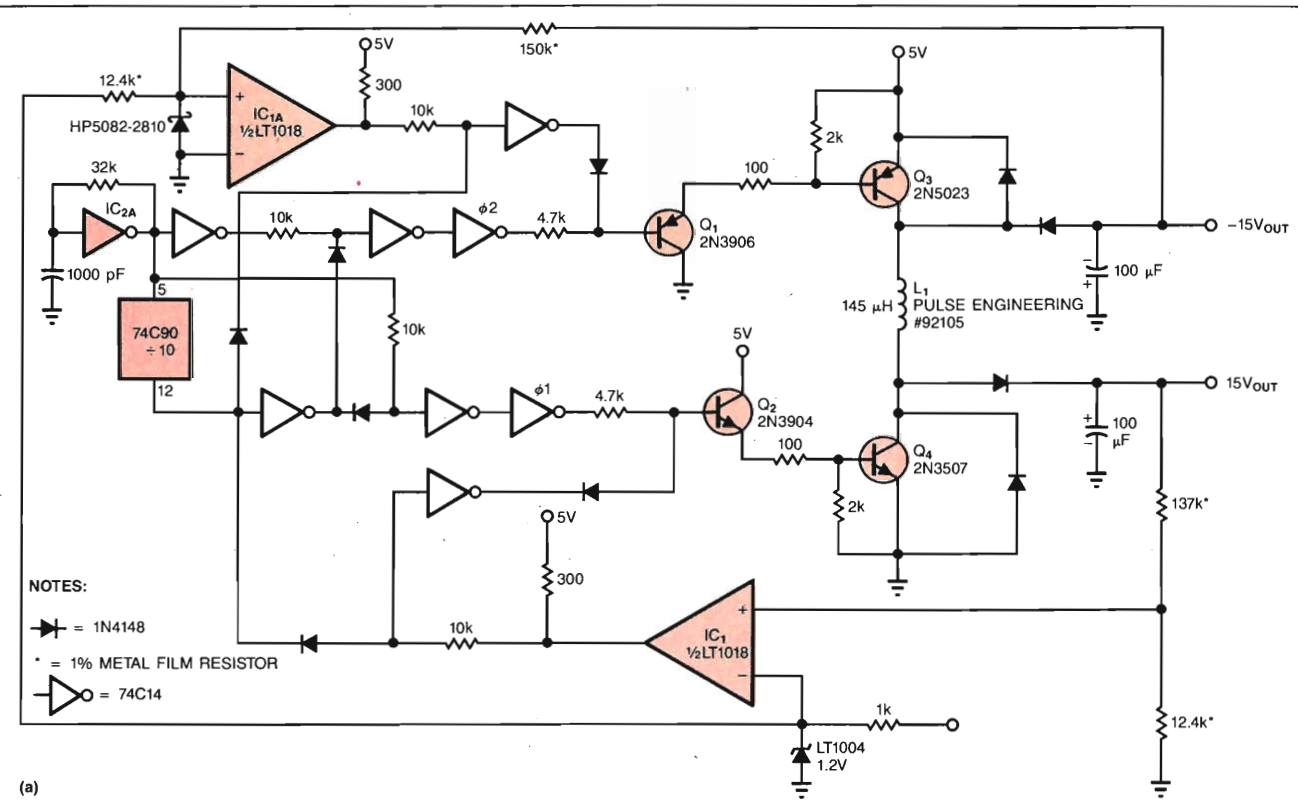


Fig 5—For circuit simplicity and economy, *the drive scheme in this converter* ***(a)*** *uses a 2-terminal inductor in place of the usual transformer. The waveforms* ***(b)*** *show that although the inductor sees irregularly spaced shots of current (trace K), the multiplexed operation has no effect on the inductor's performance.*

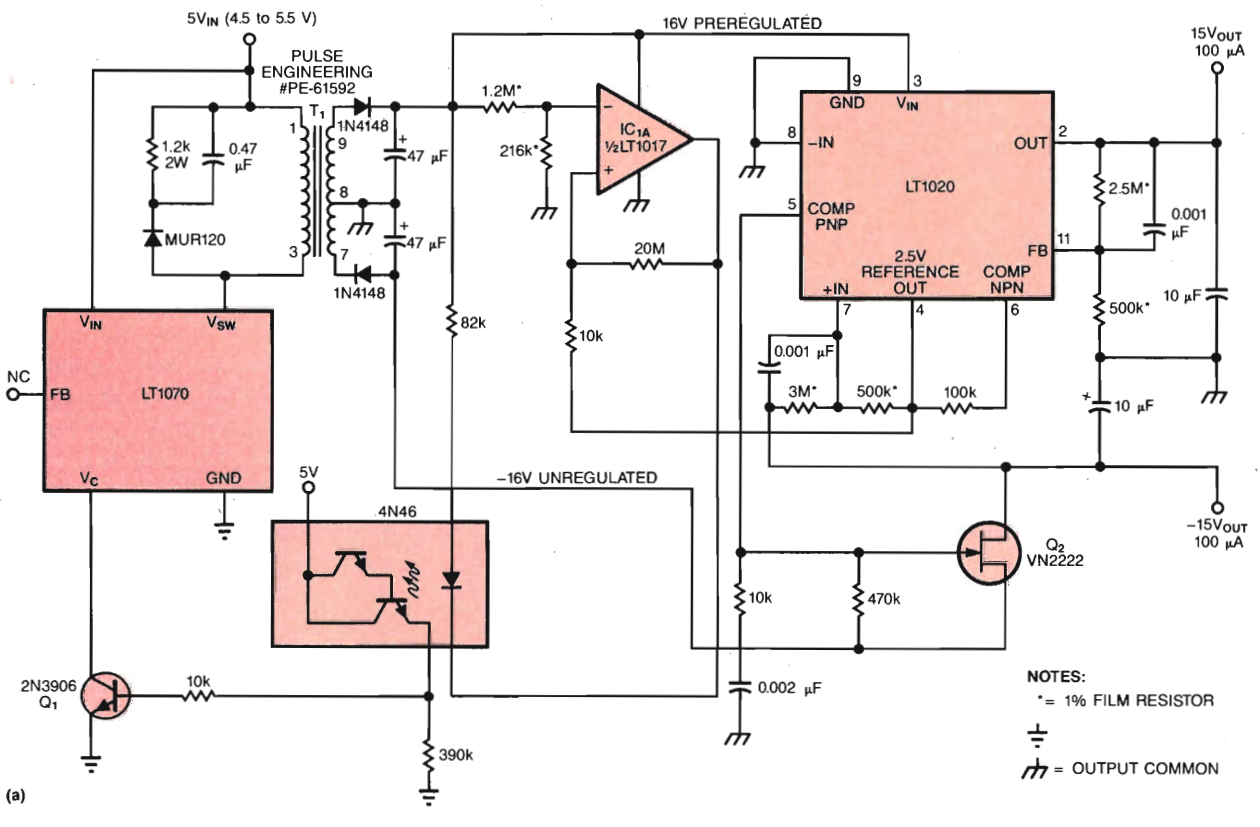
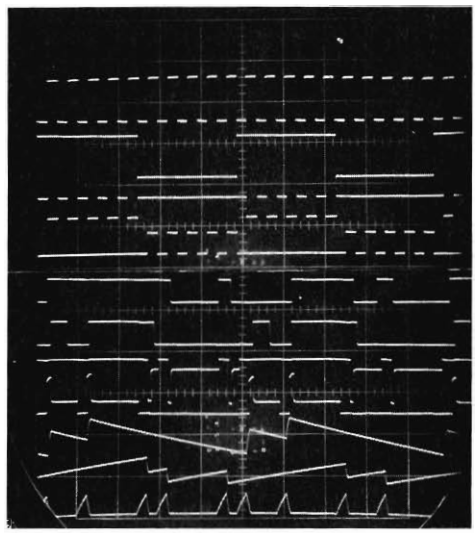
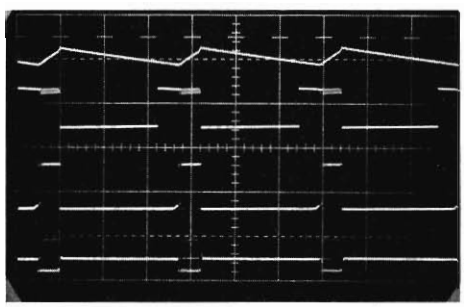


Fig 6—To satisfy the needs of many low-power systems, *this converter design* ***(a)*** *supplies ±15V outputs at 100 mA while consuming only 10 mA of quiescent current. As trace D of the scope photo* ***(b)*** *illustrates, the converter has a 40-kHz switching frequency. Compared to conventional designs, this converter's efficiency* ***(c)*** *is far superior at light loads.*



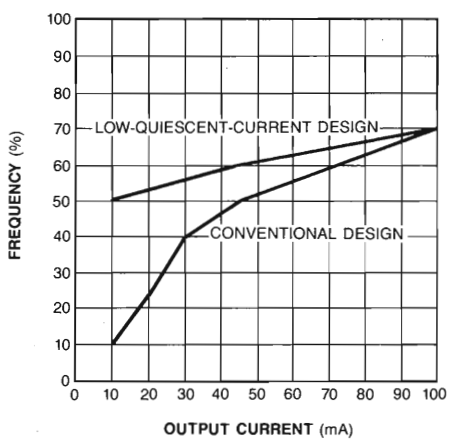
(b)

TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	100 μSEC/DIV
B	5V/DIV	100 μSEC/DIV
C	10V/DIV	100 μSEC/DIV
D	10V/DIV	100 μSEC/DIV
E	10V/DIV	100 μSEC/DIV
F	10V/DIV	100 μSEC/DIV
G	20V/DIV	100 μSEC/DIV
H	20V/DIV	100 μSEC/DIV
I	0.05V/DIV	100 μSEC/DIV
J	0.05V/DIV	100 μSEC/DIV
K	1A/DIV	100 μSEC/DIV



(b)

TRACE	VERTICAL	HORIZONTAL
A	100 mV/DIV	5 mSEC/DIV
B	20V/DIV	5 mSEC/DIV
C	2V/DIV	5 mSEC/DIV
D	20V/DIV	5 mSEC/DIV



(c)

(V_C) goes high (trace C). This action generates full-duty-cycle, 40-kHz switching at the V_{SW} pin (trace D). The resulting energy into T_1 forces the 16V output to ramp quickly positive and turn off IC_{1A}'s output. The 20-MΩ resistor, combined with the slow response of the 4N46 (note the delay between IC_{1A}'s going high and the V_C pin transition) provides about 40 mV of hysteresis.

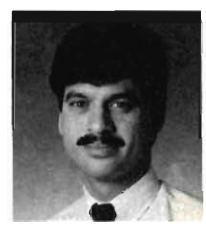
The LT1070's on/off duty cycle is load dependent, so it saves a significant amount of power when the converter operates with a light load. This characteristic is largely responsible for the 10-mA quiescent-current figure.

The optoisolator preserves the converter's input-to-output isolation. The LT1020, a low-quiescent-current regulator, further regulates the 16V line to develop the 15V output. This linear regulation eliminates the 40-mV ripple and improves transient response.

The −16V output tends to follow the regulated −16V line, but the regulation is poor. The RC damper at pin 5 allows the LT1020's auxiliary onboard comparator to function as an op amp. This op amp linearly regulates the −16V line. MOSFET Q_2 provides low-drop-current boost and sources the −15V output. The op amp stabilizes the −15V output by comparing it with the 2.5V reference via the 500k/3M summing resistors. The 1000-pF capacitors frequency-compensate each regulating loop. **Fig 6c** plots this converter's efficiency versus that of a conventional design for a range of loads. Although the results are similar for high loads, the low-quiescent-current circuit is superior at light loads. EDN

Authors' biographies

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art, and collecting antique scientific instruments.



Brian Huffman is an applications engineer at Linear Technology Corp. A member of the IEEE, he holds a BSET dgree from Indiana State University and an MSEE from Santa Clara University. In his spare time, Brian enjoys plays, concerts, and the beach, and he likes to travel.

Article Interest Quotient (Circle One)
High 491 Medium 492 Low 493

DESIGNER'S GUIDE

dc/dc converters
Part 2

Proper instrumentation eases low-power dc/dc-converter design

This article, part 2 of a 4-part series, provides tips on selecting the right instrumentation to evaluate the performance of your low-power 5, 12, and ±12V converter designs. Part 1 emphasized the design of low-noise 5 to ±15V converters; parts 3 and 4, respectively, will show how to design dc/dc converters for power conservation and how to replace inductors with switched-cap techniques in dc/dc converter designs.

Jim Williams and Brian Huffman,
Linear Technology Corp

Flexibility is the key parameter in selecting instrumentation for dc/dc-converter design. Although wide bandwidths, high resolution, and computational sophistication are valuable features, they're really unimportant in designing converters. Typically, converter design requires the simultaneous observation of a number of relatively slow circuit events. The instruments used in converter design must have such features as fully floating inputs, high sensitivity, differential dc nulling or slide-back plug-in capability, high-impedance probes, and versatile triggering/multitrace capability.

Consider probe impedance, for example. Standard 1× and 10× scope probes are fine for many measurements, but the ground strap can be a problem in some cases. Because wideband switching noise is present in dc/dc converters, you must use the shortest possible ground return when making low-level measurements.

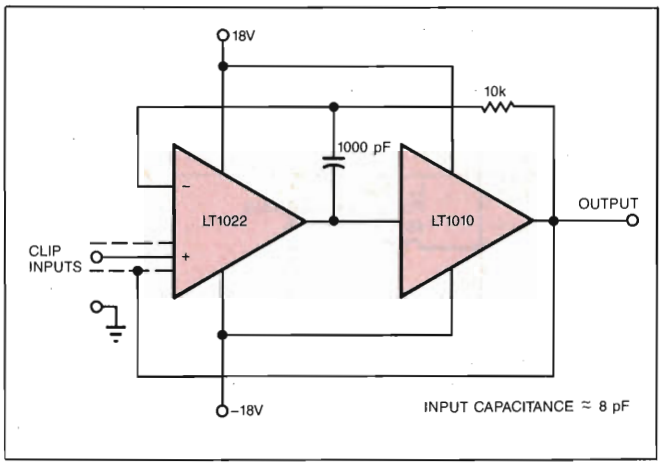


***Fig 1—You can solve a lot of loading problems** by using this simple probe, which employs an LT1022 high-speed FET op amp to drive an LT1010 buffer. The LT1010's output serves as a cable and probe drive source, and it also biases the circuit's input shield.*

It's important, therefore, to use a probe that can accommodate a variety of tip-grounding accessories.

You'll rarely require wideband, FET-type probes, but a moderate-speed, high-impedance buffer probe is quite useful. In many converter circuits (especially micropower designs), you'll have to monitor high-impedance nodes. Usually, the 10-MΩ loading of standard 10× probes will suffice, but when you use these standard probes, you have to trade away sensitivity. On the other hand, the sensitivity of 1× probes is adequate for most measurements, but these probes can create loading problems.

You'll rarely require wideband FET-type probes, but a moderate-speed, high-impedance buffer probe is useful.

The simple circuit in **Fig 1** solves probe-loading problems. The design's LT1022 high-speed FET op amp drives an LT1010 buffer. The LT1010's output serves as a cable and probe drive source and also biases the circuit's input shield. This biasing bootstraps the input capacitance and reduces its effect. The bandwidth as well as the ac and dc errors of this circuit are low enough for almost all converter work. If you build the circuit, along with its own power supply, into a small enclosure, you can use it as an input to an oscilloscope, with good results.

An isolated probe allows you to make fully floating measurements even in the presence of high common-mode voltages. Such a capability is very useful when you have to look across floating points in a circuit rather than make the usual ground-referenced measurements. This probe can be very valuable for directly observing an ungrounded transistor's saturation characteristics or for monitoring waveforms across a floating shunt.

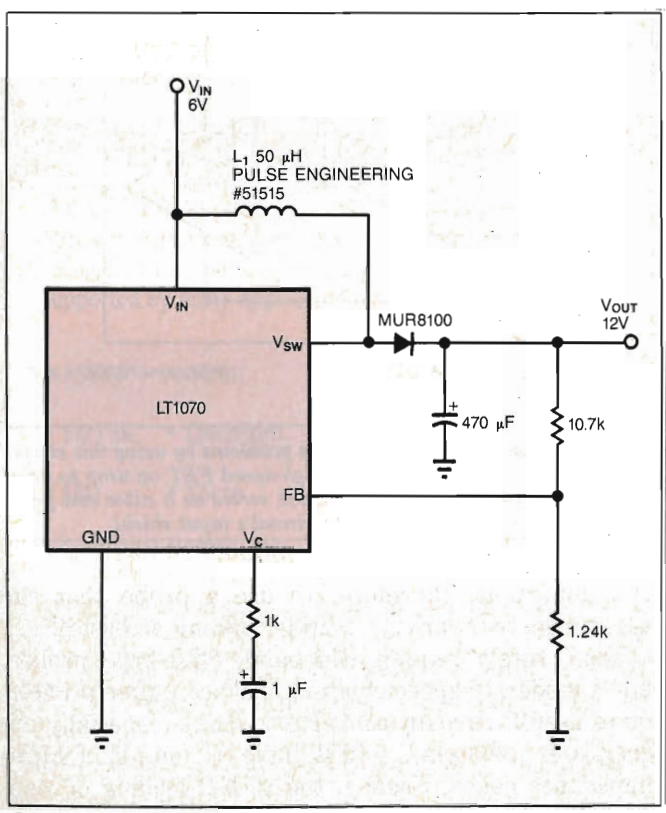


Fig 2—In this typical flyback-type converter, *the LT1070's internal 40-kHz clock produces a flyback event every 25 µsec. Each time the LT1070's V_{SW} pin internally switches to ground, it produces an inductive flyback voltage that converts the 6V battery input to a 12V output.*

Current probes are also an indispensable tool for converter design. In many cases, current waveforms contain more valuable information than do voltage waveforms. Clip-on current probes are convenient. Hall-effect-based versions respond as low as dc and feature 50-MHz bandwidth capability. Transformer-type current probes are faster, but they have rolloff below several hundred hertz. Both types have saturation limitations. If you exceed these limitations, you'll get some confusing displays on the CRT.

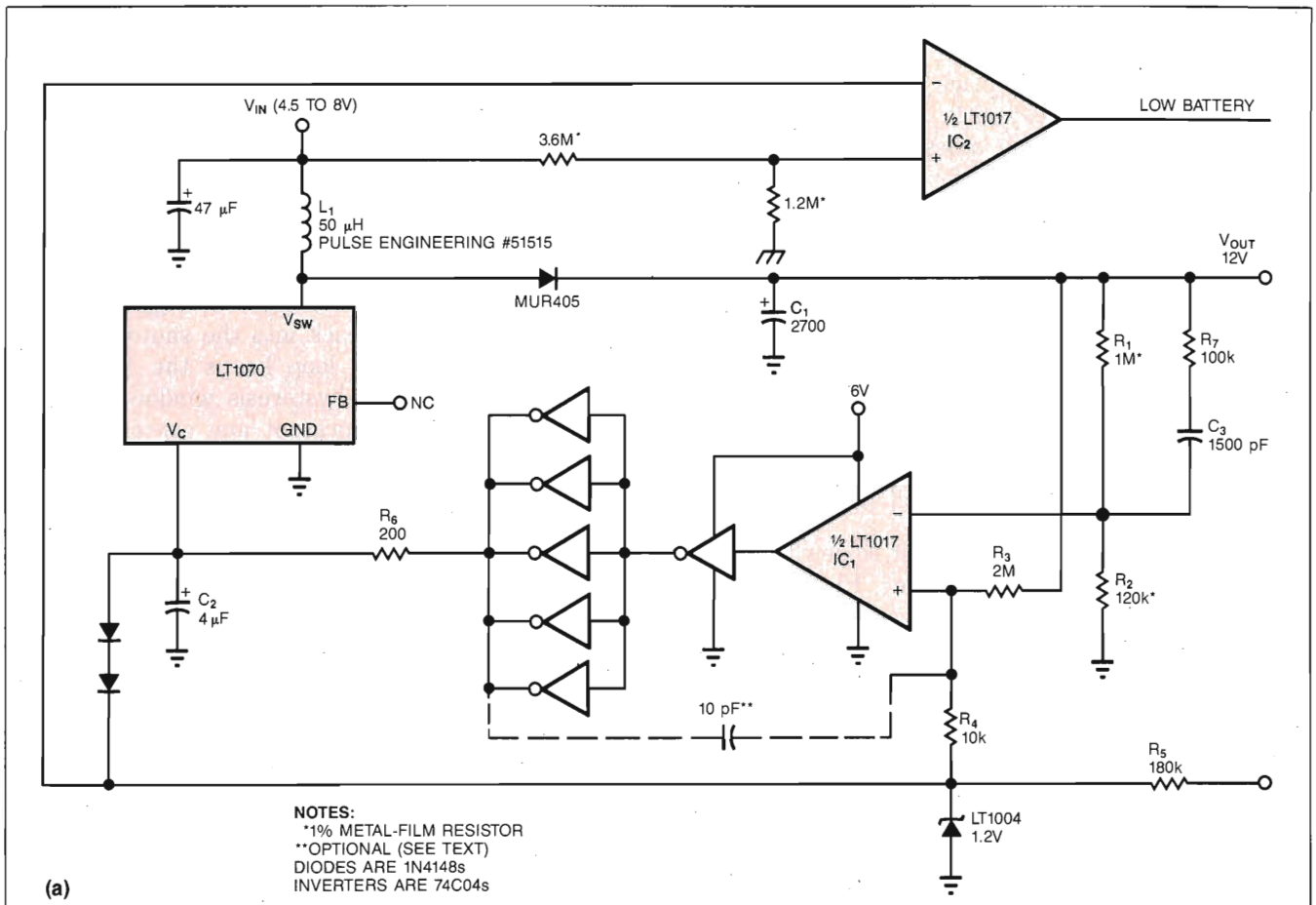
Consider using a nonelectronic voltmeter

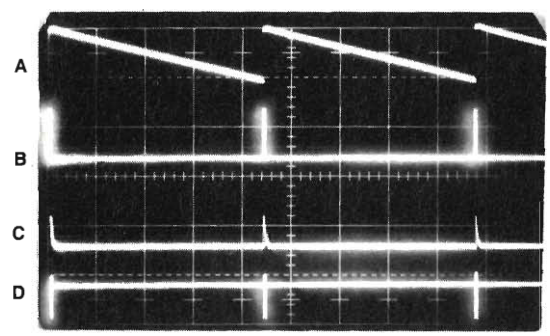
Almost any digital voltmeter will suffice for converter work. The meter should have current-measurement capability and provisions for battery operation. The instrument's capability to operate from battery power allows you to make floating measurements and eliminates possible ground-loop errors. In addition, a nonelectronic voltmeter (or volt-ohmmeter) is a worthwhile addition to the converter-design bench. Converter noise occasionally disturbs electronic voltmeters and produces erratic readings. A nonelectronic voltmeter contains no active circuitry, so it's less susceptible to noise-related problems.

Addressing the needs of portable applications

The power supply's current requirements can vary widely in many battery-powered applications. Although normal operation might require currents in the ampere range, supply-current drain might drop into the microampere range for systems that are in standby or sleep mode. A typical lap-top computer may draw 1 to 2A while running and require only a few hundred microamps for memory backup when not running. Theoretically, any dc/dc converter designed for loop stability under no-load conditions will work in this computer application. From the practical standpoint, however, a converter with a relatively large quiescent-current requirement may drain the battery excessively during intervals of low output current.

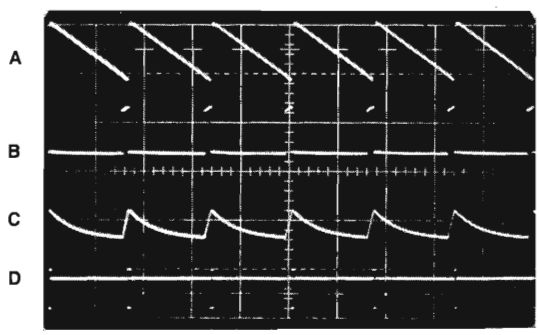
Fig 2 shows a typical flyback-type converter. Each time the LT1070's V_{SW} pin internally switches to ground, it produces an inductive flyback voltage that converts the 6V battery input to a 12V output. The LT1070's internal 40-kHz clock produces a flyback event every 25 µsec. The LT1070's internal error amplifier controls the energy in this event by forcing the feedback pin, FB, to a 1.23V reference level. The RC damper network on the error amplifier's high-impedance output (V_C pin) provides compensation to stabilize





(b)

TRACE	VERTICAL	HORIZONTAL
A	0.02V/DIV (AC COUPLED)	1 SEC/DIV
B	5V/DIV	1 SEC/DIV
C	2V/DIV	1 SEC/DIV
D	10V/DIV	1 SEC/DIV



(c)

TRACE	VERTICAL	HORIZONTAL
A	0.02V/DIV	20 mSEC/DIV
B	5V/DIV	20 mSEC/DIV
C	2V/DIV	20 mSEC/DIV
D	10V/DIV	20 mSEC/DIV

Fig 3—You can reduce quiescent current to only 150 µA *by pulling the V_C down to within 150 mV of ground* ***(a).*** *Under no-load conditions* ***(b),*** *the 12V output (trace A) ramps down over a number of seconds. During this period, the outputs of the paralleled 74C04 inverters and comparator IC_1 (trace B) are low, pulling the V_C pin low (trace C) and putting the LT1070 into its 50-µA shutdown mode. For a 3-mA load current* ***(c),*** *the loop-oscillation frequency increases to keep up with the load's sink-current demands.*

An isolated probe lets you make fully floating measurements even in the presence of high common-mode voltages.

the loop. This circuit works well, but it draws 9 mA of quiescent current. The 9 mA value might be excessive for applications that place size or weight limitations on the battery's capacity.

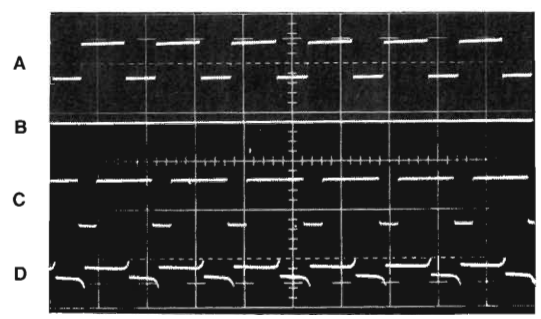
So how do you reduce quiescent current without degrading high-current performance? An auxiliary function of the LT1070's V_C pin offers one possible solution. When you pull V_C within 150 mV of ground, the LT1070 shuts down and draws only 50 μA. The special loop in **Fig 3a** exploits this feature, reducing the quiescent current to only 150 μA. This technique is particularly significant, and it has broad implications for battery-powered systems. IC_2 functions as a simple low-battery detector, pulling low when V_{IN} drops below 4.8V. You can readily employ the technique in a wide variety of dc/dc converters to meet the needs of a great number of applications.

The signal flow in **Fig 3**'s circuit somewhat mirrors the flow in **Fig 2**'s circuit. However, **Fig 3a** has additional circuitry between the feedback divider and the V_C pin. In addition, the circuit in **Fig 3a** does not use the LT1070's internal feedback amplifier and reference. **Fig 3b** shows operating waveforms for **Fig 3a** under no-load conditions.

The 12V output (trace A) ramps down over a period of seconds. During this period, the outputs of the paralleled 74C04 inverters and comparator IC_1 (trace B) are low, pulling the V_C pin low (trace C) and putting the LT1070 into its 50-μA shutdown mode. The V_{SW} pin (trace D) is high during this sequence, so there's no inductor current flow. When the 12V output decreases about 20 mV, IC_1 triggers and the 74C04 inverter outputs go high.

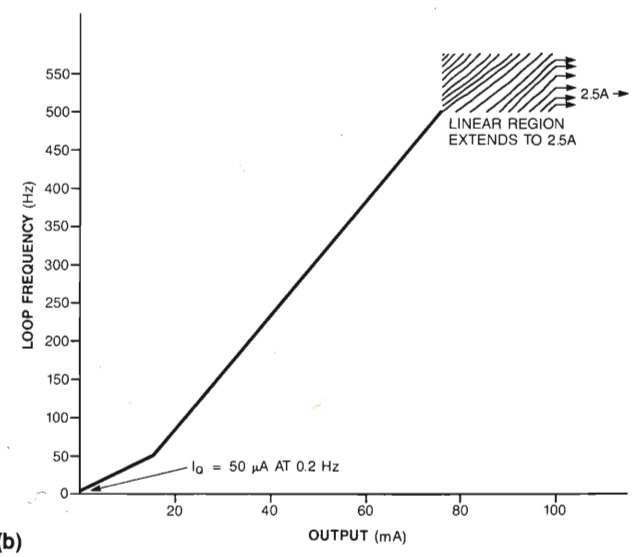
This inverter output transition pulls the V_C pin high and turns on the LT1070. The V_{SW} pin pulses the inductor at the 40-kHz clock rate, abruptly increasing the circuit's output. This transition triggers IC_1 low and forces the V_C pin back into the shutdown mode. This bang-bang control loop keeps the 12V output within the 20-mV ramp-hysteresis window set by R_3 and R_4. Diode clamps prevent any overdrive at the V_C pin. Note that the 4- to 5-sec loop-oscillation period minimizes the significance of the R_6-C_2 time constant at V_C. Because the LT1070 spends most of the time in a shutdown mode, the circuit draws very little quiescent current.

Fig 3c shows the same waveforms for a 3-mA load current. The loop-oscillation frequency increases to keep up with the load's sink-current demands. The V_C pin's waveform (trace C) now begins to take on a filtered appearance, thanks to R_6-C_2's 10-msec time constant. If the load continues to increase, the loop-oscillation frequency will also increase. The Ris fixed, however. Above some frequency, therefore, the R_6-C_2



TRACE	VERTICAL	HORIZONTAL
A	0.02V/DIV	20 μSEC/DIV
B	5V/DIV	20 μSEC/DIV
C	2V/DIV	20 μSEC/DIV
D	10V/DIV	20 μSEC/DIV

(a)



(b)

Fig 4—When you look at the waveforms for a 1A load, *you see that the V_C pin is at dc and the repetition rate now equals the LT1070's 40-kHz clock frequency* ***(a).*** *As the loading increases* ***(b),*** *the loop oscillates at a higher frequency because of C_1's decreased decay time.*

network must average loop oscillations to dc.

When you look at the waveforms for a 1A load (**Fig 4a**), you see that the V_C pin is at dc and the repetition rate now equals the LT1070's 40-kHz clock frequency. **Fig 4b** plots what's happening. As the output current rises, the loop-oscillation frequency also increases until it reaches approximately 500 Hz. At 500 Hz, the R_6-C_2 time constant filters the V_C pin to dc, and the LT1070 goes into normal operation. When the V_C pin is at dc, it's convenient to think of **Fig 3a**'s IC_1 and the inverters as a linear error amplifier with a closed-loop gain set by the R_1-R_2 feedback divider. Actually, IC_1 is still duty-cycle modulating, but it's doing so at a rate far above R_6-C_2's break frequency. The R_6-C_2 roll-off plus the R_7-C_3 network dominate the phase-error contribution from C_1 (which was selected for low loop frequency at low output currents). The loop is stable, and it responds linearly for all loads greater than 80 mA. In this high-current region, the LT1070 is actually fooled into behaving as it does in **Fig 2**'s circuit.

Simplifications give insight into loop's stability

Performing a formal stability analysis for this circuit is quite complex, but some simplifications can provide insight into the loop's operation. When the load current is 100 μA, C_1 and the load resistance form a decay time constant that exceeds 300 sec. This value is larger by several orders of magnitude than the R_7-C_3 and R_6-C_2 time constants or the LT1070's 40-kHz commutation rate. As a result, C_1 dominates the loop.

Wideband amplifier IC_1 sees phase-shifted feedback that develops very-low-frequency oscillations similar to those that occur in **Fig 3b.** Some layouts may require substantial trace area for IC_1's inputs. In such cases, the optional 10-pF capacitor shown in **Fig 2a** ensures clean transitions at IC_1's output. Although C_1 has a long *decay* time constant, it has a short *charge* time constant because the circuit has a low source impedance. These disparate time constants account for the ramp-like nature of the oscillations.

You can reduce the C_1 load's time constant by increasing the loading. As the loading increases (**Fig 4b**), the loop oscillates at a higher frequency because of C_1's decreased decay time. When the load impedance becomes low enough, C_1's decay time constant ceases to dominate the loop and passes control to the R_6-C_2 combination. Once R_6 and C_2 take over as the dominant time constant, the loop begins to behave as a linear system does.

In the region above 75 mA, the LT1070 runs continuously at its 40-kHz clock rate. Now the R_7-C_3 time constant becomes significant, and it acts as a simple feedback lead to smooth the output response.

Selecting values for R_7 and C_3 involves a fundamental tradeoff. When the converter is running in its linear

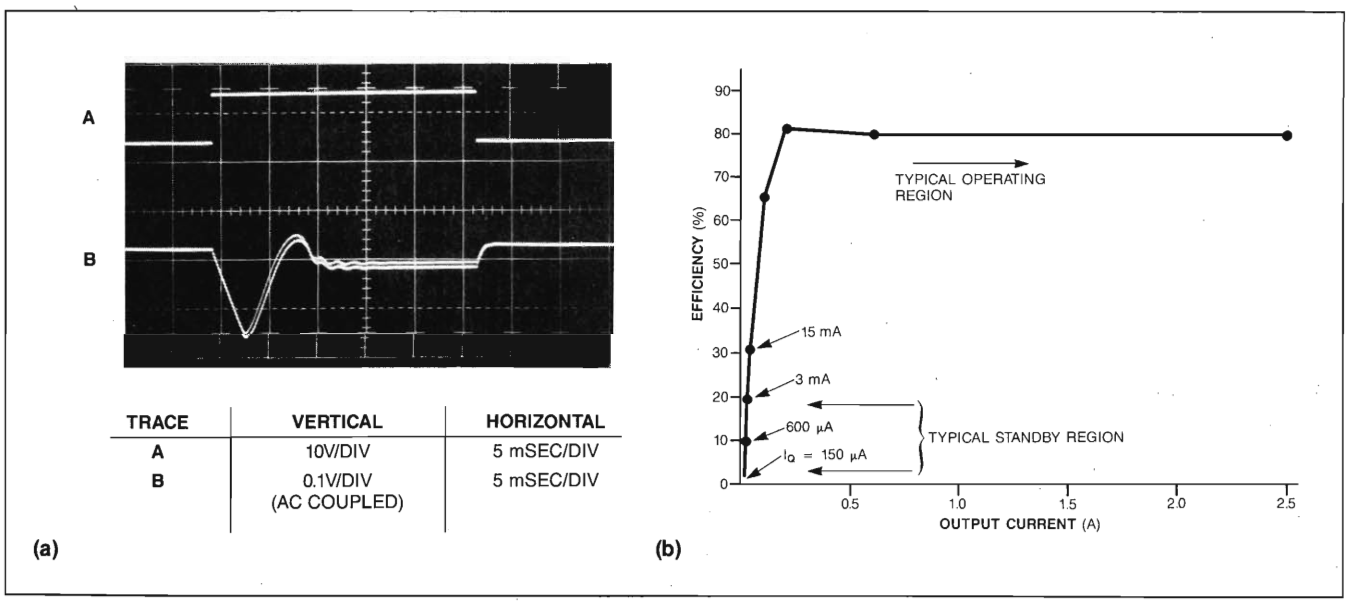


Fig 5—Despite the complex dynamics inherent in Fig 3, *the transient response for a no-load-to-1A step* ***(a)*** *is quite good. When you look at the converter's efficiency performance* ***(b),*** *you'll note that the converter's high-power efficiency matches that of standard converters, and its low-power efficiency is somewhat better than that available from standard converters.*

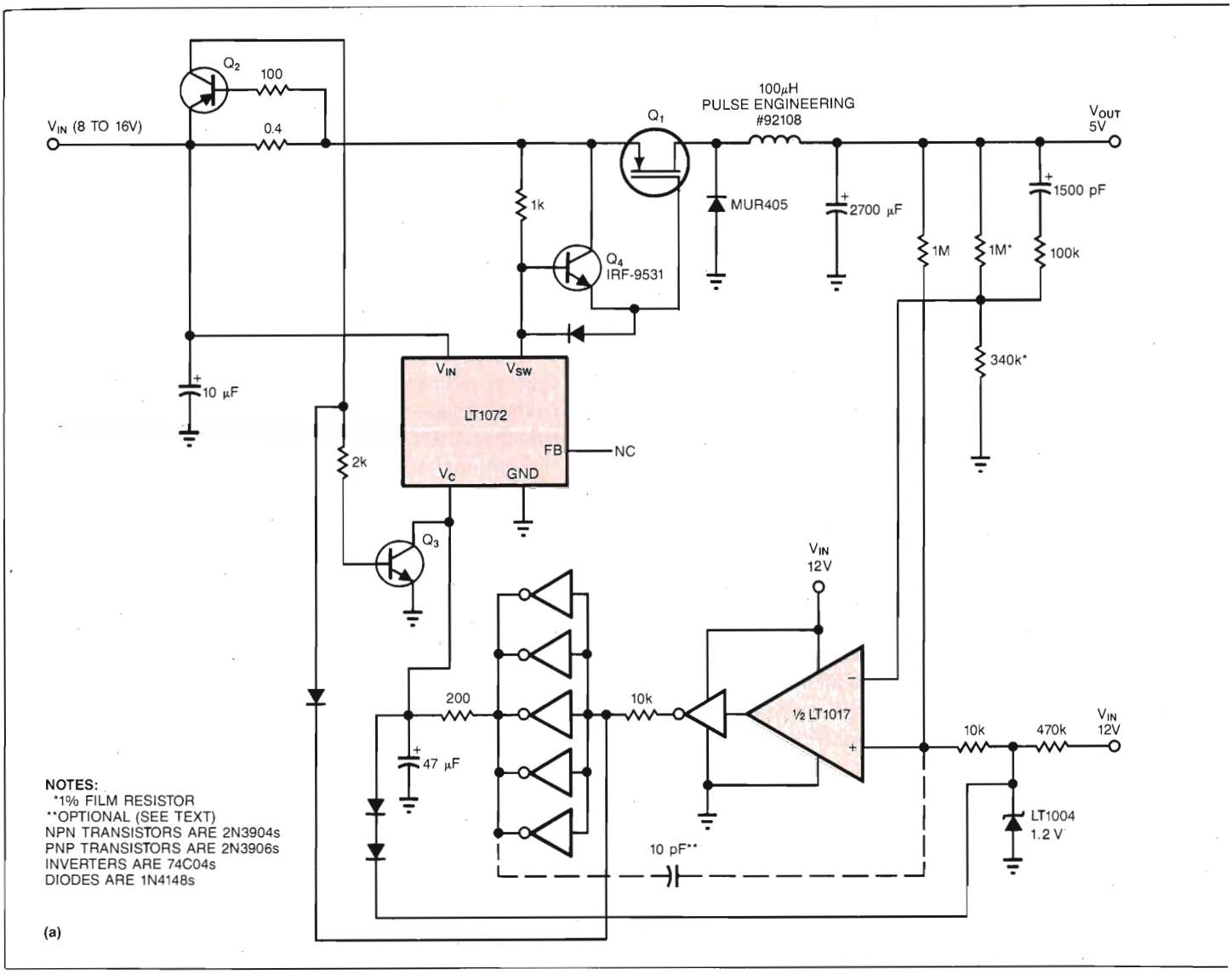


Fig 6—Using the special loop technique to introduce conditional instability *works just as well in step-down converters* ***(a).*** *In transformer-coupled converters* ***(b),*** *you can use the loop technique to develop multiple outputs.*

region, R_7 and C_3 must dominate the designed-in dc hysteresis generated by R_3-R_4. As a result, you must select values for R_7 and C_3 that provide the best compromise between the output ripple at high load levels and the loop's transient response.

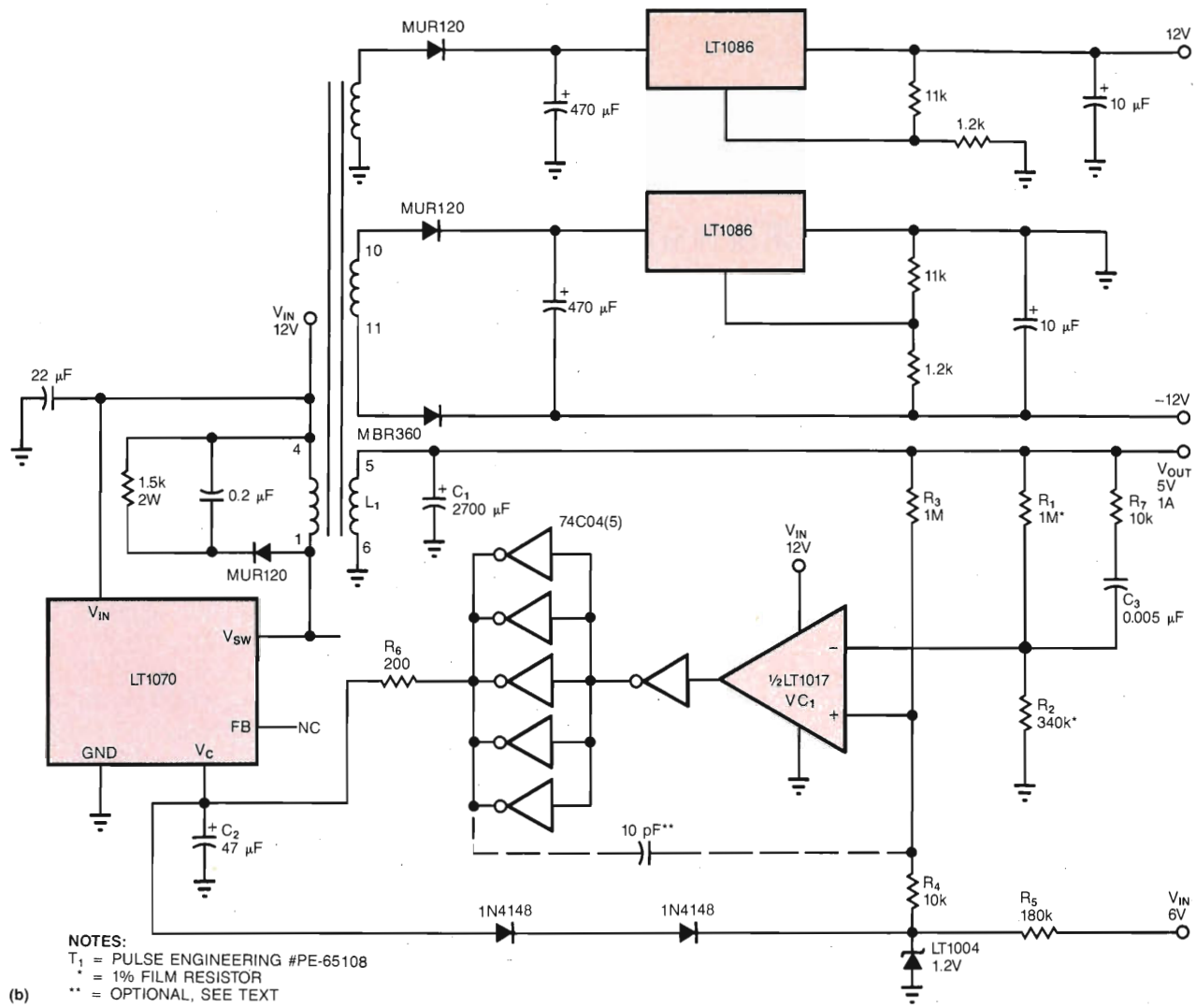
Flyback converter has good transient response

Despite the complex dynamics, the transient response of **Fig 3a** is very good. **Fig 5a** illustrates the circuit's performance for a no-load-to-1A step. When trace A goes high, a 1A load (trace B) appears across the output. Initially, the slow loop-response time causes the output to sag by almost 150 mV. When the LT1070 comes on (signaled by the 40-kHz fuzz at the very bottom of trace B), the output response is reasonably quick and surprisingly well behaved, considering the circuit dynamics. The multitime-constant decay (or rattling) shows up as trace B approaches steady state between the fourth and fifth vertical divisions.

Fig 5b plots efficiency versus output current for **Fig 3a**'s circuit. The circuit's high-power efficiency matches that of standard converters. Its low-power efficiency is somewhat better than that available with standard converters. Its standby efficiency is rather low, but that fact is not particularly bothersome, because the power loss approaches battery self-discharge levels.

The special loop in **Fig 3a** provides a controlled, conditional instability, rather than the usually more desirable and often elusive unconditional stability. This deliberately introduced characteristic lowers the converter's quiescent current by a factor of 60 without sacrificing high-power performance. This special loop technique is not restricted to boost-type converters—it will readily work in other designs.

The step-down (buck-mode) configuration in **Fig 6a,** for example, uses the same basic loop and most of the same components. The LT1072 (a low-power version of the LT1070) drives Q_1 (a p-channel MOSFET) to convert a 12V input to a 5V output. Q_2 and Q_3 provide current limiting, and Q_4 supplies turn-off drive for Q_1. **Fig 6a**'s hysteresis biasing (the 1-MΩ resistor at the comparator's noninverting input) differs slightly from



that of **Fig 2a** because of the lower output voltage. In other respects, the loop and its performance are identical to those of **Fig 2a**. **Fig 6b** shows how you can use this loop concept in a transformer-coupled converter. Note that the floating secondaries allow the circuit to generate a ±12V output. EDN

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Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art, and collecting antique scientific instruments.

Article Interest Quotient (Circle One)
High 488 Medium 489 Low 490

DESIGNER'S GUIDE

dc/dc converters
Part 3

Design dc/dc converters for power conservation and efficiency

This article, part 3 of a 4-part series, will demonstrate design techniques for optimizing power conservation, efficiency, and wide input range in dc/dc converters. Parts 1 and 2 of this series covered the design of 5- to ±15V converters and the proper use of instrumentation in converter design. Part 4 will show how to replace inductors with switched-capacitor techniques in dc/dc-converter designs.

Jim Williams and Brian Huffman,
Linear Technology Corp

At first glance, converter power drain, efficiency, and input range might seem an odd threesome. In portable applications, however, power drain and efficiency go hand in hand. And wide-input-range capability is often closely related to both these parameters. In applications where space or reliability are major considerations, it's sometimes best to operate circuitry from a single 1.5V cell. This objective eliminates almost all ICs as design candidates. Although it's possible to design circuitry that runs directly from a single cell, a dc/dc converter with a wide input-range capability allows you to use standard higher-voltage ICs.

Fig 1's design converts the output of a 1.5V cell to a 5V output and features quiescent current of only 125 μA. Oscillator IC_{1a}'s output—trace D in **Fig 1b**—is a 2-kHz square wave. This circuit has a conventional configuration, with one exception: The biasing scheme accommodates the narrow common-mode range available with the 1.5V supply. To maintain low power, IC_{1a}'s integrating capacitor has a small value, which limits the swing to only 50 mV. IC_{2a} and IC_{2b} operate in parallel to drive T_1. This parallel connection minimizes saturation losses.

When the 5V output (trace A) slopes down far enough, IC_{1b}'s output goes low (trace B) and pulls the noninverting inputs of both IC_{2a} and IC_{2b} close to ground. IC_{1a}'s clock signal now forces energy into T_1. T_1's flyback pulses, rectified and stored in the 47-μF capacitor, form the converter's dc output. IC_{1b} on-off modulates C_2 at whatever duty cycle is necessary to maintain the converter's 5V output. The LT1004 serves as a reference, and the resistor divider at IC_{1b}'s positive input sets the output-voltage level. The Schottky clamp at IC_2's outputs prevents any parasitic behavior of T_1 from developing negative-going overdrives.

The LT1004's output is bootstrapped to the 5V output so that the converter can operate with inputs as low as 1.1V. The 10-MΩ bleed resistor ensures circuit start-up, and the 1-MΩ resistors divide the 1.2V reference to keep IC_{1b} within common-mode limits. IC_{1b}'s positive feedback establishes hysteresis of about 100 mV, and the 22-pF capacitor suppresses high-frequency oscillations.

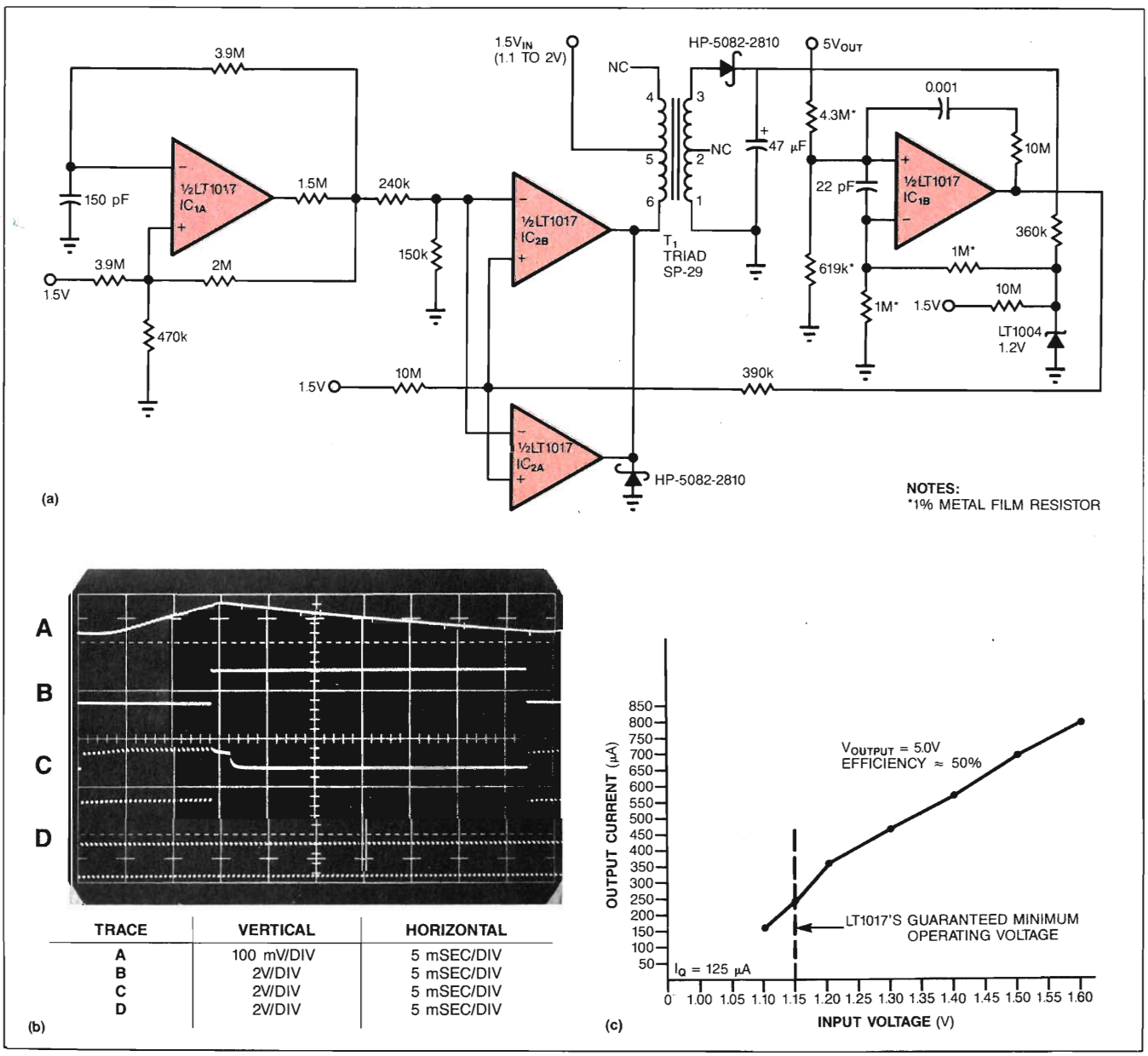
This circuit's low duty cycle at light loads minimizes quiescent current. The 125-μA figure noted is quite close to the LT1017's steady-state currents. As the

In small portable computers, converters must operate from a battery input with very high efficiency.

load increases, the duty cycle increases to meet the demand, drawing more power from the battery. A decrease in the battery's output voltage produces similar behavior.

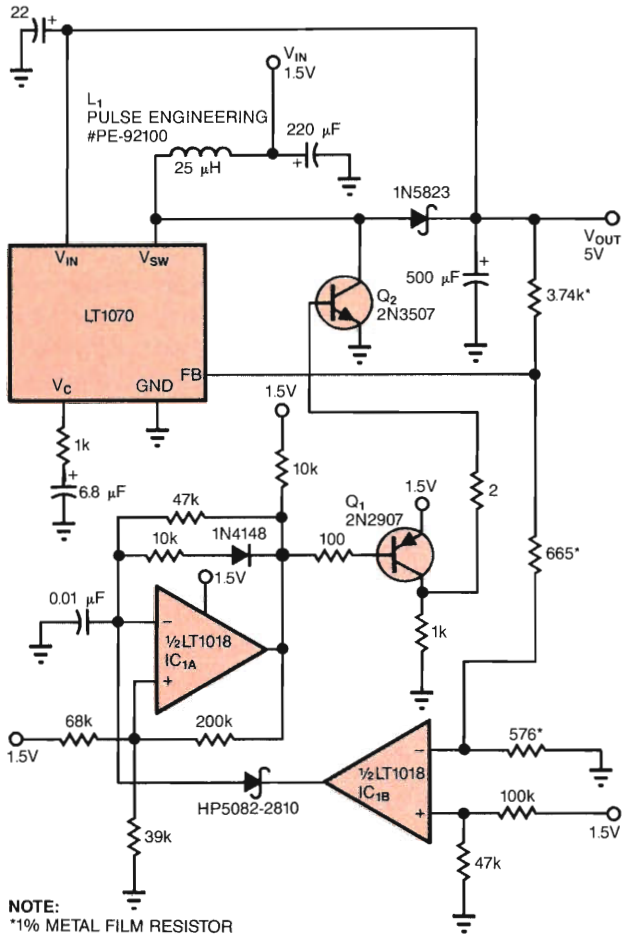
Fig 1c plots the available output current versus the battery voltage for **Fig 1a**. Predictably, the highest power is available from a fresh cell, although the circuit maintains regulation to 1.15V for 250-μA loading. Because of the low supply voltage, it's difficult to control the saturation and other losses in **Fig 1**'s circuit. As a result, the circuit's efficiency is only about 50%.

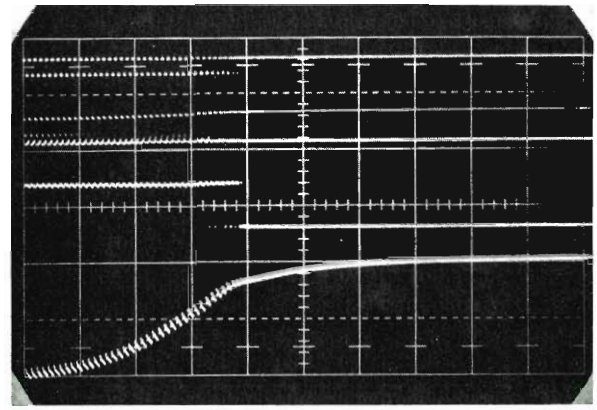
Fig 1's circuit is useful in low-power applications, but some 1.5V systems require much more power. **Fig 2**'s circuit provides a 5V/200-mA output. Assuming that **Fig 2**'s circuit operates continuously at high power, its quiescent-current level is allowed to be higher than



TRACE	VERTICAL	HORIZONTAL
A	100 mV/DIV	5 mSEC/DIV
B	2V/DIV	5 mSEC/DIV
C	2V/DIV	5 mSEC/DIV
D	2V/DIV	5 mSEC/DIV

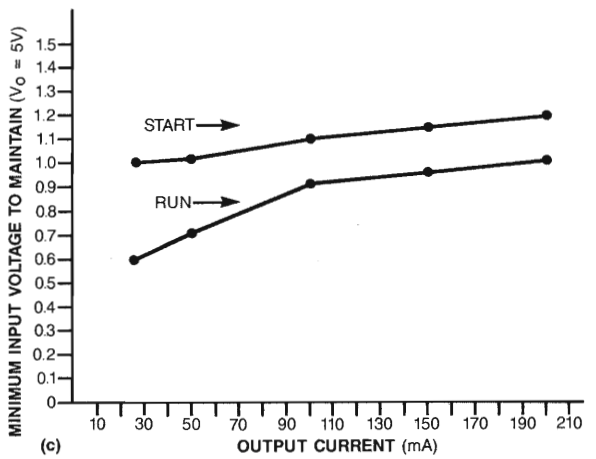
Fig 1—Featuring a quiescent current of only 125 μA, *this dc/dc converter* ***(a)*** *generates 5V from a 1.5V cell input. Oscillator IC_{1a}'s output is a 2-kHz square wave (**b,** trace D). A plot of output current versus battery voltage* ***(c)*** *shows that the highest power is available from a fresh cell.*



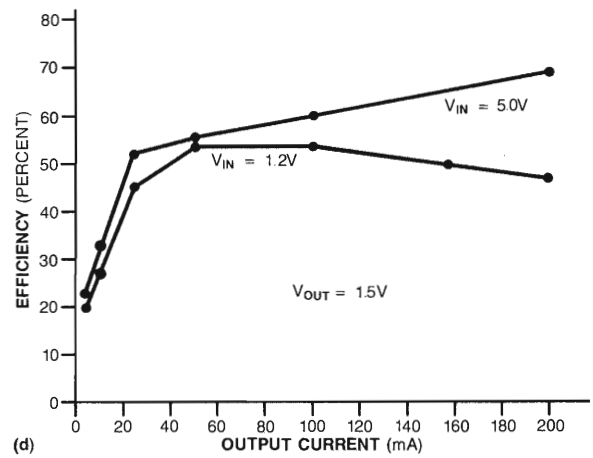


(b)

TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	2 mSEC/DIV
B	10V/DIV	2 mSEC/DIV
C	2V/DIV	2 mSEC/DIV
D	1V/DIV	2 mSEC/DIV



(c)



(d)

Fig 2—Essentially a flyback-type regulator, *this dc/dc converter* ***(a)*** *generates 5V at 200 mA. When power is applied, IC_{1a} oscillates at 5 kHz* ***(b)****. The circuit's input-output characteristics* ***(c)*** *illustrate that the circuit will start into a full load as long as the battery voltage equals 1.2V. Although the circuit's performance is impressive, its quiescent power requirements at lower currents degrade its efficiency figures* ***(d)****.*

that of **Fig 1**.

The circuit in **Fig 2** is essentially a flyback-type regulator. Because the LT1070 exhibits low saturation losses and is easy to apply, it's simple to design the flyback regulator to supply the 1W output. Unfortunately, the LT1070 has a 3V min supply-voltage requirement. Bootstrapping from the 5V converter output to the LT1070's supply pin satisfies that requirement. The dual comparator (IC_{1a} and IC_{1b}) and the transistors form a start-up loop.

When power is applied, IC_{1a} oscillates at 5 kHz (see trace A in **Fig 2b**), biasing Q_1 and allowing it to drive the base of Q_2. Q_2's collector (trace B) pumps energy into L_1 and generates step-up voltage-flyback signals. These signals are rectified and stored in the 500-µF capacitor to produce the converter's 5V output.

In many applications, dc/dc converters must accommodate a wide range of input voltages.

IC_{1b} is configured so that its output (trace C) goes low when the converter's output crosses the 4.5V level. When IC_{1b}'s output goes low, IC_{1a}'s integration capacitor pulls low and terminates the circuit's oscillations. Under these conditions, Q_2 can no longer drive L_1. The LT1070 can, however. You can see this behavior (trace D) at the LT1070's V_{SW} pin. When the start-up circuit activates, the V_{IN} pin of the LT1070 has an adequate supply voltage and starts to operate—at the fourth vertical division in **Fig 2b**'s scope photo. There's some overlap between the turn-off of the start-up loop and the LT1070's turn-on, but it has no detrimental effect.

Careful design allows the start-up loop to function over a wide range of loads and battery voltages. Start-up currents exceed 1A, so Q_2's saturation and drive characteristics are particularly important.

Fig 2c plots the circuit's I/O characteristics. Note that the circuit will start for all loads as long as the battery voltage is 1.2V or better. With reduced loads, the circuit will start for battery levels as low as 1V. Once the circuit starts, it can drive full 200-mA loads with battery voltages as low as 1V. **Fig 2d** plots the efficiency of **Fig 2a**'s circuit at two supply-voltage levels for a range of output currents. Although the circuit's performance is impressive, its quiescent power requirements at lower currents degrade its efficiency figures. Fixed junction-saturation losses at the lower supply-voltage levels are responsible for the lower overall efficiency.

Addressing the efficiency question

Efficiency is a prime concern in some converter applications (see **box,** "Design converters for optimum efficiency"). In small portable computers, for example, the converter typically must generate 5V from a 12V

Design converters for optimum efficiency

Squeezing the utmost efficiency out of a converter is a complex, demanding design task. To obtain efficiencies in excess of 80 to 85%, you'll have to use some finesse, some witchcraft, and some plain luck. The interaction of electrical and magnetic terms produces subtle effects that influence a converter's efficiency. It's not possible to establish a detailed, generalized method for obtaining maximum converter efficiency, but it's easy to list some guidelines.

Losses fall into several loose categories: junction, ohmic, drive, switching, and magnetic. Semiconductor junctions produce losses. Diode drops increase with operating current, a fact that can be quite costly in low-output-voltage converters. A 700-mV drop in a 5V-output converter introduces a loss of more than 10%. Schottky devices will cut this loss by almost 50%, but it's still appreciable. Germanium devices, which are rarely used today, cut losses even more, but their switching losses negate their low-drop performance at high speeds. Germanium devices' reverse leakage may be equally oppressive in very-low-power converters.

Synchronously switched rectification **(Fig 3a)** is more complex, but it can sometimes simulate a more efficient diode. When evaluating such a scheme, however, remember to include both ac and dc drive losses in efficiency calculations. DC losses include base or gate current in addition to dc consumption in any driver stage. AC losses might include the effects of gate (or base) capacitance, transition region dissipation, and power lost because of the delay between the application of the drive and the actual switch action.

Transistor saturation losses are also a significant term. Channel and collector-emitter saturation losses become increasingly significant as the operating voltage decreases. The most obvious way to minimize these losses is to select low-saturation components. This scheme will work, in some cases, but remember to include drive losses (which are usually higher for low-saturation devices) in overall loss estimates.

Sometimes, it's difficult to ascertain the actual losses caused by saturation effects and diode drops. Changing duty cycles and time-variant currents complicate matters. However, there's one simple way to make relative-loss judgments: You can measure the rise in device temperature. Unfortunately, this technique is not very effective at low power levels. In some cases, you can determine losses by deliberately adding a known loss to the component in question and then noting any change in efficiency.

Ohmic losses in conductors are

battery input, and it must do so very efficiently. With a 90% efficiency rating, the positive buck converter in **Fig 3a** fills the bill easily.

Transistor Q_1 serves as the pass element. Replacing the catch diode typically used in buck-type converters with a a synchronous rectifier (Q_2) improves the efficiency of **Fig 3a**'s circuit. The input supply is nominally 12V, but it can vary from 9.5 to 14.5V. The NMOS transistors used for Q_1 and Q_2 have a low (0.028Ω) source-to-drain resistance, which minimizes power losses. The inductor's low-loss core material helps squeeze a little more efficiency out of the design. In addition, keeping the current sense-threshold low minimizes the power loss in the current-limiting circuit.

Fig 3b illustrates the operating waveforms. When the V_{SW} pin turns off (trace A), Q_5 drives Q_2. Q_2 turns off (through D_1 and D_2) when V_{SW} is on. To turn on Q_1, you must drive its gate (trace B) above the input-voltage level. C_1, bootstrapped from the drain of Q_2 (trace C), provides this drive. C_1 charges up through D_1 when Q_2 turns on. When Q_2 turns off, Q_3 conducts to provide a path for C_1 to turn Q_1 on. During this period, current flows through Q_1 (trace D), through the inductor (trace E), and into the load.

Q_1 turns off when the V_{SW} pin is off, allowing Q_5 to turn on Q_4 and pull Q_1's gate low through D_3 and the 50Ω resistor. This resistor reduces the noise voltage generated by Q_1's fast switching transitions. Q_1 must be off when Q_2 is conducting (trace F). The efficiency of **Fig 3a**'s circuit will suffer if both transistors are conducting simultaneously. The 220Ω resistors combine with D_2 to minimize any switch-cycle overlap.

Transistors Q_6 through Q_9 provide short-circuit protection. The LT1004, Q_6, and the 9-kΩ resistor generate a 200-μA current that flows through R_1 and develops a 124-mV threshold for the Q_7-Q_8 comparator.

usually significant only at higher current levels. Hidden ohmic losses include socket and connector contact resistance and equivalent series resistance (ESR) in capacitors. ESR generally decreases as the capacitance value increases, and increases as the operating frequency increases.

Don't forget the copper resistance of inductive components. Quite often, you have to evaluate the tradeoffs between an inductor's copper resistance and its magnetic characteristics.

Components make a difference

Drive losses are also important when it comes to efficiency. A MOSFET's gate capacitance draws substantial ac drive current per cycle, which implies that average currents will increase as frequency increases. Bipolar devices have lower capacitance, but dc base-current requirements make them very power hungry.

Large-area devices may appear attractive because of their low saturation, but you must evaluate drive losses carefully. Usually, large-area devices are viable only when the converter will operate consistently at a significant percentage of its rated current.

Efficiency should be a major consideration in any drive-circuit design. Class A drives (resistive pull-up or pull-down drives) are simple and fast, but they're inefficient. For efficient operation, you'll typically need to use active source-sink combinations that have minimal cross-conductance and biasing losses.

Switching losses occur when devices spend significant amounts of time (relative to operating frequency) in their linear region. At higher repetition rates, transition times can become a substantial source of loss. Proper device selection and drive-circuit design can minimize these losses.

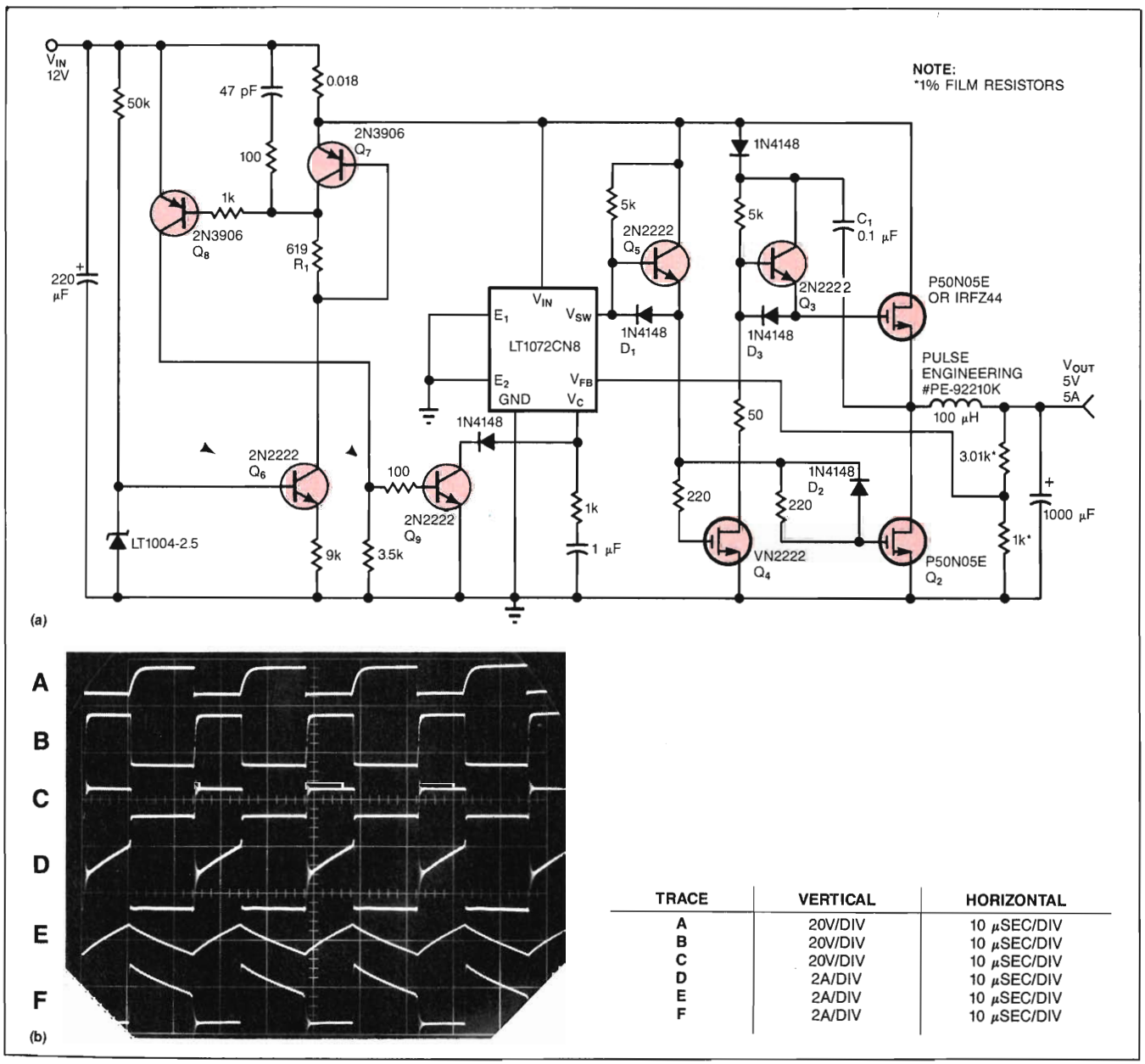
Magnetics design can also influence a converter's efficiency. It's important for you to consider such issues as core-material selection, wire type, winding techniques, size, operating frequency, current levels, and temperature. Practically speaking, access to a skilled magnetics specialist is the only way to ensure a successful design. Fortunately, electrical losses typically outweigh magnetic losses, so you can usually realize fairly high efficiency by using standard magnetic components. If the converter's efficiency is still too low after you've reduced losses to the lowest practical level, you'll need to use custom magnetics.

The buck-boost converter topology is very useful in circuits where the input voltage can be either lower or higher than the output voltage.

When the voltage drop across the 0.018Ω sense resistor exceeds 124 mV, Q_8 turns on. The LT1072's V_{SW} pin goes off when the V_C pin drops below approximately 0.9V. This drop occurs when Q_8 forces Q_9 to saturate. The RC damper across Q_8 suppresses line transients that might turn on Q_8 prematurely.

Designing for wide input-range capability

Converters must often accommodate a wide range of inputs. Telephone-line voltages, for example, can vary over a considerable range. **Fig 4**'s circuit uses an LT1072 to supply a 5V output from a telecomm-type input. The raw telecomm supply is nominally −48V, but it can vary from −40 to −60V. The V_{SW} pin can accommodate this voltage range, but the V_{IN} pin requires some protection, because it has a 60V max rating. Q_1 and the 30V zener diode provide this protection, decreasing the V_{IN} pin's voltage to acceptable levels



TRACE	VERTICAL	HORIZONTAL
A	20V/DIV	10 µSEC/DIV
B	20V/DIV	10 µSEC/DIV
C	20V/DIV	10 µSEC/DIV
D	2A/DIV	10 µSEC/DIV
E	2A/DIV	10 µSEC/DIV
F	2A/DIV	10 µSEC/DIV

Fig 3—With a 90% efficiency specification, *this positive-buck-converter design readily satisfies the needs of small portable computers.*

under all line conditions.

In **Fig 4,** the top of the inductor is at ground and the LT1072's ground pin is at the negative supply-voltage rail. The LT1072's feedback pin senses signals with respect to the ground pin, so the 5V output must provide a level shift. Q_2 provides this shift by introducing a low (−2-mV/°C) drift. Such a drift normally presents no problems in a logic supply. In problem cases, the optional network shown will provide appropriate compensation.

The RC damper at the V_C pin provides frequency compensation. The 68V zener diode is designed to clamp and absorb excessive line transients that might otherwise damage the LT1072; the V_{SW} pin has a 75V max rating.

The approach in **Fig 5** has an even wider input range. In this case, the converter produces a −5V output (+5V optional). The coupled inductor will accommodate buck, boost, or buck-boost converter configurations. As the figure shows, this converter will handle an input range of 3.5 to 35V dc.

Fig 5b shows the operating waveforms for the circuit. When the V_{SW} pin is on (trace A), current flows through the transformer's primary winding (trace B). The reverse bias on catch diode D_1 prevents any current transfer to the secondary winding during this period: The energy is stored in the transformer's magnetic field. When V_{SW} turns off, D_1 forward-biases and transfers the energy to the secondary winding. Traces C and D show the voltage on the secondary winding and the current flow through the secondary winding, respectively. Because the transformer is not an ideal device, not all of the primary winding's energy is coupled into the secondary winding. The energy left in the primary winding generates overvoltage spikes on the V_{SW} pin (trace E).

A leakage-inductance term in series with the transformer's primary winding models this phenomenon. When V_{SW} turns off, the transformer current continues to flow, causing the snubber diode to conduct. As the

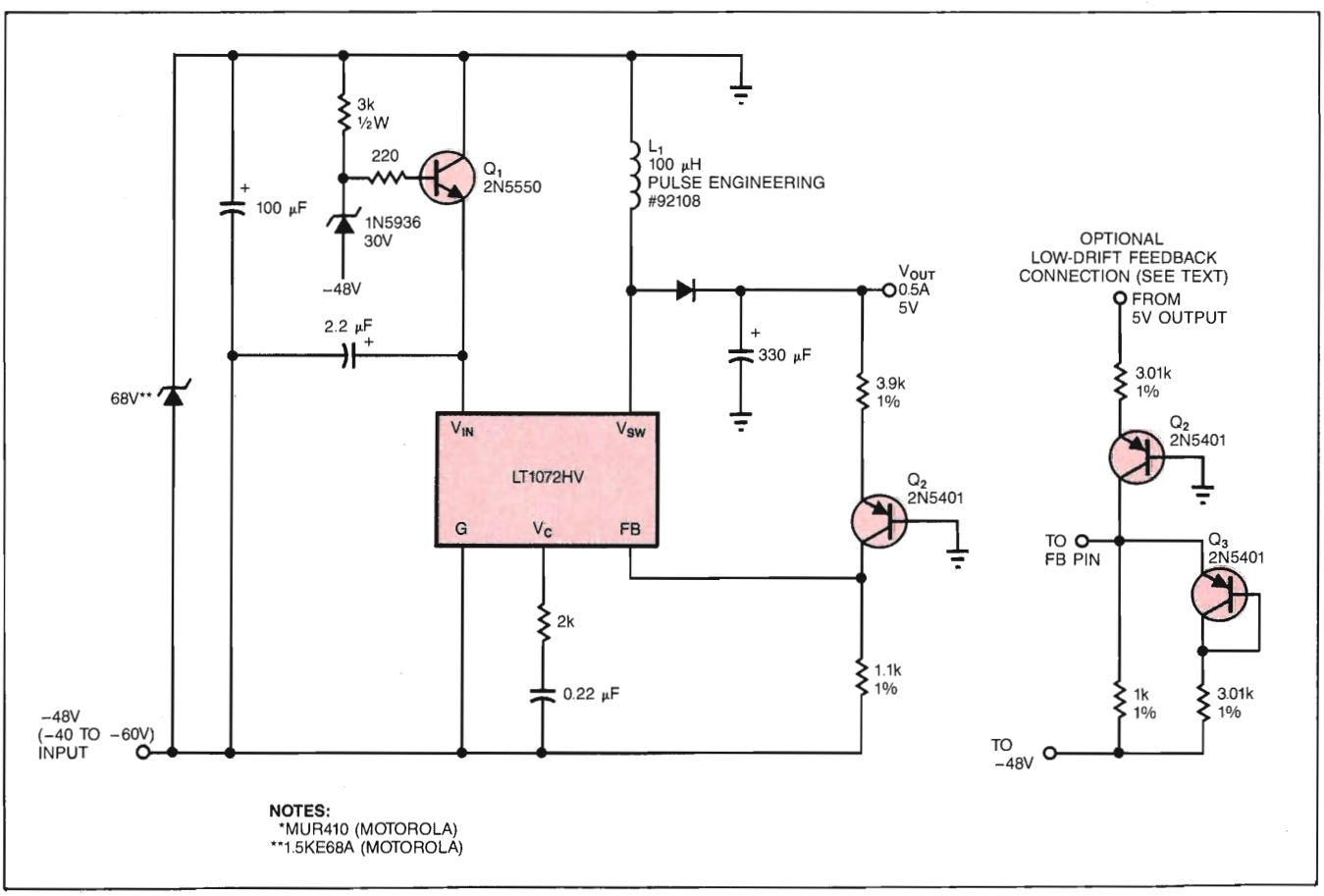


Fig 4—To accommodate applications with wide input-voltage ranges, *this converter can handle 40 to 60V dc signals.*

Linear converters don't encounter the dynamic problems that switching regulators face under varying input and output ranges.

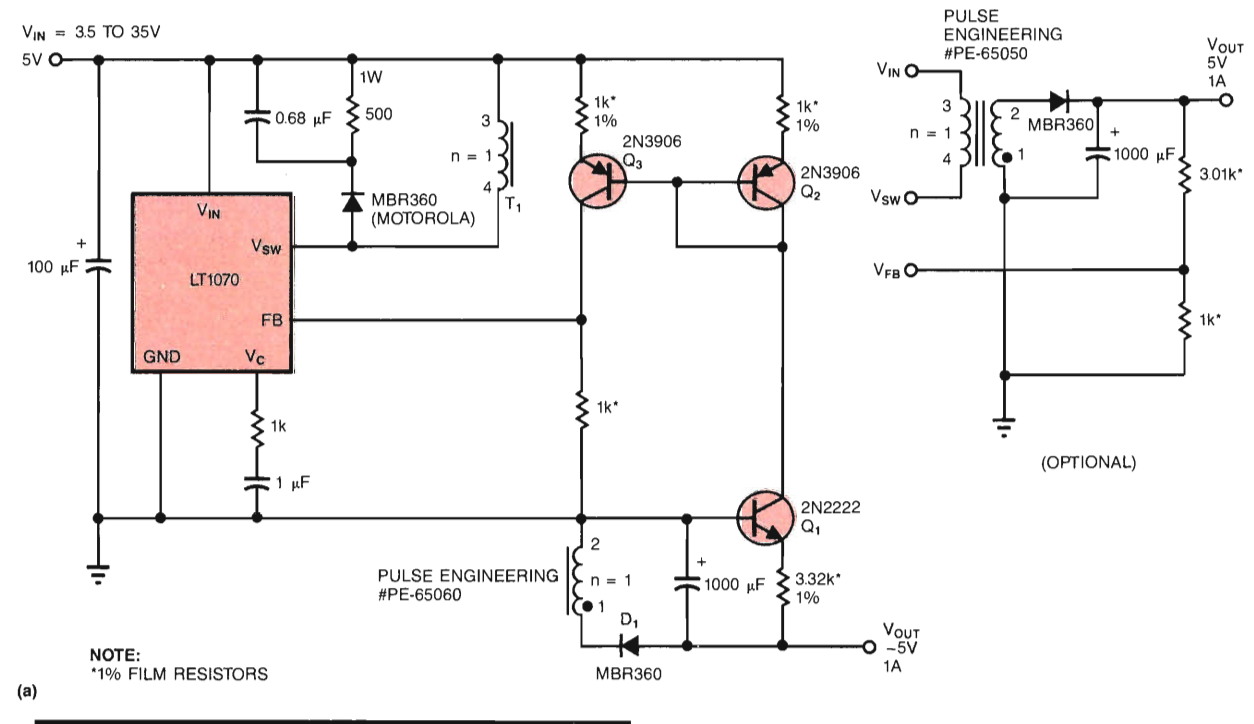
transformer loses its energy, the snubber-diode current falls to zero, clamping the voltage spike. The feedback pin senses with respect to ground, so Q_1 through Q_3 use the −5V output to provide a level shift.

The buck-boost solution for wide input range

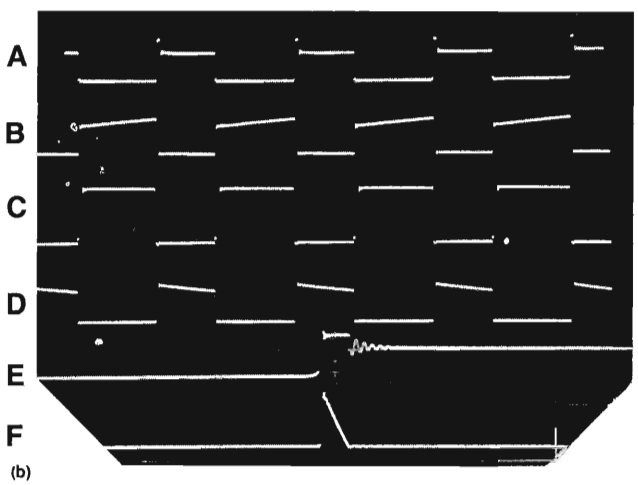
The buck-boost topology is useful in circuits whose input voltage can be either lower or higher than the output voltage. The design in **Fig 6** uses a single inductor in place of the transformer that you'd typically use in such designs. The circuit's operation somewhat mirrors that of **Fig 5**'s converter.

The pass-transistor gate-drive scheme is identical in both cases, except that in **Fig 6** the gate-source voltage is clamped so that it won't exceed the device's ±20V rating. **Fig 6b** shows the operating waveforms.

When V_{SW} is on (trace A), pass transistor Q_1 saturates. The gate voltage (trace B) is clamped by the



(a)



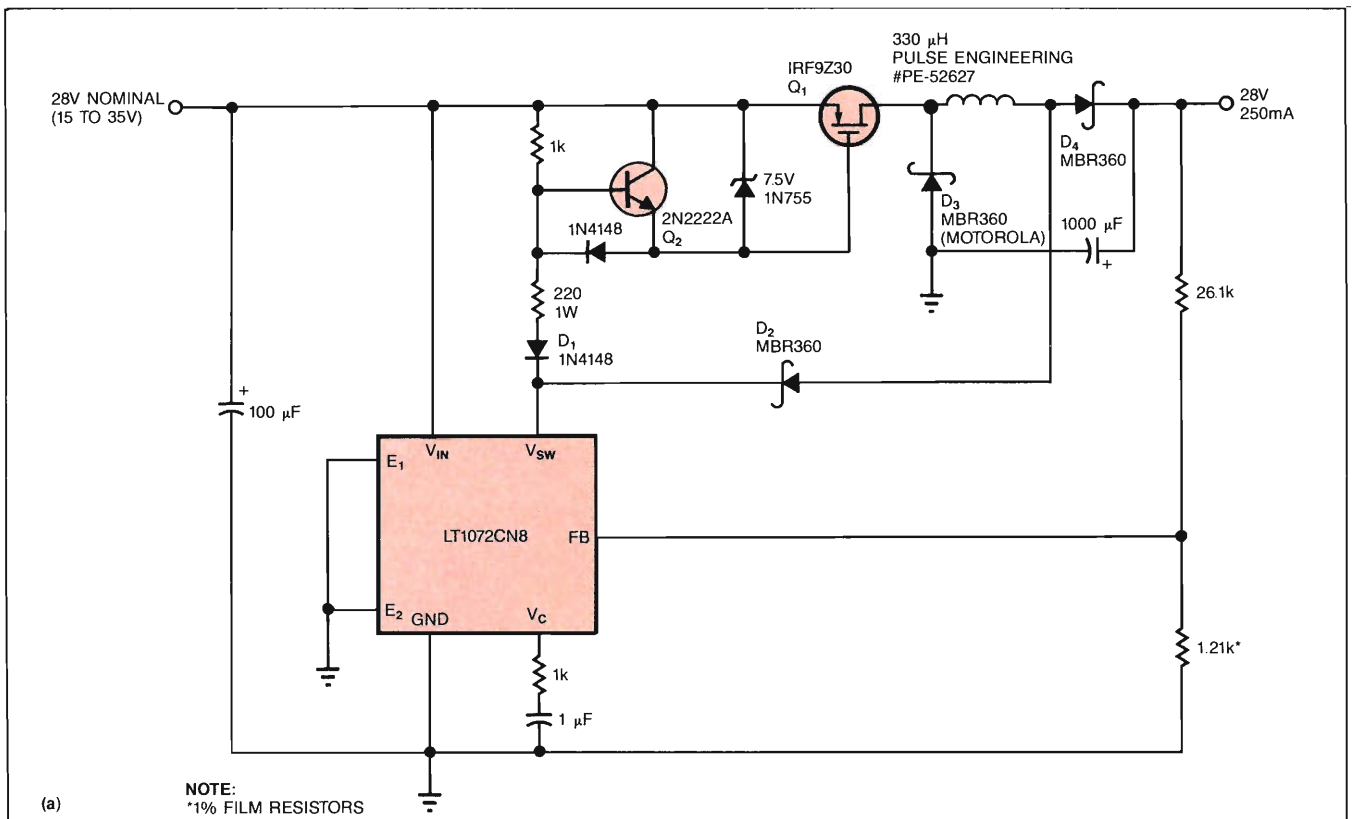
(b)

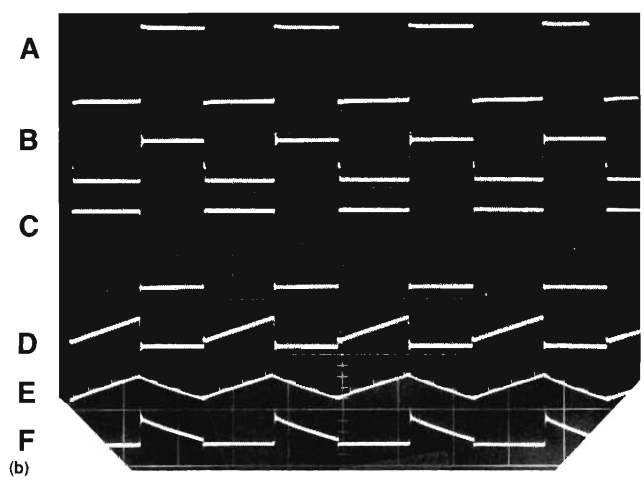
TRACE	VERTICAL	HORIZONTAL
A	20V/DIV	10 µSEC/DIV
B	4A/DIV	10 µSEC/DIV
C	10V/DIV	10 µSEC/DIV
D	4A/DIV	10 µSEC/DIV
E	20V/DIV	1 µSEC/DIV
F	2A/DIV	1 µSEC/DIV

Fig 5—Able to handle inputs ranging from 3.5 to 35V dc, *this circuit's coupled-inductor design will accommodate buck, boost, or buck-boost converter configurations.*

zener diode. Traces C and D show the voltage on Q_1's drain and the current through Q_1, respectively. The similarities between the two circuits end here.

In **Fig 6**'s circuit, the inductor is within one diode drop (D_2) above ground, instead of being tied to the output, as it is in **Fig 5**. As a result, the voltage drop across the inductor—except for Q_1's V_{BE} drop and saturation losses—is now equal to the input voltage. D_1 is reverse-biased, and it prevents the output capacitor from discharging into the V_{SW} pin. When the V_{SW} pin is off, Q_1 and D_2 cease to conduct. Because the current in the inductor (trace E) continues to flow, D_3 and D_4 forward-bias, allowing the inductor energy to transfer into the load. Trace F illustrates the current





TRACE	VERTICAL	HORIZONTAL
A	20V/DIV	10 µSEC/DIV
B	10V/DIV	10 µSEC/DIV
C	20V/DIV	10 µSEC/DIV
D	2A/DIV	10 µSEC/DIV
E	2A/DIV	10 µSEC/DIV
F	2A/DIV	10 µSEC/DIV

Fig 6—The buck-boost topology is useful *in circuits where the input voltage can be either lower or higher than the output voltage.*

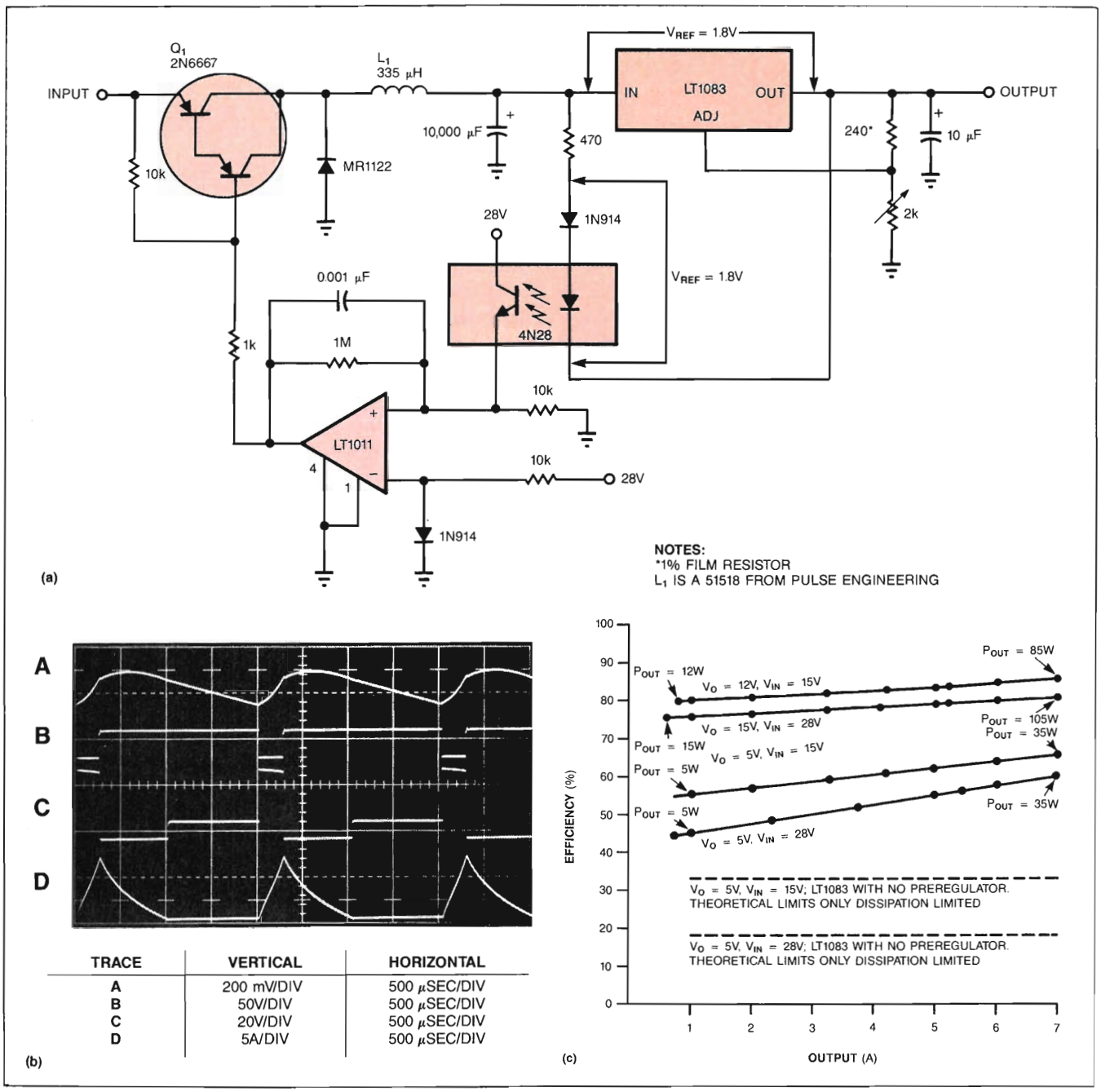


Fig 7—Although typical linear converters have efficiency and temperature-rise problems, *this design efficiently controls high power under widely varying input and output conditions.*

flow through D_3. D_2 prevents Q_1 from staying on when the circuit is operating in buck mode. D_1, on the other hand, blocks current flow into the gate-drive circuit when the converter is operating in boost mode.

A look at a linear-type solution

In a sense, linear regulators are extremely wide-range dc/dc converters. They don't encounter the dynamic problems that switching regulators face under varying input and output ranges. Linear regulators simply dissipate excess energy as heat. This elegantly simple energy-management mechanism creates a significant amount of inefficiency and temperature rise. **Fig 7** illustrates a design that allows a linear regulator to control high power efficiently under widely varying input and output conditions.

The regulator resides within a switched-mode loop that servocontrols the voltage *across* the regulator. In this arrangement, the regulator functions normally, while the loop maintains the voltage across the regulator at a minimal value regardless of line-, load- or output-setting changes. Although this approach can't match the efficiency of a classical switching regulator, it maintains the low noise and fast transient response inherent in the linear regulator.

The LT1083 functions conventionally, supplying a regulated, 7.5A output. The remaining components form the switched-mode, dissipation-limiting control loop. This loop forces the potential across the LT1083 to equal the 1.8V value of V_{REF}. The optoisolator pro-

Large-area devices may appear attractive because of their low saturation, but you must evaluate drive losses carefully.

vides a convenient way to look at the differentially sensed voltage across the LT1083 as though it were a single-ended input. When the regulator input (trace A in **Fig 7b**) decays far enough, the LT1011 output (trace B) switches low and turns Q_1 on (trace C), allowing current to flow from the circuit input (trace D) into the 10,000-μF capacitor and raise the regulator's input voltage.

When the regulator input rises high enough, the comparator goes high, turning off Q_1; the capacitor stops charging. The MR1122 damps the current-limiting inductor's flyback spike. The 0.001-μF/1-MΩ combination sets the loop hysteresis at about 100 mV p-p. This free-running, oscillation-control mode substantially reduces dissipation in the regulator without degrading its performance. Despite changes in the input voltage, regulated outputs, or load shifts, the loop always ensures minimum dissipation in the regulator.

Fig 7c plots the efficiency of the circuit in **Fig 7a** at various operating points. Thanks to the loop's performance, the circuit losses are relatively small at high output-voltage levels, and the circuit's efficiency is quite good. Its efficiency suffers at low output-voltage levels, but compares very favorably with the theoretical data for an LT1083 operating with no preregulator. At the higher theoretical dissipation levels, the LT1083 will shut down, precluding practical operation.

Meeting applications' high voltage needs

Fig 8's design features a fully floating output. This provision allows you to reference the output away from system ground, a technique that's often desirable for applications in which you want to limit noise or provide biasing. In this converter, galvanically isolated equivalents replace the LT1072's internal error amplifier and reference. Power for the replacement parts is bootstrapped from the output via source-follower Q_1 and its 2.2-MΩ ballast resistor. IC_1 and the LT1004 (both

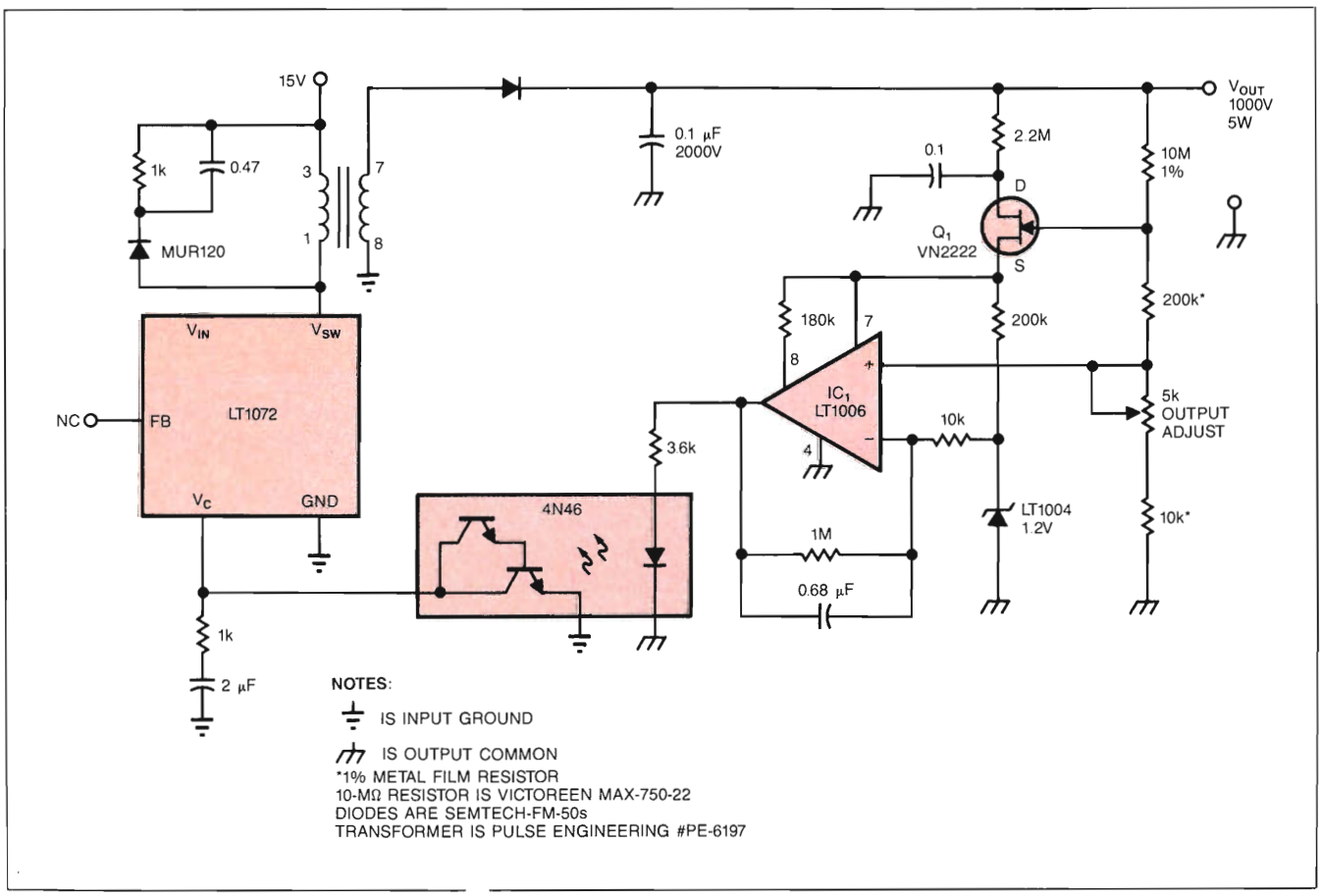


Fig 8—With a fully floating output, *this converter configuration allows you to reference the output away from system ground, a technique that's often desirable for applications in which you want to limit noise or provide biasing.*

Squeezing the utmost efficiency out of a converter requires some finesse, some witchcraft, and some luck.

are micropower components) minimize dissipation in the Q_1/ballast-resistor combination.

Q_1's gate bias, tapped from the output divider string, produces about 15V at its source. IC_1 compares the scaled divider output with the LT1004 reference. The error signal (IC_1's output) drives the optocoupler, which operates at low levels, saving power. The optocoupler's output pulls down on the V_C pin to close the loop. Frequency compensation at the V_C pin and IC_1 stabilizes the loop.

Transformer and optocoupler restrictions impose limitations on the common-mode breakdown performance in **Fig 8**'s converter. Isolation amplifiers, certain transducer measurements, and ESD-sensitive applications require high breakdown capability. In addition, very precise floating measurements such as signal conditioning for high-impedance bridges can require extremely low leakeage to ground.

You need to take a different design approach to achieve high common-mode voltage capability with minimal leakage. Some feel that a magnetic approach is the only viable way to achieve the isolated transfer of appreciable amounts of electrical energy. That idea is simply not correct: You can employ ceramics to solve the high-energy/low-leakage problem. In fact, the high voltage breakdown and low electrical conductance associated with ceramics surpasses the isolation characteristics of magnetic approaches. In addition, the acoustic transformer is a simple device.

You can form the transformer by bonding a pair of leads to each end of the ceramic material. In such a simple structure, the insulation resistance can exceed $10^{12}\Omega$, and primary-secondary capacitances can measure in the 1- to 2-pF range. The resonant frequency is a function of the material and its characteristics. You can think of the device as a high-Q resonator

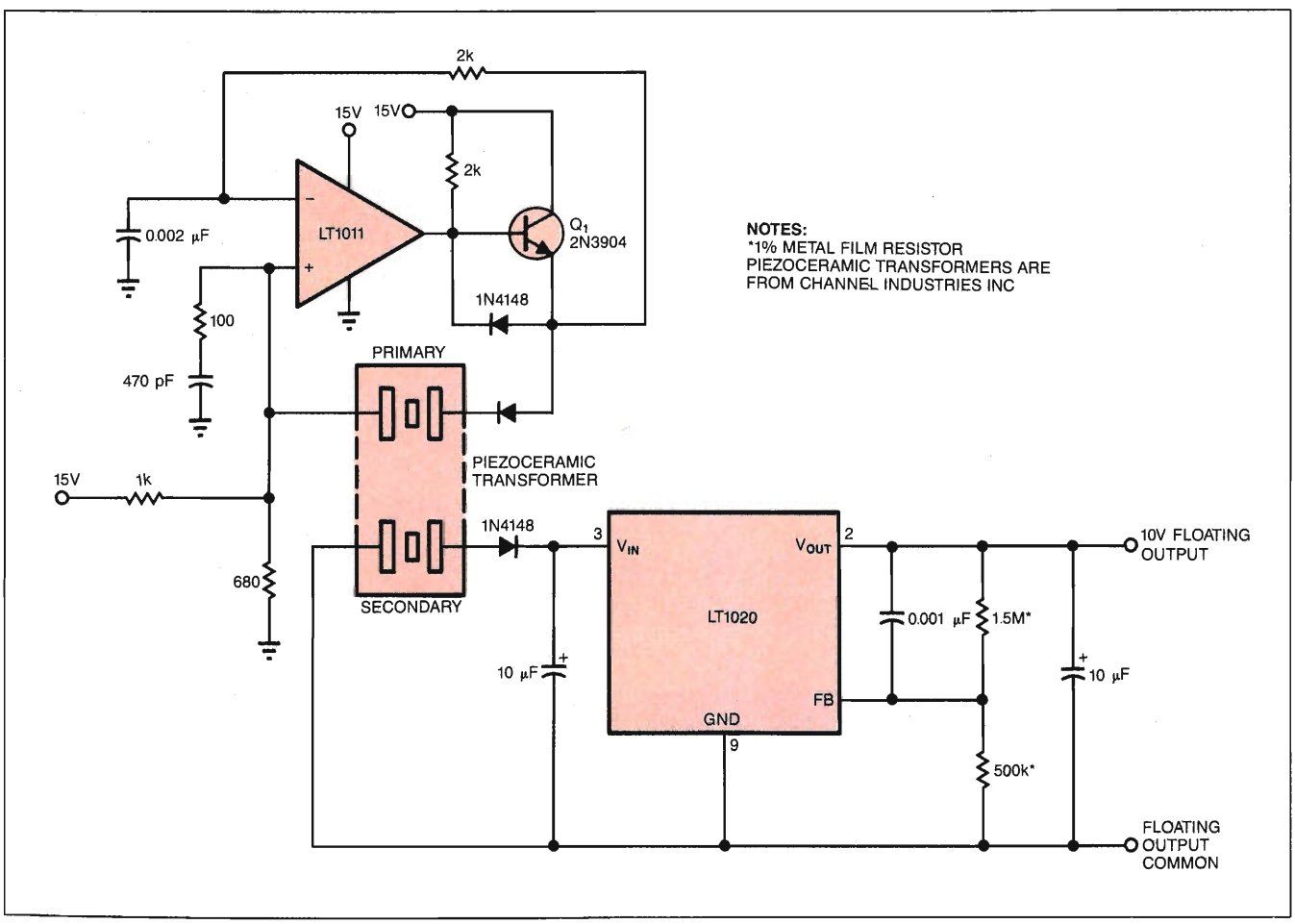


Fig 9—A ceramic-based design approach *proves to be a viable way to achieve the isolated transfer of appreciable amounts of electrical energy.*

similar to a quartz crystal. You must design drive circuitry to excite the device in the positive-feedback path of a wideband gain element.

In this design, unlike a design using a crystal, you must configure the drive circuitry so that a substantial amount of current passes through the ceramic, and you must maximize power in the transformer. In **Fig 9,** the piezoceramic transformer is in the LT1011 comparator's positive feedback loop. Q_1 serves as an active pull-up for the open-collector LT1011 device. The 2-kΩ/0.002-μF path biases the LT1011's inverting input.

Positive feedback occurs at the transformer's resonance frequency, and oscillation commences. The transformer, like a quartz crystal, has significant harmonic and overtone modes. The 100Ω/470-pF damper circuit suppresses spurious oscillations and mode hopping. The transformer appears as a highly resonant filter to the resultant wave that it propagates internally. The transformer's secondary voltage is sinusoidal.

The transformer also provides some voltage gain. The diode and the 10-μF capacitor convert the secondary voltage to dc. The LT1020 low-quiescent-current regulator provides a stabilized 10V output. This converter has an output-current capability of only a few milliamps, but you can improve this performance by devoting more attention to transformer design. EDN

Authors' biographies

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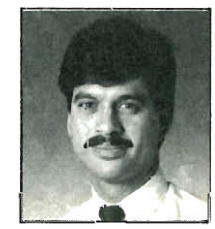

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Article Interest Quotient (Circle One)
High 497 Medium 498 Low 499

DESIGNER'S GUIDE

dc/dc converters
Part 4

Switched-capacitor networks simplify dc/dc-converter designs

This article, part 4 of a 4-part series, shows how to use switched-capacitor networks to replace inductors in dc/dc converters. Parts 1 through 3 of the series discussed the design of 5 to ±15V converters, the criteria for selecting proper instrumentation for converter design, and the design of power-conservative converters.

Jim Williams and Brian Huffman,
Linear Technology Corp

The inductor, a key component in a typical dc/dc converter, can negatively affect converter design and operation. The most common problem the inductor causes is saturation, a condition that can often result in destructive failure of the converter. The inductor also adds a number of negative factors to your design considerations—it's expensive, relatively large, and can be scarce, and it also has heat-related problems. Fortunately, you can sometimes replace the inductor without affecting your converter's performance. One way is to use a switched-capacitor network as an energy-storage element. Such a network can significantly simplify the dc/dc-converter-design process.

Back to basics

To understand the theory of switched-capacitor converter operation, it might help to review how a basic switched-capacitor building block (**Fig 1**) functions. In **Fig 1a,** C_1 charges to V_1 when the switch is in the left position. The total charge (q_1) on C_1 equals C_1V_1. When the switch moves to the right position, C_1 discharges to voltage V_2. The total charge (q_2) on C_1 will now equal C_1V_2.

Note that the switch action has transferred charge from the source (V_1) to the output (V_2). The total charge is:

$$q = q_1 - q_2 = C_1(V_1 - V_2).$$

If you cycle the switch f times per second, the charge transfer per unit time (current) is:

$$1 = fq = fC_1(V_1 - V_2).$$

If you rewrite this equation in terms of voltage and equivalent impedance, you wind up with an equivalent resistance for the switched-capacitor network:

$$1 = \frac{V_1 - V_2}{\frac{1}{fC_1}} = \frac{V_1 - V_2}{R_{EQUIV}}.$$

The new variable R_{EQUIV} is equal to $1/fC_1$.

Switched-capacitor converters such as the LT1054 have the same switching action as the basic switched-capacitor building block. Although the preceding simplified analysis doesn't consider parameters such as finite switch on-resistance and output-voltage ripple, it does provide an intuitive feel for how the device

Converters such as the LT1054 have the same switching action as does the basic switched-capacitor building block.

works. For example, the analysis explains voltage loss as a function of frequency. As frequency decreases, the $1/fC_1$ term will eventually dominate the output-impedance figure, and voltage losses will rise.

Note that losses also rise as frequency increases, because of internal switching losses resulting from the loss of some finite charge on each switching cycle. When multiplied by the switching frequency, this charge loss per unit cycle becomes a current loss. This loss is particularly significant at high frequencies.

The oscillators in practical converters are designed to run in a frequency band that will minimize these losses. **Fig 1c** is the block diagram of the LT1054. The LT1054 is a monolithic, bipolar, switched-capacitor voltage converter and regulator. Its adaptive drive scheme optimizes its efficiency over a wide range of output currents. Its total voltage loss at a 100-mA output current is typically 1.1V. This loss figure holds true over the full supply-voltage range of 3.5 to 15V. The part's quiescent-current drain is typically 2.5 mA.

When you combine it with an external resistive divider, the LT1054 provides a regulated output, which will withstand changes in input voltage and output current. The LT1054 can operate in a standby mode—at a quiescent current of only 100 μA—when you ground the feedback pin. The internal oscillator runs at a nominal frequency of 25 kHz. You can use the oscillator pin to externally adjust the oscillator frequency or to synchronize the LT1054's operation.

Getting rid of inductors

Most converters employ inductors simply because inductors can store energy. This stored magnetic energy, released and expressed in electrical terms, is the basis of dc/dc-converter operation. Inductors are not the only components that can store and efficiently release energy, however. Capacitors can store energy; thus, they can serve as the basic transfer element in dc/dc-conversion processes.

Fig 2a illustrates the inherent simplicity of a switched-capacitor-based dc/dc converter. The LT1054 provides clocked drive to charge C_1. A second clock

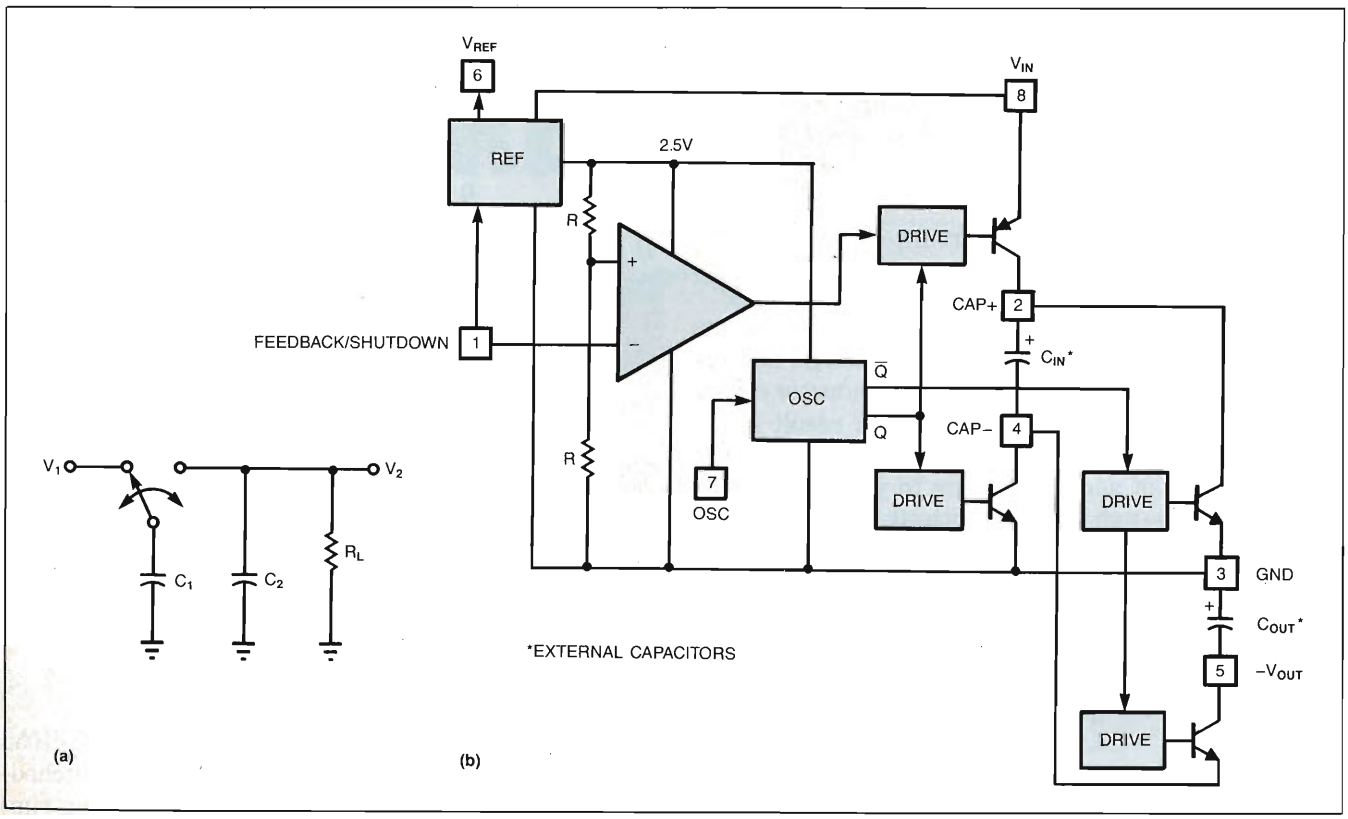

Fig 1—When the switch is in the left position, *the total charge on C_1 in a basic switched-capacitor building block* ***(a)*** *equals C_1V_1. When the switch moves to the right position, C_1 discharges to voltage V_2 and total charge on C_1 now equals C_1V_2. Switched-capacitor converters like the LT1054* ***(b)*** *have the same switching action as the basic switched-capacitor building block.*

phase discharges C_1 into C_2. The internal switching scheme is designed to flip C_1 during the discharge interval and produce a negative output at C_2. Continuous clocking allows C_2 to charge to the same absolute level as that of C_1. Junction losses and other losses preclude ideal results, but the circuit's performance is quite good. **Fig 2b** shows how well the circuit converts V_{IN} to $-V_{OUT}$.

By adding some external steering diodes, you can alter **Fig 2**'s circuit to develop a design that converts a negative input to a positive output **(Fig 3a)**. By modifying the circuit somewhat, you can develop a converter **(Fig 3b)** that transforms a 6V input into ±5V outputs. **Fig 3b**'s circuit is extremely flexible. If you provide some diode steering, the circuit will provide some voltage boost and develop an output of approximately $2 \times V_{IN}$.

Satisfying high power needs

By employing some discrete devices, the switched-capacitor converter in **Fig 4** can provide a 5W output (5V at 1A). The LTC1043 switched-capacitor building block provides nonoverlapping complementary drive to the four MOSFETs. The MOSFETs are arranged so that C_1 and C_2 are alternately in a series and a parallel configuration.

During the series phase, the 12V supply current

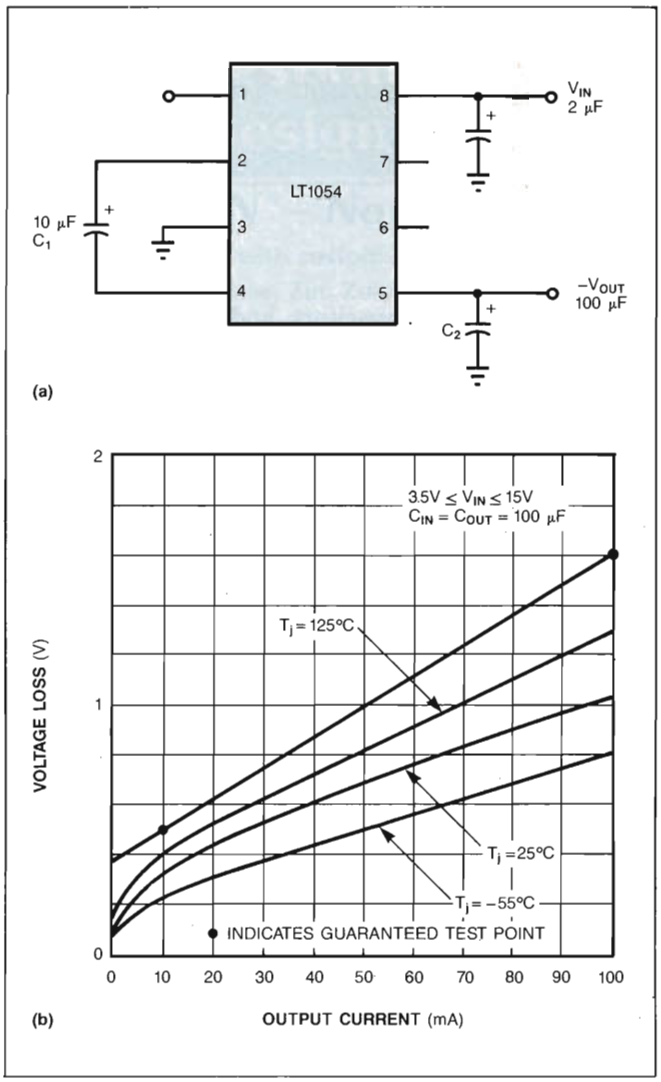

***Fig 2—Circuit simplicity is an inherent feature** of a switched-capacitor based dc/dc converter **(a)**. Despite its simplicity, this circuit does a good job of converting V_{IN} to $-V_{OUT}$ **(b)**.*

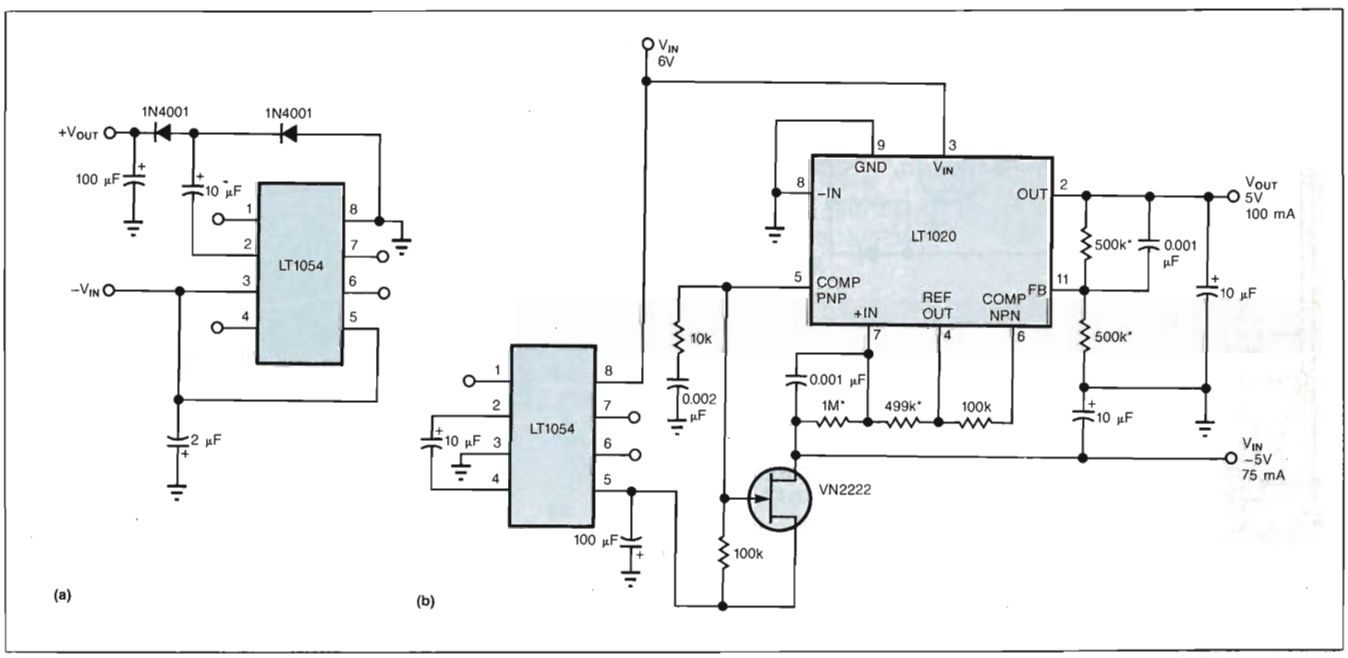

***Fig 3—By adding some steering diodes to Fig 2's circuit,** you can convert a negative input into a positive output **(a)**. By modifying the circuit somewhat **(b)**, you can develop a converter that transforms a 6V input into ±5V outputs.*

Capacitors can store energy; thus, they can serve as the basic transfer element in dc/dc-conversion processes.

flows through both capacitors and charges them to furnish load current. During the parallel phase, both capacitors work to provide half the load current. **Fig 4b** illustrates the LTC1043-supplied drive inputs to Q_3 and Q_4 (traces A and B, respectively). Q_1 and Q_2 receive similar drive inputs from pins 11 and 3 of the LTC0143. The diode-resistor networks ensure that the series-parallel phase switches see no simultaneous drive pulses.

If the circuit didn't include IC_1, its output would equal $V_{IN}/2$, but IC_1 and its associated components reduce the converter's output to 5V. When the circuit is in the series phase, the output has a rapid transition in the positive direction (trace C). When the output exceeds 5V, IC_1 trips and forces the LTC1043's oscillator pin high (trace D). This transition truncates the LTC1043's triangle-wave oscillator cycle.

The truncation forces the circuit into the parallel phase, and the output slowly diminishes until the beginning of the LTC1043's next clock cycle. IC_1's output diode ensures that any sharp transitions from the 180-pF capacitor will have no effect on the triangular down-

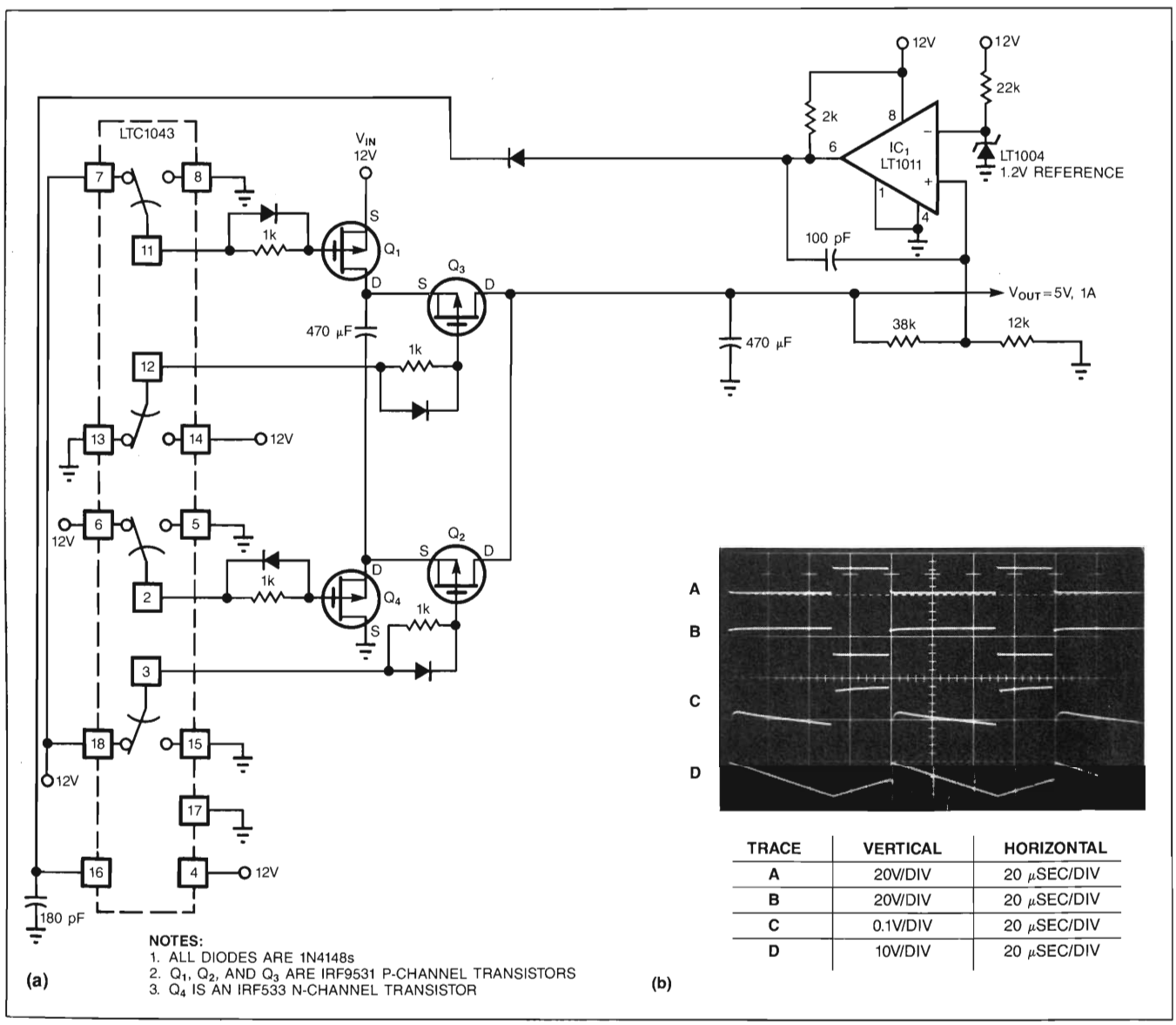

Fig 4—You can develop a high-power converter *by adding some discrete devices to the basic switched-capacitor circuitry* ***(a)****. The diode-resistor networks ensure that the series-parallel phase switches (Q_1 and Q_2) see no simultaneous drive pulses* ***(b)****.*

slope waveform. The feedback loop regulates the output by controlling the turn-off point of the series phase. The circuit's power MOSFETs easily handle any high transient currents, and the circuit's efficiency measures 83%. EDN

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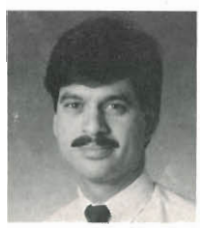
Authors' biographies

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art, and collecting antique scientific instruments.



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Article Interest Quotient (Circle One)
High 494 Medium 495 Low 496

Design linear circuits that serve digital system needs

Digital circuits require a slew of analog support circuits to provide life support in the real world. Many of these functions are related to memory support and range from power-sense circuits to voltage supplies for programming onboard, nonvolatile memories.

Jim Williams, *Linear Technology Corp*

The pristine, regimented symmetry of digital circuit boards is occasionally interrupted by irregular huddles of linear components. Designers tolerate these aberrants because they perform a variety of ancillary tasks necessary to keep the digital system running. Most analog designers wouldn't relish lifetime employment working on digital circuit boards, but the need for certain kinds of analog circuits exists. Memory- and power-control circuits are two examples of linear circuits needed in digital systems.

The recently introduced flash memories offer a good example of linear circuits supporting a predominantly digital function. Flash memory, unlike conventional EPROM, lets you erase and reprogram a memory chip electrically. A full-chip erasure takes one second with 100-μsec byte-program times and two seconds for full-chip programming. (See **box,** "A primer on flash memory," for a more complete description of flash memory.)

Flash-memory devices require carefully controlled, high-voltage programming power. A typical unit, the Intel 28F010 1M-bit flash memory, specifies V_{PP} pulses of 12 or 12.75±0.2V, depending on the part type. (PP stands for program power.) V_{PP} excursions beyond 14V for 20 nsec or longer will destroy the device. To reliably generate such pulses in a 5V-powered digital system, you must deal with several analog issues. You must derive or supply a high-voltage source and then control its output and the pulses generated from it within the tight tolerances required by the memory device. In addition, you may want to control the high-voltage pulses with a 5V logic command.

Memories require precise programming pulses

A simple way to provide the necessary programming power would be to use an existing high-voltage power-supply line or a switching-regulator output voltage set at the desired V_{PP} level. You could then use a simple, low-resistance FET or bipolar switch to generate the V_{PP} pulses. In theory, this approach will work. In practice, however, transmission-line effects in printed-circuit trace runs may cause memory-destroying overshoots. The **box,** "Preventing memory destruction," details this phenomenon.

In general, you need more sophisticated design techniques to stay within the V_{PP}-pulse tolerance limits. The circuit shown in **Fig 1a** meets almost all flash-

Whichever design world you find yourself in—analog or digital—you should be aware of the linear-circuit needs of different types of digital circuitry.

memory V_{PP} requirements. When the V_{PP} command pulse goes low (**Fig 1b,** trace a), the LT1072 switching regulator drives L_1, thus producing high voltage at the output. Resistors R_1 and R_2 provide the necessary dc feedback; the ac rise and fall times are controlled by the 2-pole compensation of the LT1072. This compensation is set by the values chosen for C_1, C_2, and R_3; these values have been selected for optimal compensation with respect to this application. The circuit's response should have no overshoot under any conditions including short-circuit recovery (see **Ref 1** for more information on LT1070/LT1072 compensation).

The final output of the circuit is a smoothly rising V_{PP} pulse (**Fig 1b,** trace b) that settles to either 12 or 12.75V, depending on the values you choose for R_1 and R_2. The 5.6V Zener diode permits the output to return to zero volts when the V_{PP} command pulse goes high; you may delete the diode in cases where a 4.5V minimum output is acceptable or desirable. You can eliminate circuit-trimming requirements by using precision resistors for R_1 and R_2. Alternatively, you can use 1% resistors and a trimmer for R_1 and R_2.

You can easily modify the circuit of **Fig 1a** to eliminate the 1N5919 Zener diode and its attendant power dissipation by inserting a pnp transistor in its place as shown in **Fig 2a**. To further modify the circuit for

A primer on flash memory

Saul Zales, *Intel Corp*

Flash memories reduce firmware-update costs for EPROM-based products. Such products often need software revisions, and EPROMs are costly to update. You often have to dismantle your equipment, either to UV erase and then reprogram the EPROMs or to replace them with new ones. This operation takes a technician at least 15 minutes. Double that time if you wait for UV erasure. In contrast, flash memories allow in-system reprogramming in seconds and are not discarded as EPROMs often are. In the factory, flash EPROMs let you execute multiple tests during a single board-testing step.

To distinguish between EEPROMs and flash EPROMs consider that EEPROMs suit parameter storage, as opposed to code storage. Parameters need to be rewritten individually in real time—that is, while the system is on-line and in normal operation. Parameters also require less memory storage space than code does.

In contrast, flash EPROMs better match embedded-code needs. Even if you only change one line of code, an entirely new microcomputer program results. You must update the software as a complete copy to ensure error-free updating. Flash memories accomplish this process with full-chip erase characteristics in a few seconds of off-line system time.

One flash-EPROM reprogramming method is In-System-Write (ISW). ISW eliminates external programming equipment altogether; it uses an existing data-communication channel, such as a modem. ISW utilizes the embedded, local CPU for the flash-memory device's reprogramming "intelligence," thus taking advantage of the off-line nature of updates. The only new requirement for ISW is a local programming power supply (V_{PP}) of either 12 or 12.75V, depending on device specifications.

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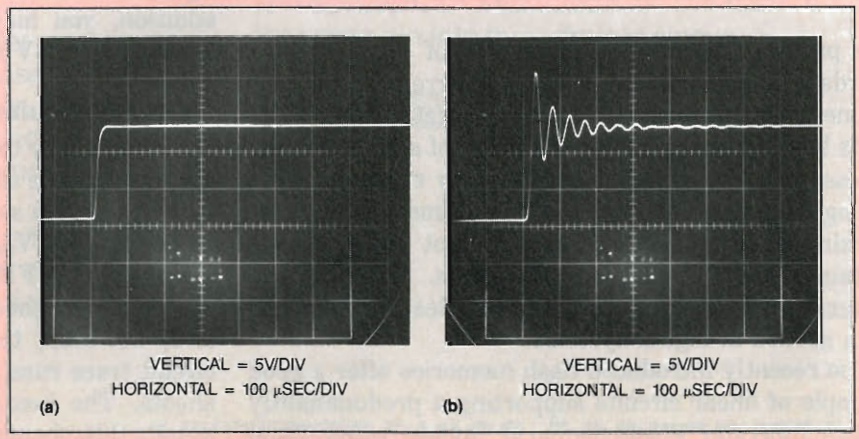
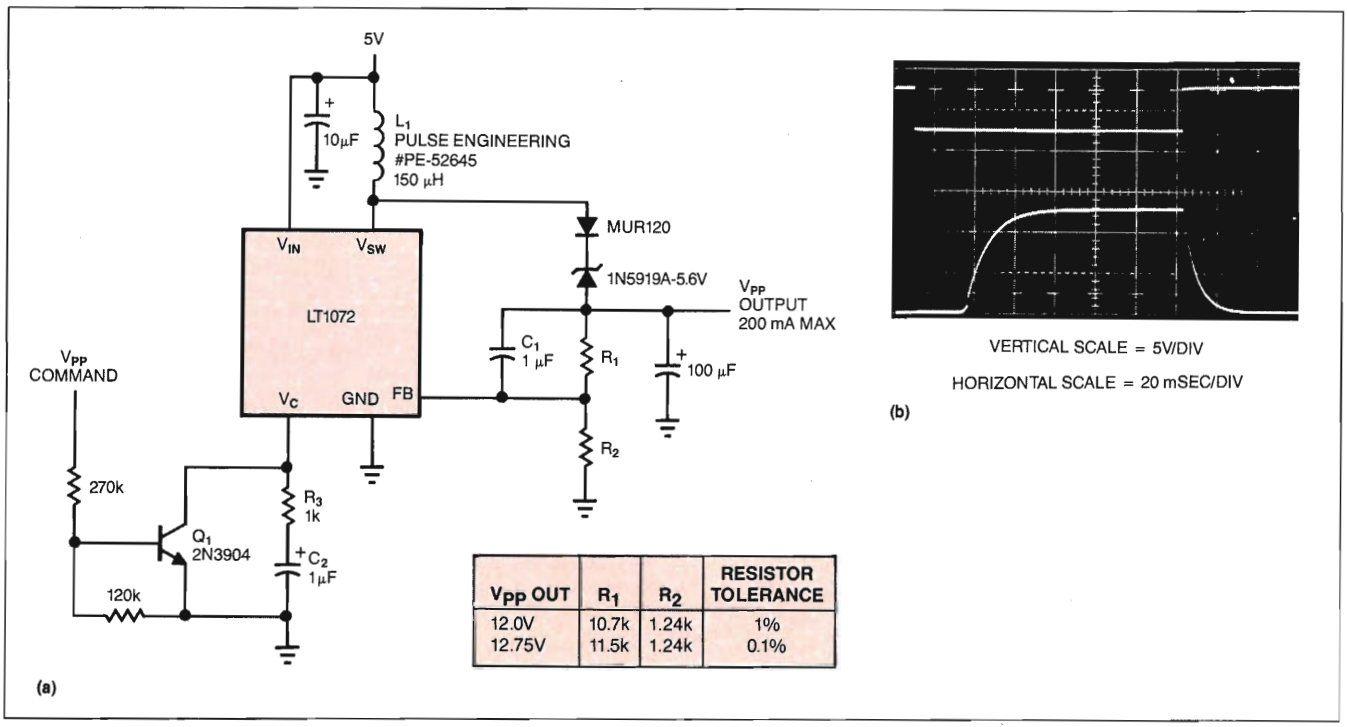


***Fig A—An ideal flash EEPROM V_{PP} pulse** has a smooth rise time with no overshoot (**a**). If your pulse-generator design doesn't include circuitry for rise-time control, the pulse can ring at destructive voltages (**b**) simply due to transmission along a pc trace.*



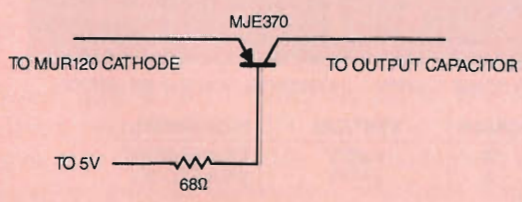
VPP OUT	R1	R2	RESISTOR TOLERANCE
12.0V	10.7k	1.24k	1%
12.75V	11.5k	1.24k	0.1%

Fig 1—High-voltage pulses with smooth rise characteristics *are the basic flash-memory programming requirements that this circuit* ***(a)*** *fulfills. Due to the compensation of the LT1072 switching regulator, the command pulse (****b****, trace A) produces a pulse with a clean rise-time characteristic (****b****, trace B).*

high power outputs, see the table in **Fig 2b**.

A key feature of the circuit in **Fig 1a** and many circuits similar to it is that they will not spuriously overshoot during power-up or power-down, thereby preventing memory destruction. This feature is due to the compensation of the LT1070, which causes a highly overdamped pulse response, and to the fact that the control components of these circuits function even at low supply voltages. In other words, the control circuits will be active long before the memory circuits settle and will prevent uncontrolled V_{PP} outputs.

The repetition rate of the circuit in **Fig 1** is limited because the regulator must fully rise and settle for each V_{PP} command. Depending on how often your memory devices require updating, this limited repetition rate may or may not present a problem. Most requirements are for low repetition rates (from one hertz to the kilohertz range), but there are cases where the pulser is required to serve many memories. The circuit in **Fig 3** serves those cases that require higher-



POWER OPTIONS FOR BASIC V_{PP} PULSE GENERATOR

OUTPUT CURRENT	C_{OUT}	REGULATOR	INDUCTOR	ZENER
400 mA	200 μF	LT1071	PE-52645	1N5339A OR SYNCHRONOUS SWITCH OPTION
800 mA	400 μF	LT1070	PE-51516	1N5339 OR SYNCHRONOUS SWITCH OPTION

(b)

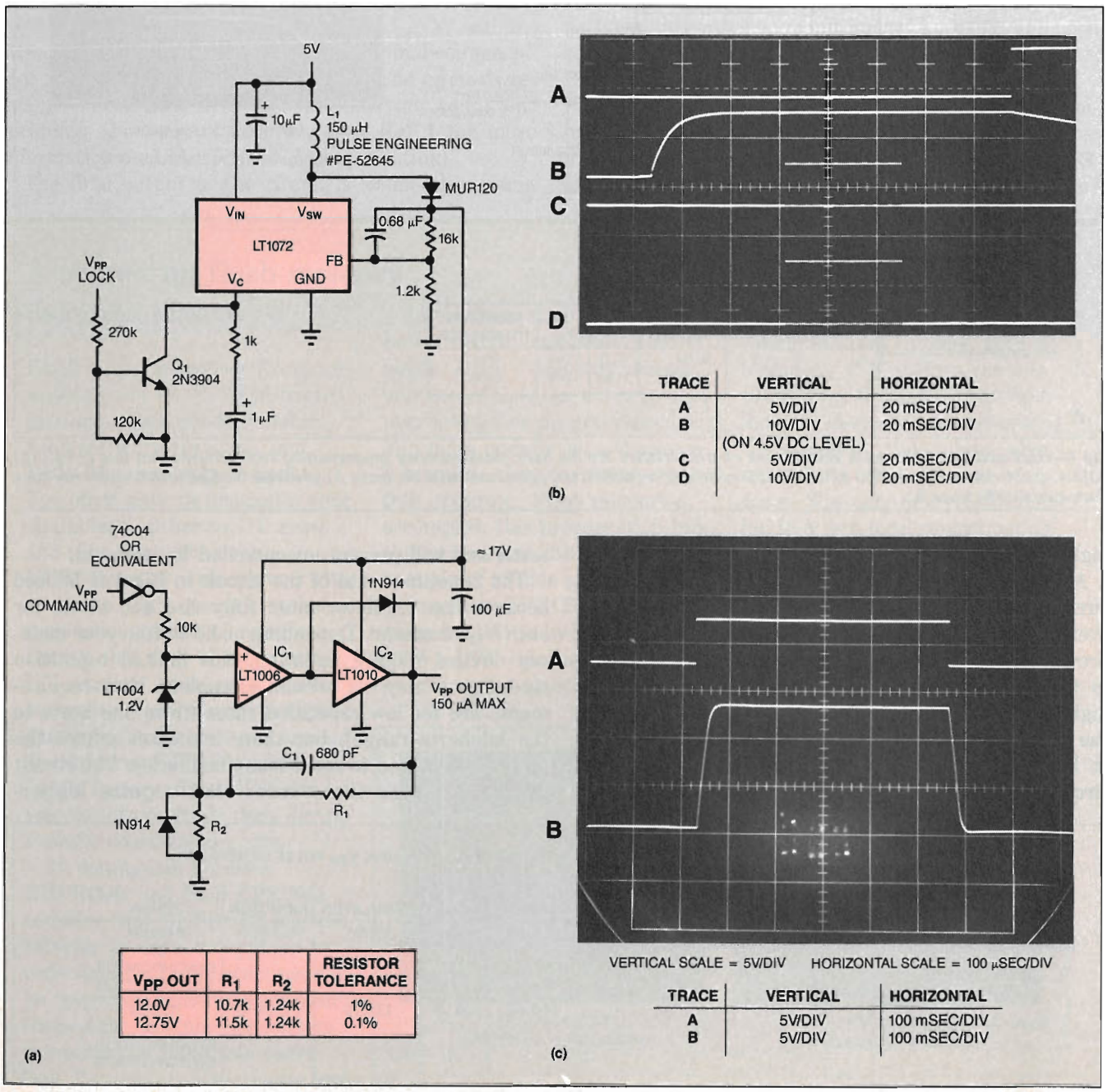
NOTE: ASSUME EACH 28F010 DEVICE REQUIRES 30 mA of VWF CURRENT

Fig 2—You can replace the Zener diode of Fig 1 *with a pnp transistor* ***(a)****. You can also modify* ***Fig 1*** *for higher power outputs* ***(b)****.*

Power control and memory management are just two areas where some analog design tricks will come in handy on a digital circuit board.

repetition-rate V_{PP} pulses. In this design, the switching regulator runs continuously. You provide a V_{PP} command pulse to drive an op-amp (IC_1) and buffer-amplifier (IC_2) loop, which generates the required pulses.

The waveforms in **Fig 3b** demonstrate the circuit's operation. You can drive the V_{PP} lock line to a logic high, which will shut down the regulator, thus preventing any possiblility of inadvertent V_{PP} outputs. After the V_{PP} lock goes low (trace A), the LT1072 loop comes



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	20 mSEC/DIV
B	10V/DIV (ON 4.5V DC LEVEL)	20 mSEC/DIV
C	5V/DIV	20 mSEC/DIV
D	10V/DIV	20 mSEC/DIV

V_{PP} OUT	R_1	R_2	RESISTOR TOLERANCE
12.0V	10.7k	1.24k	1%
12.75V	11.5k	1.24k	0.1%

VERTICAL SCALE = 5V/DIV HORIZONTAL SCALE = 100 µSEC/DIV

TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	100 mSEC/DIV
B	5V/DIV	100 mSEC/DIV

Fig 3—To fulfill higher-repetition-rate voltage-programming requirements, *you can run a switching regulator continuously and generate the V_{PP} pulses by using an op amp and a buffer amplifier* ***(a)****. High-voltage pulses, whose level is dependent on the value you choose for R_1 and R_2, result from the application of the V_{PP} command pulse* ***(b,*** *trace D); these pulses exhibit clean rise times* ***(c,*** *trace B).*

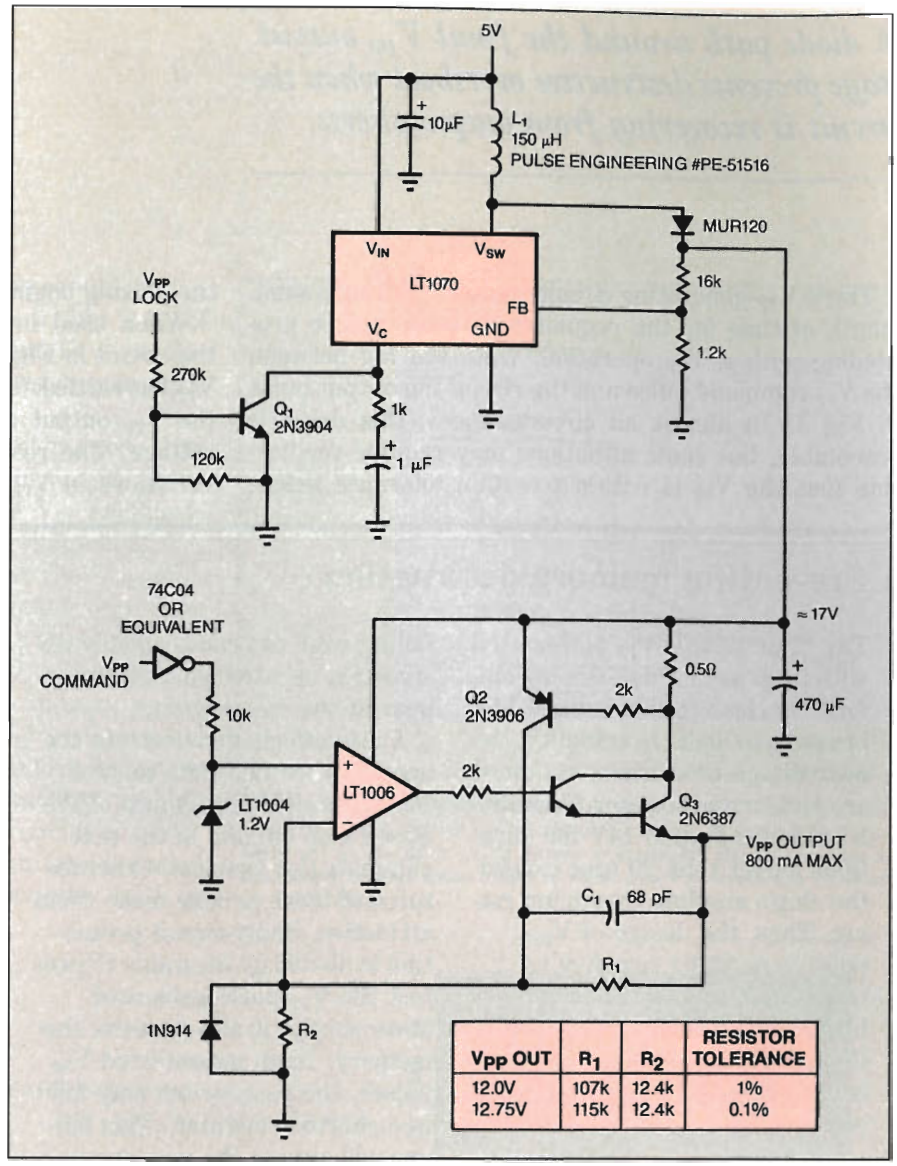


***Fig 4—By replacing the buffer-amplifier stage of Fig 3** with a discrete-output stage, you can supply up to 800 mA of output current.*

on (trace B), stabilizing at about 17V. Pulsing the V_{PP} command line then causes the 74C04's output (trace C) to bias the LT1004 reference. The LT1004 clamps at 1.23V, and the gain loop containing IC_1 and IC_2 produces a pulsed output voltage dependent on the values you choose for R_1 and R_2 (trace D). The 680-pF feedback capacitor, C_1, controls loop slewing, thereby eliminating overshoots. **Fig 3c** details the V_{PP} output. Trace A is the 74C04 output; trace B displays the clean V_{PP}-pulse characteristics.

As in **Fig 1**, the 2-pole compensation of the LT1072 in **Fig 3a** ensures a clean rise time, and spurious V_{PP} outputs are suppressed during power-up and power-down. The LT1010 buffer amplifier provides short-circuit protection and 150 mA of drive current, which is enough for five 28F010s. The diode path around the LT1010 prevents destructive overshoot when the circuit is recovering from output shorts. The diode at IC_1's input clips excessive negative voltages arising from C_1's differentiated response.

To drive more memory devices—supply more output current—you can modify the circuit in **Fig 3a** by replacing the LT1010 buffer amplifier with a discrete power stage, as shown in **Fig 4**. Q_3 furnishes up to 800 mA of output current, enough to drive 26 28F010 memories; Q_2 functions to limit the current to a maximum of approximately 1.2A. The values of the feedback components used in **Fig 3a** have been scaled by a factor of 10; R_1 and R_2 were increased and C_1 was decreased to maintain the same level of compensation. These changes prevent Q_2's collector current from causing excessive heating in the grounded resistor, R_2. This heating could occur during prolonged short-circuit conditions. The ac dynamics of the circuit in **Fig 4**, including a glitchless short-circuit recovery, are identical to those of the circuit in **Fig 3a**.

You should note that for both **Fig 3a** and **Fig 4** the LT1070 or LT1072 is running continuously to provide a fixed high voltage. If a suitable high voltage is already available in your system, you can power IC_1 and IC_2 directly from that high-voltage line and delete the regulators from the circuit.

A diode path around the final V_{PP} output stage prevents destructive overshoot when the circuit is recovering from output shorts.

These V_{PP}-generating circuits require waiting a small length of time for the regulator to settle before proceeding with a V_{PP} operation. Note the lag between the V_{PP} command pulse and the rise of the output pulse in **Fig 1**. In almost all circumstances, this delay is acceptable, but some situations may require verification that the V_{PP} is within a certain tolerance before the pulsing begins.

When used in conjunction with either V_{PP} pulser, the circuit in **Fig 5** gives a handshake output when the V_{PP} has settled. This simple circuit works by comparing the V_{PP} output against the known LT1004 reference voltage. The resistor values given allow for possible variations in V_{PP} voltage due to component tolerance

Preventing memory destruction

The 12 or 12.75V V_{PP} pulses used with flash memories seem uncomfortably close to the devices' 14V breakdown limit. In actuality, the overvoltage precautions required are similar to those for 5V rails. Excursions beyond 14V for durations longer than 20 nsec exceed the chip's absolute maximum rating. Thus, the design of V_{PP}-pulse-generating circuitry requires care to avoid seemingly mysterious memory failures. Although the 28F010 flash memory is used here as an example, the considerations are applicable to other devices.

In theory, a simple low-loss transistor switching a low-impedance power supply will generate the required pulses. In practice, this is a hazardous approach. **Fig Aa** shows an ideal V_{PP} pulse produced by simple transistor switching. The pulse settles to the desired V_{PP} level quickly with no overshoots or aberrations. **Fig Ab** shows the same pulse measured at the memory pins after a printed-circuit trace run. The pc trace looks like an unterminated transmission line with ill-defined characteristics. Reflections occur, which cause ringing exceeding 20V. This ringing is well beyond specified destructive levels and almost guarantees chip failures. Similar overshooting on the falling edge can cause equally destructive negative voltages to appear at the memory pins.

These effects demonstrate the necessity for rise-time control. The controlled edge times of the closed-loop circuits in the text eliminate this problem. Other features of these circuits make them attractive. Short-circuit protection is obviously desirable to protect the V_{PP}-pulse generator. More subtly, it also protects the memory. In an unprotected V_{PP} pulser, the pass switch may fail in a shorted condition. This failure will expose the memory to destructive overvoltage. You should design short-circuit-protection circuitry so that it does not cause overshoots when operating or recovering from overload.

For example, removing IC_2's shunt diode from the circuit shown in **Fig 3** in the text causes dangerous overshoots on short-circuit recovery. **Fig Ba** shows V_{PP} output recovery with the diode removed. With the diode in place (**Fig Bb**), the recovery is free from overshoot. Similar considerations apply on power-up and power-down. The V_{PP} generator must not produce spurious outputs during power application or removal. You can avoid these unwanted outputs by employing circuit techniques and ICs that operate down to low voltage. Circuits that provide control even when the power supply is not yet at its specified operating level yield predictable and controllable outputs during transient supply conditions.

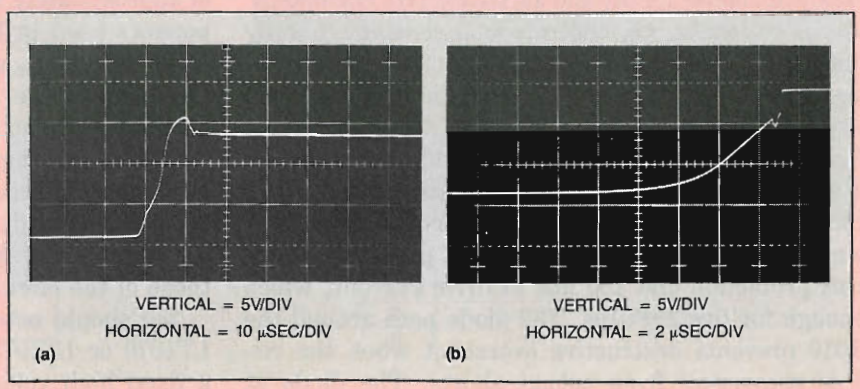


Fig B—Without a shunt diode at the output *of a V_{PP}-pulse generator, dangerous memory-destroying overshoots can occur (**a**). With the diode in place, the recovery is smooth and controlled (**b**).*

stack-up. When you use this circuit, you should set the output of the V_{PP} generator circuit to within 0.4% of nominal value. You can set the output to a precise value by trimming or by using 0.05% resistors in place of the 0.1% values specified.

Although EEPROMs fulfill a different purpose than flash memories, their V_{PP}-pulse requirements have similarities. The Intel 2816 specifies a V_{PP} amplitude of 21 ± 1V with a maximum allowable voltage of 22.5V. A special EEPROM stipulation is that the V_{PP}-pulse rise time must have an RC time constant very close to 600 μsec. The circuit in **Fig 6** meets these requirements. As in the circuit in **Fig 3**, an LT1072 switching regulator generates the high supply voltage; an op amp (IC_1) and a buffer amplifier (IC_2) generate the actual V_{PP} pulse. While the Erase/Write lock line is low (**Fig 6b**, trace A), the LT1072 is in standby; no high voltage is produced, and there is no circuit activity. Under these conditions, the V_{PP} output line is pulled toward 5V via the 1N914 diode. (Note the 4.5V dc

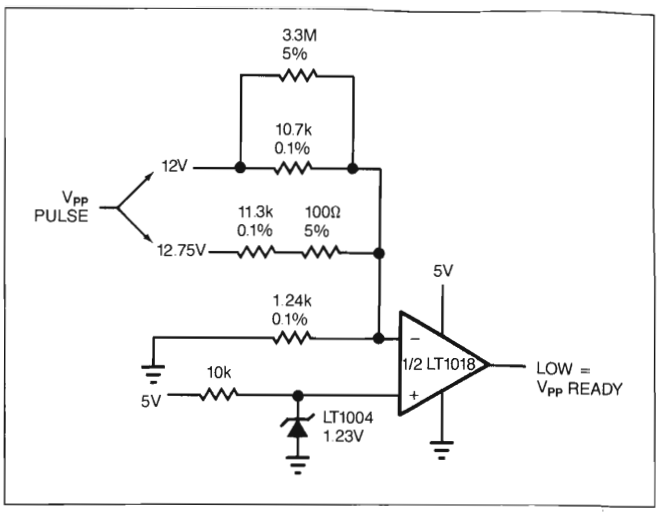
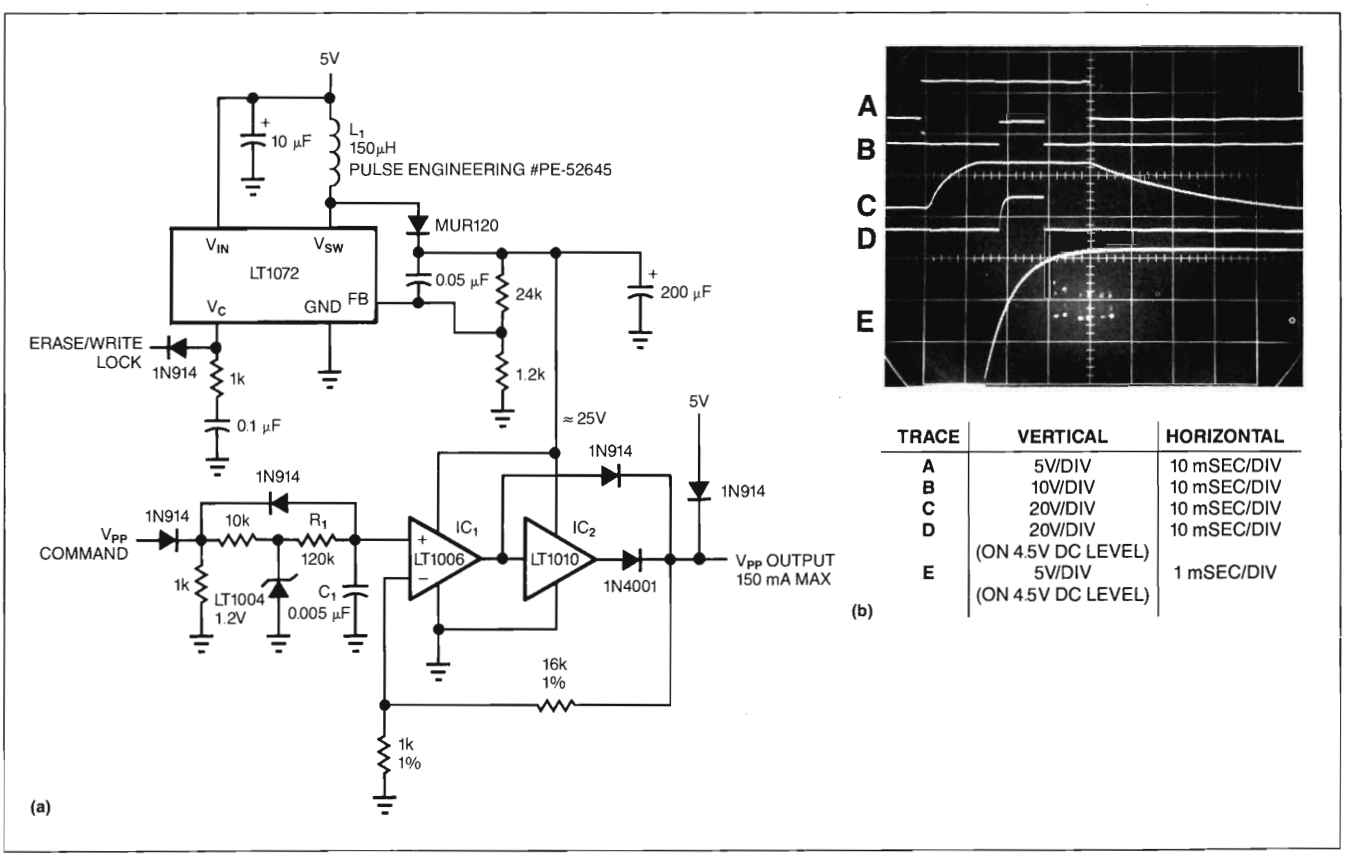


***Fig 5—Switching-regulator-based circuits require** that you wait a certain length of time for the regulator output to settle before you begin a V_{PP} operation. This simple comparator circuit provides a handshake output when either of these two V_{PP} levels has reached its final value.*



TRACE	VERTICAL	HORIZONTAL
A	5V/DIV	10 mSEC/DIV
B	10V/DIV	10 mSEC/DIV
C	20V/DIV	10 mSEC/DIV
D	20V/DIV (ON 4.5V DC LEVEL)	10 mSEC/DIV
E	5V/DIV (ON 4.5V DC LEVEL)	1 mSEC/DIV

***Fig 6—EEPROM high-voltage programming requirements** are similar to those of flash memory. EEPROMs require 21V amplitude pulses with RC time constants of 600 μsec. A simple modification of **Fig 3**'s input **(a)** provides rise-time control via R_1 and C_1. By choosing R_1 and C_1 so that their product equals 600 μsec, the output-pulse conditions are met (**b**, trace E).*

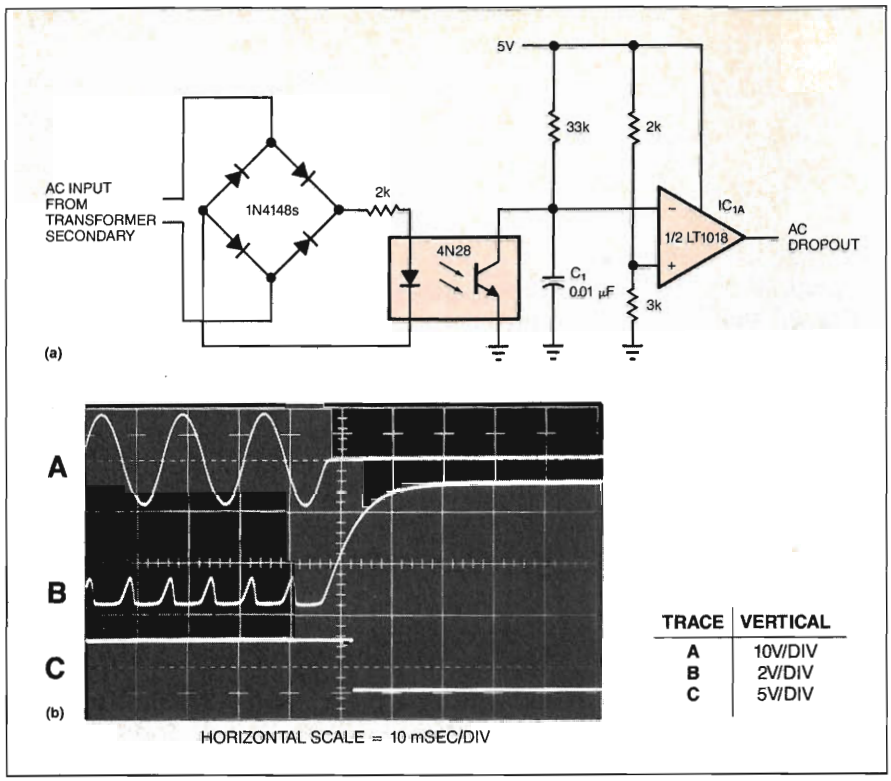


Fig 7—Dropout detection enables you to issue *memory-store commands before power fails. This ac detector uses an optoisolator connected across the secondary of a transformer to continually reset C_1 (**b**, trace B). When power fails, C_1 charges up and triggers the comparator (**b**, trace C).*

level on traces D and E of **Fig 6b.**)

When the Erase/Write lock line goes high (trace A), the regulator output (trace C) builds smoothly and regulates at 25V. The 2-pole LT1072 compensation allows the regulator output to rise relatively quickly. When the V_{PP} command line is pulsed high (trace B), the LT1004 reference clamps at 1.23V, and the RC network made up of R_3 and C_1 delivers a 600-µsec edge to IC_1's positive input. The feedback-resistor values chosen produce 21V at the V_{PP} output (trace D). The 21V amplitude is ensured by the LT1004 reference and closed-loop operation. Trace E is a time- and amplitude-expanded version of this pulse.

When the V_{PP} command goes low, the V_{PP} output returns cleanly to 4.5V. The shunt diode at IC_1's noninverting input speeds the recovery of the 0.005-µF capacitor. IC_2 provides 150 mA of output current, enough to drive 10 2816 EEPROMs. As in **Fig 3**, a shunt diode

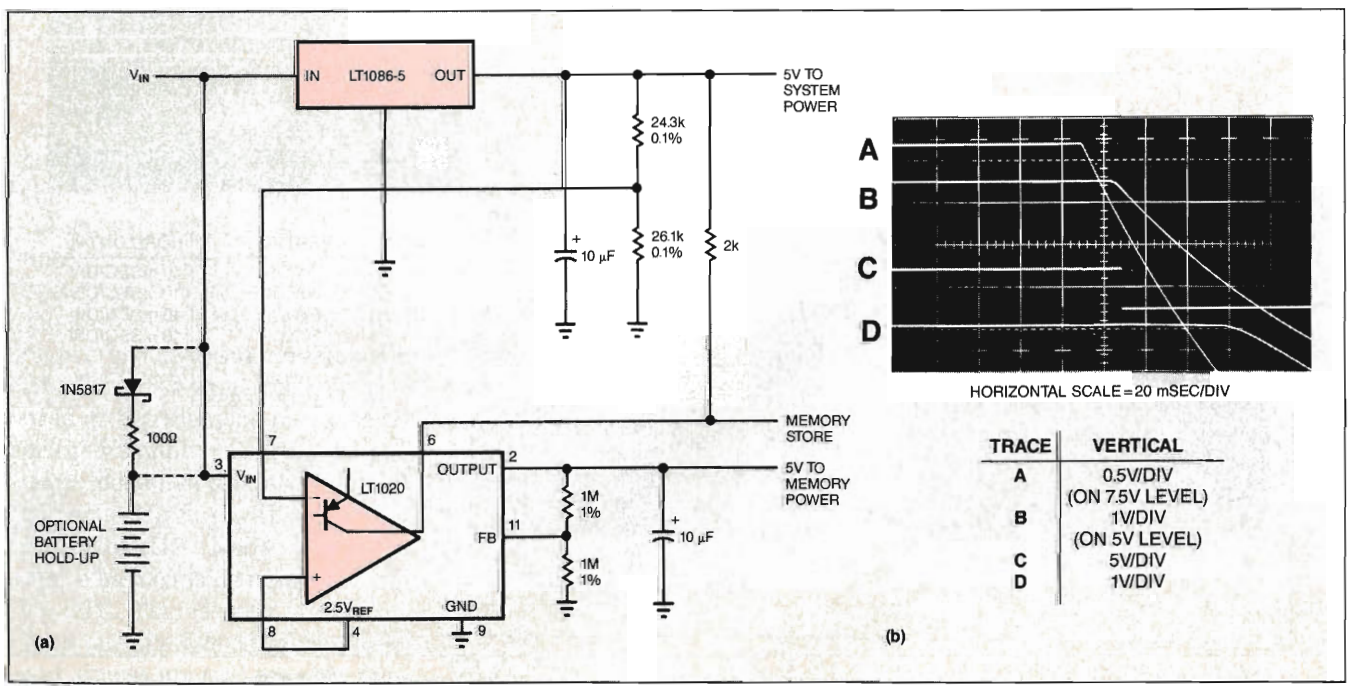


Fig 8—By making use of two 5V dc regulators (a), *you can alert the memory section to store data (**b**, trace C) before the memory power fails (trace D).*

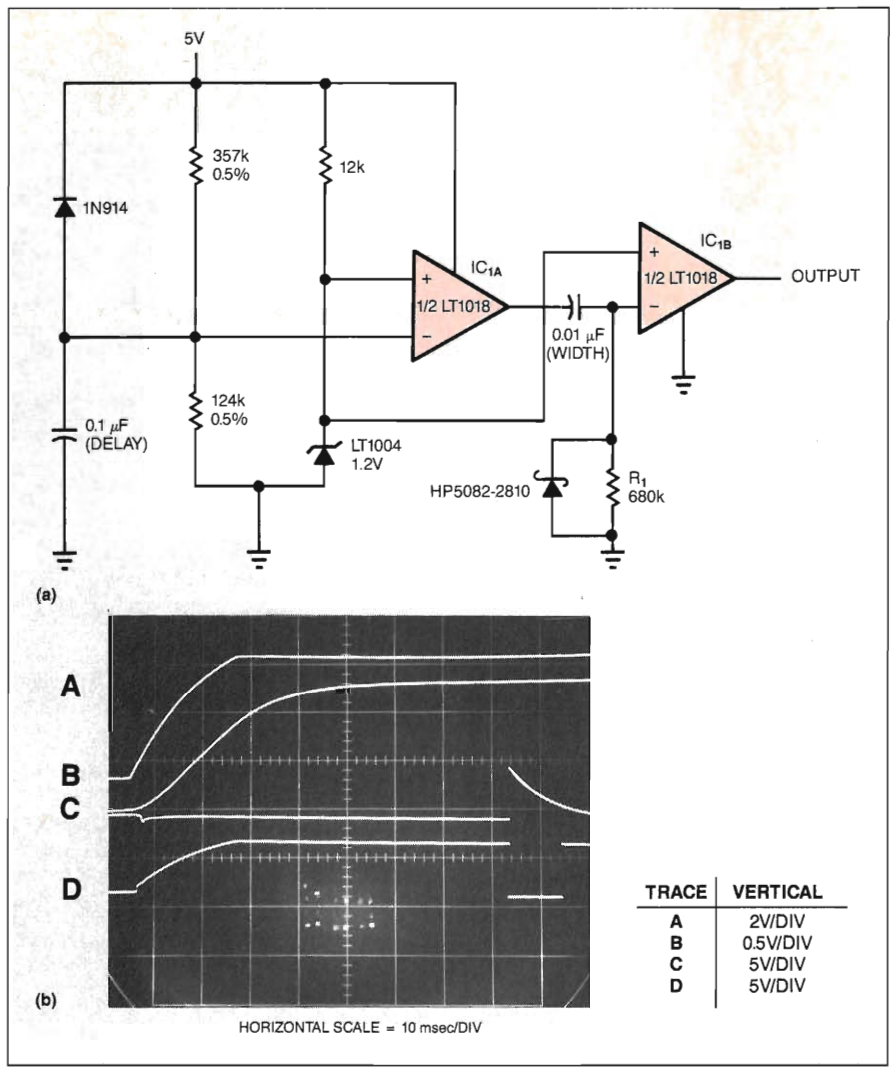


Fig 9—The flexible power-on-reset circuit *shown in* ***a*** *lets you modify the delay between the power onset and the pulse-onset trigger (***b****, trace C). The circuit also lets you modify the reset pulse-width by changing R_1 and C_1 (****b****, trace D).*

around the LT1010 prevents overshoot when the circuit is recovering from output shorts. When the Erase/Write lock line returns low, the regulator's output decays toward zero. As with the other V_{PP} circuits, this design does not produce undesired outputs during power-up or power-down.

Digital systems driven from the ac power line often require dropout detection. You'll want to implement fast ac line dropout detection in order to issue a memory-store command before the dc power falls. The circuit in **Fig 7** detects ac dropout by connecting an optoisolator across the power transformer's rectified secondary. Under normal power conditions, the ac line (**Fig 7b,** trace A) turns on the LED every 8 msec, or ½ cycle of the line. This repetitive action causes the output transistor to continually discharge the 0.01-µF capacitor (trace B). However, when the ac line drops out, the capacitor charges via the 33-kΩ resistor. IC_{1A} compares the resultant ramp voltage to a 5V supply-derived reference. In this case, the 2-kΩ and 3-kΩ resistors bias IC_{1A} to go low (trace C) within one cycle of ac line dropout.

In many cases, you won't have access to the ac power line. Such cases include PC add-on memory applications and battery-powered systems in which there simply isn't any ac power available. When ac line dropout detection isn't feasible, you'll have to implemement a dc-sensing circuit, such as the one shown in **Fig 8a.** This circuit uses the different dropout voltages of two regulators. Under normal operating conditions, the LT1086 supplies 5V power to the main system, and the LT1020 drives the memory section.

When the input power falls (**Fig 8b**, trace A), the LT1086 drops out first (trace B). This voltage change is detected by the LT1020's onboard auxiliary comparator, which then goes low (trace C). This action alerts the memory section to store data. The LT1020 regulator output (trace D) maintains memory power for an additional amount of time due to its low-dropout characteristics. The LT1020's output begins to fall approximately 50 msec after the memory-store command. You can include the optional battery and diode as shown in **Fig 8a** to extend the holdup time.

In addition to these power-fail circuits, digital systems often require power-up circuitry, such as power-on-reset. When supply power is applied to the circuit in **Fig 9a,** the 5V rail comes up (**Fig 9b**, trace A). The LT1004 clamps at 1.2V, and IC_{1A}'s positive input (trace

B) ramps at a time constant determined by the 0.5% resistors and the 0.1-μF capacitor. When IC_{1A}'s positive input ramps beyond the LT1004 potential, its output goes high, which delivers a differentiated pulse to IC_{1B}'s negative input (trace C). IC_{1B}'s output (trace D) then goes low for a period determined by the differentiator made up of R_1 and C_1. This pulse is used for system reset.

The 1N914 quickly resets the 0.1-μF delay capacitor, and the Schottky diode clips differentiator-caused negative voltages at IC_{1B}'s input. The ratio of the 0.5% resistors determines the turn-on threshold, in this case 4.8V. The output-pulse delay time—the time at the onset of the pulse in relation to the 5V rail—is controlled by the 0.1-μF capacitor; you can vary the delay time by changing the value of the capacitor. Similarly, the RC combination at IC_{1B} sets the output pulse width and may be similarly varied. As previously discussed, the LT1018's 1.2V minimum supply voltage prevents spurious output during supply power-up. EDN

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Author's biography

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art, and collecting antique scientific instruments.

Astute designs improve efficiencies of linear regulators

Linear voltage regulators outperform switching-type devices in many applications, but they have one major drawback—poor efficiency. By employing careful design techniques and using new regulator components, you can greatly improve efficiencies.

Jim Williams, *Linear Technology Corp*

Although switching-type voltage regulators are gaining in popularity, linear voltage regulators are still popular devices. Linear regulators are easy to implement and have much better noise and drift characteristics than switchers. In addition, they function with standard magnetics, are easy to compensate, don't radiate RF, and have fast response times. However, linear regulators are saddled with one major drawback—poor efficiency. As a result, they're associated with high operating temperatures and large heat-sink requirements. Linear regulators cannot compete with switching regulators in these performance characteristics, but by using certain design techniques and new linear-regulator devices, you can achieve significantly better results than you might think is possible.

A basic way to improve the efficiency of linear regulators is to minimize the input-to-output voltage across the regulator. The smaller this term is, the lower the power loss. Manufacturers refer to the minimum input-output voltage necessary to support regulation as the dropout voltage. Different regulator design techniques and technologies offer different regulator performance (see **box,** "Achieving a low dropout voltage"). Conventional 3-terminal linear regulators typically have a 3V dropout, but newer devices feature a 1.5V dropout at 7.5A and a 0.05V dropout at 100 μA. You can use these new regulators to achieve relatively high efficiencies. However, the overall regulator performance depends greatly on the quality and amplitude of the input signal.

Stable inputs ease problems

Lower dropout voltage leads to significant power savings when the input voltage is relatively constant—that is, when a linear regulator postregulates a switching-power-supply output (**Fig 1**). Here, feedback to the switching regulator stabilizes the main output, A. Output A usually supplies most of the power available from **Fig 1**'s circuit. Therefore, the power demands at the B and C outputs have relatively little effect on the amount of energy in the transformer.

Because of this action, the input voltages to the B and C regulators are relatively constant. Judicious design enables the regulators to run at or near their dropout voltage, regardless of the loading or switcher input voltage. Low-dropout regulators thus save considerable power.

Unfortunately, not all applications boast a stable input voltage. **Fig 2** illustrates a classic situation in which

You can improve the efficiency of a linear regulator by minimizing the input-to-output voltage across the device.

the ac line drives the linear regulator through a step-down transformer. A 90 to 140V ac swing (brownout to high-line range) causes a proportionate change at the regulator input. The efficiencies of standard regulators versus low-dropout devices can vary considerably under such circumstances.

A low-dropout regulator has much higher efficiency on its 5V main output, where dropout figures can be a significant percentage of the output voltage. An efficiency comparison at a 15V output still favors the low-dropout regulator, although the gain in efficiency is not as great as that of a standard regulator. A look at power dissipation under the same output conditions shows that a low-dropout regulator requires less heat-sink area than a normal regulator to maintain the same die temperature. Input voltage variations have a deleterious effect on the efficiencies of both regulators, but a low-dropout regulator clearly cuts power losses.

Fig 3 shows a way to minimize regulator input variations even though the ac line has a wide voltage swing. This preregulator circuit combined with a low-dropout regulator provides high efficiency but still retains the desirable characteristics of a linear regulator.

This circuit servo controls the firing point of the SCRs to stabilize the LT1086 input voltage. IC_1 compares a portion of the LT1086's input voltage to the LT1004 reference. The amplified difference voltage at IC_1's output drives the inverting input of IC_{2B}. The circuit then compares IC_{2B}'s output to a line-synchronous ramp derived by IC_{2A} from the rectified secondary of the main transformer, T_1.

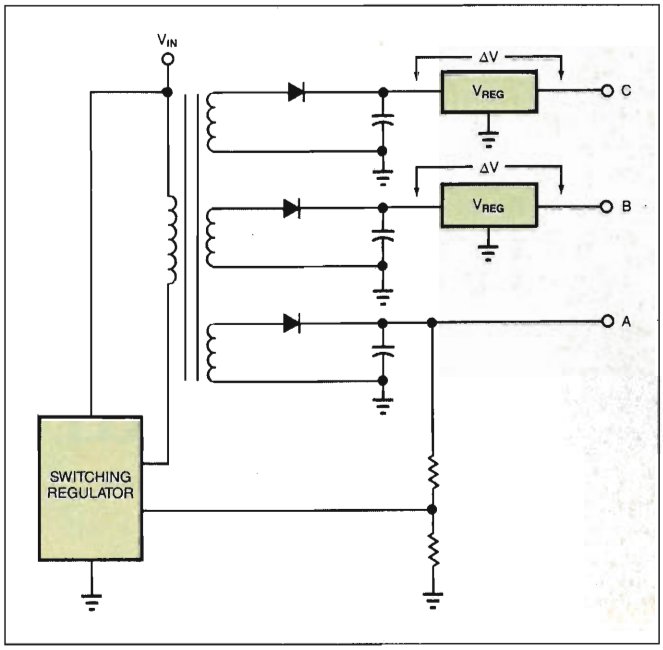

Fig 1—You can realize significant power savings *in applications in which the input voltage is relatively constant. In this circuit, a linear regulator postregulates a switching-power-supply output.*

The pulse output from IC_{2B} fires the appropriate SCR to develop a current flow from the transformer through L_1. This current flow charges the 4700-μF capacitor. When the transformer output drops low enough, the SCR commutates and charging stops. On

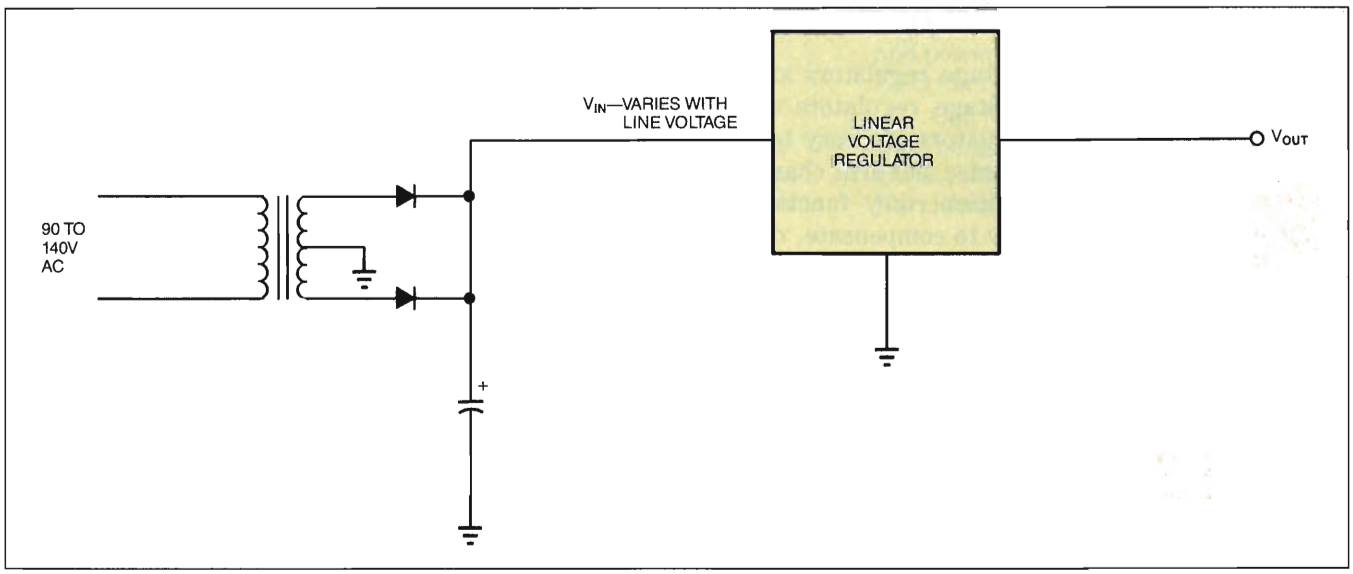

Fig 2—Achieving high efficiencies is difficult *when the input to the linear regulator varies in proportion to any line-voltage changes.*

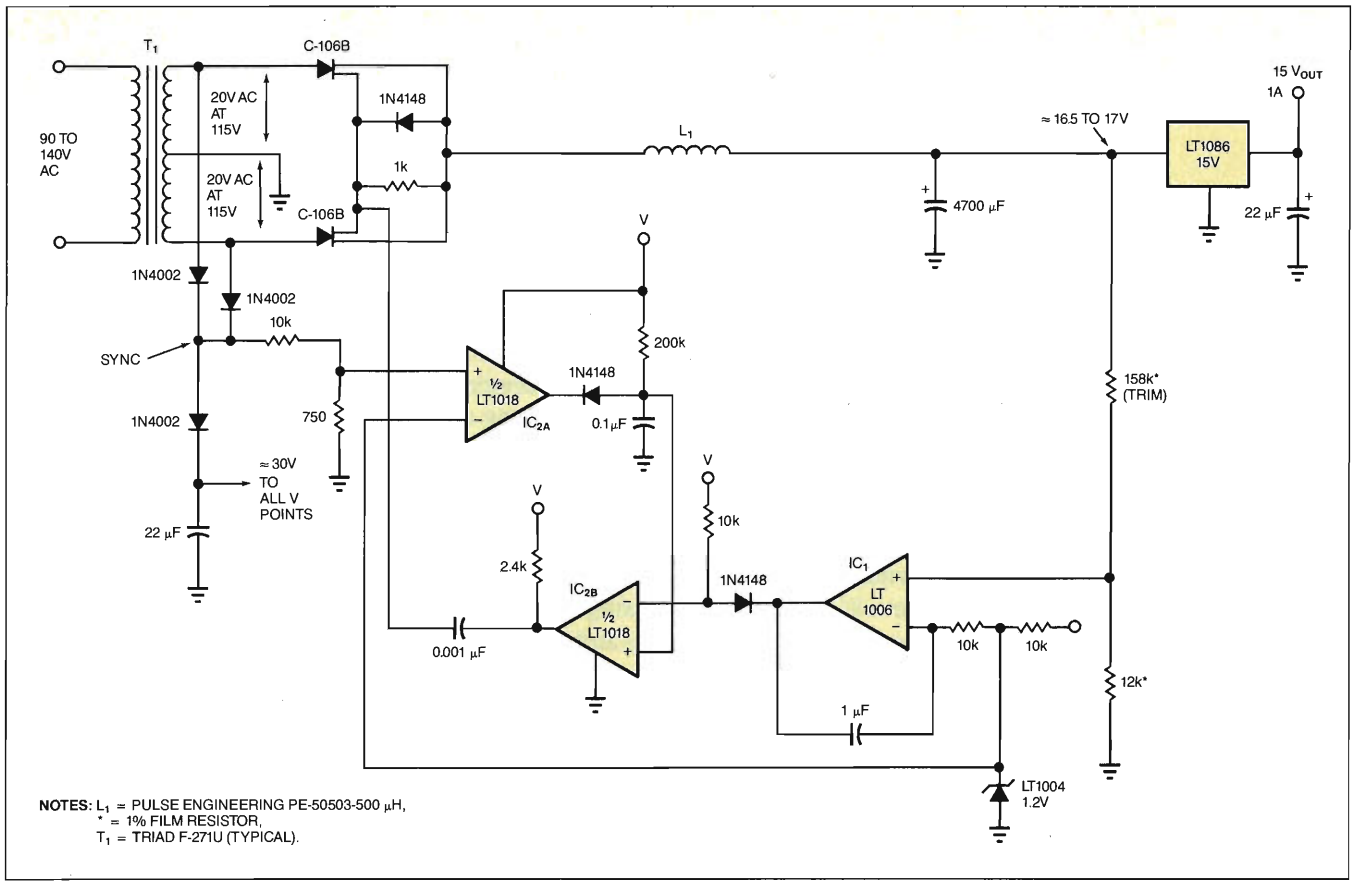

Fig 3—There are ways to eliminate regulator input variations, *even those with wide ac-line variations. This circuit provides high efficiency and retains all the desirable characteristics of linear regulators.*

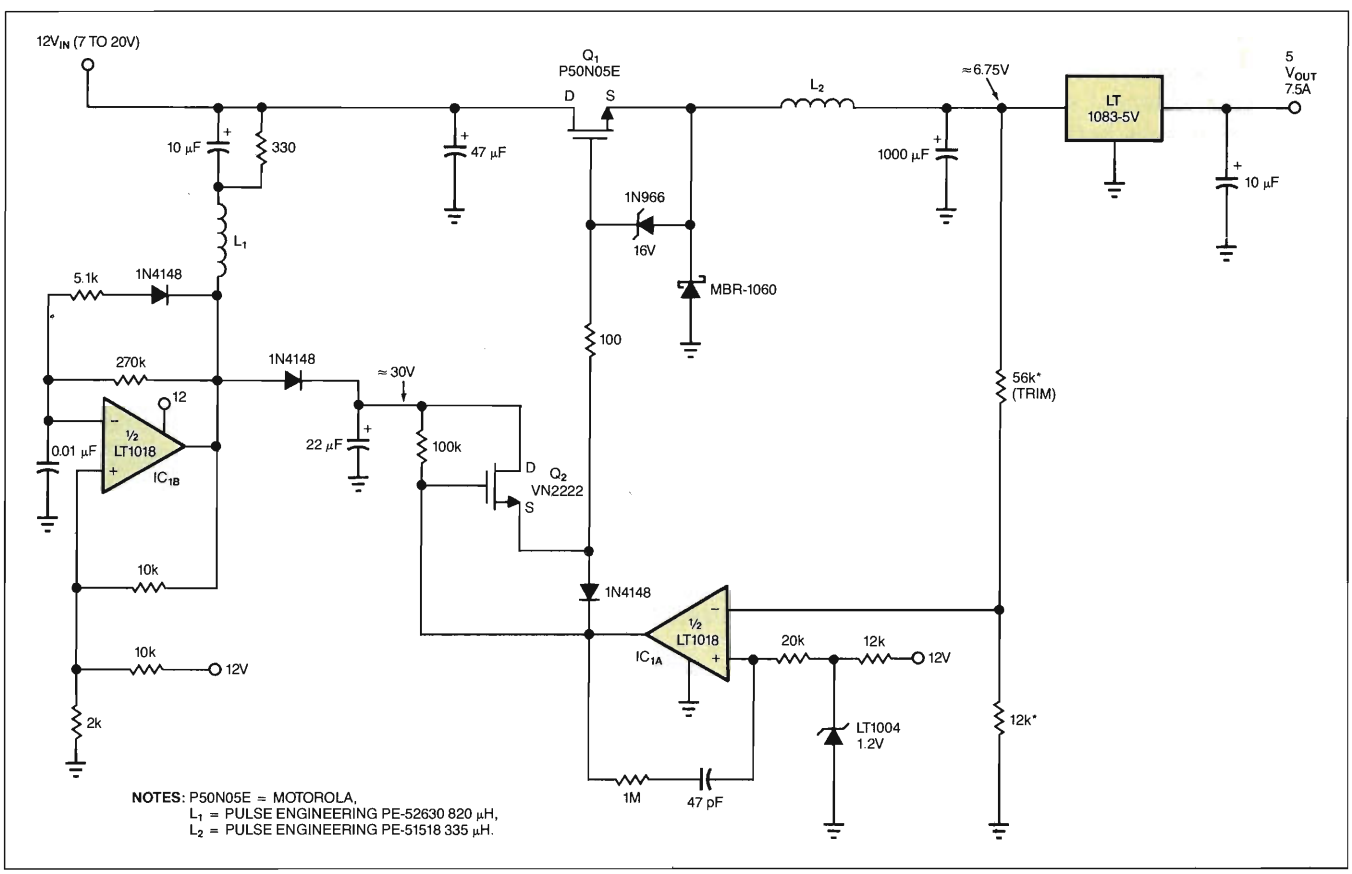

Fig 4—Designed for low losses at high currents, *this circuit is useful in applications involving dc inputs. The LT1083 functions normally; the remaining components form a switched-mode dissipation regulator.*

Wide voltage variations on the ac-line input have a deleterious effect on regulator efficiency.

the next half-cycle, the process repeats with the alternate SCR doing the work. The loop phase modulates the SCR's firing point to maintain a constant LT1086 input voltage.

The 1-μF capacitor around IC_1 compensates the loop, and the 10-kΩ resistor at IC_1's output ensures circuit startup. The 3-terminal regulator's current limit protects the circuit from overloads. This circuit has a dramatic impact on LT1086 efficiency versus ac-line swing. An important note here. The transformer in a preregulator can significantly influence the circuit's overall efficiency. One way to evaluate power consumption is to measure the actual power taken from the ac line.

Fig 4's circuit is useful when an application involves dc inputs—a regulated or unregulated power supply or a battery. This circuit features low losses at high current levels. The LT1083 functions in a conventional fashion, supplying a regulated output at 7.5A max. The remaining components form a switched-mode dissipation regulator, which maintains the LT1083 input level just above the dropout voltage under all conditions.

When the LT1083 input decays enough, IC_{1A}'s output goes high and increases the voltage on Q_1's gate. This rising voltage turns on Q_1, which drives current into L_2 and the 1000-μF capacitor and raises the input voltage at the LT1083 regulator. When the regulator input rises far enough, IC_{1A}'s output goes low, which turns

Achieving a low dropout voltage

Linear voltage regulators almost always use the design illustrated in **Fig A** for the basic regulating loop. The on-impedance limits of the pass element in the circuit establish the dropout voltage. The ideal pass element should have zero impedance between the input and the output and consume no drive energy.

Different pass elements offer different tradeoffs and advantages in establishing low dropout. Three are illustrated in **Fig B.** Emitter followers for transistors and source followers for MOSFETs offer current gain and easy loop compensation because the voltage gain is less than unity. They also transfer the drive current to the load. Unfortunately, you have to provide a voltage overdrive at the input to saturate a follower. Since V_{IN} must supply the drive, achieving overdrive is not an easy task. Practical regulator circuits must either generate the overdrive or obtain it from another source. You can easily generate overdrive in discrete regulator designs, but it's hard to do so with an IC power regulator.

Without voltage overdrive, the saturation loss is set by V_{BE} for bipolar transistors and by the channel on-resistance for MOSFETs. The on-resistance of a MOSFET varies considerably without overdrive, but bipolar losses are more predictable. Note that voltage losses in the drive stages add directly to the dropout voltage parameter. The follower output used in conventional 3-terminal IC regulators combines with the drive-stage loss to set the dropout at 3V.

Common-emitter configurations for transistors and common-source configurations for MOSFETs are another pass-element option. With bipolar devices, the common-emitter scheme removes the V_{BE} loss contribution. It's quite easy to saturate a pnp common-emitter driver, even in IC form. The tradeoff here is that the base current never gets to the load—a situation that wastes substantial power. At higher current levels, base drive current losses can negate a common emitter's saturation advantage. This is a particular problem in IC regulators, where the use of high-beta, high-current pnp transistors is not practical. At moderate current levels, pnp common-emitter drive stages are practical for IC-type regulators—the LT1020 and LT1120 use this approach.

Common-source, p-channel MOSFET configurations don't suffer from the drive-loss problems of bipolars but typically require 10V of gate-to-channel bias to fully saturate. In low-voltage applications, you have to generate negative potentials to satisfy the bias needs. P-channel devices also have poorer saturation characteristics than equivalent-size n-channel devices. The voltage gain available in common-emitter and common-source configurations creates some loop stability concerns, but these concerns are easy to handle.

Compound connections using a pnp-driven npn transistor are a reasonable pass-element compromise, particularly for IC-regulator devices with currents greater than 250 mA. With a compound

off Q_1 and terminates capacitor charging. The MBR-1060 damps L_2's flyback spike, and the 1-MΩ/47-pF combination sets loop hysteresis at about 100 mV.

Q_1, an n-channel MOSFET, has a saturation loss of only 0.028Ω but requires a 10V gate-to-source turn-on bias. IC_{1B} is set up as a simple flyback-voltage booster to provide about 30V of dc boost for Q_2. Q_2 serves as a high-voltage pullup for IC_{1A} to provide voltage overdrive to Q_1's gate. This overdrive ensures Q_1's saturation, even though Q_1 is configured as a source follower.

The 1N966 zener diode clamps excessive gate-source overdrives. These measures are necessary because there are no viable alternatives—low-loss, p-channel MOSFET devices aren't available, and bipolar approaches require excessive drive currents or have poor saturation characteristics.

Satisfy ultralow dropout needs

In some applications, extremely low dropout is a primary design target. The circuit in **Fig 5** is substantially more complex than a 3-terminal regulator design, but it features a 400-mV dropout level at an output of 10A. This circuit uses the same overdriven-source-follower technique employed in **Fig 4** to significantly lower saturation resistance.

The LT1072 switching regulator, set up as a flyback converter, generates Q_1's gate-boost voltage. This 30V boost voltage drives IC_{1A}. IC_{1A} compares the circuit connection, the tradeoff between the pnp V_{CE} saturation term and the reduced drive losses compared with a straight pnp is favorable. Also, the major current flow is through a power npn—a configuration that's easy to achieve in monolithic form. The compound connection has voltage gain, so you have to pay attention to loop frequency compensation. LT1083-6 regulators use the compound connection for a pass scheme and employ a capacitor at the output to provide loop compensation.

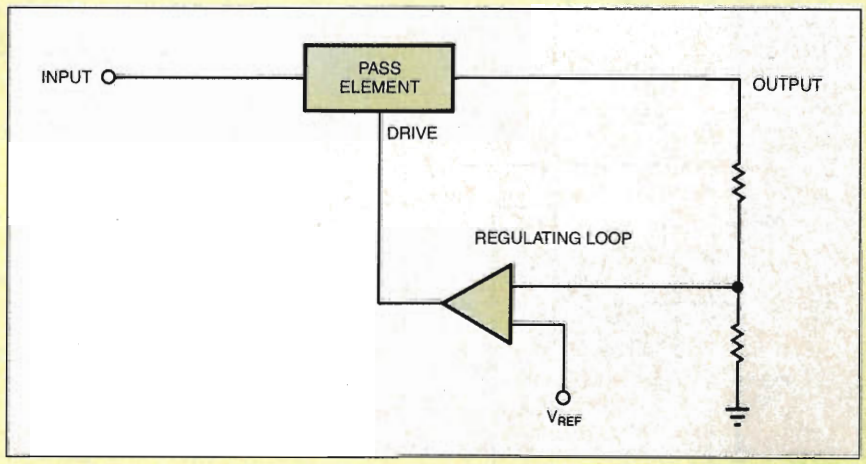

***Fig A—Dropout-voltage limitations are controlled** by the pass elements used in this basic regulating loop, which is used in just about all linear regulators.*

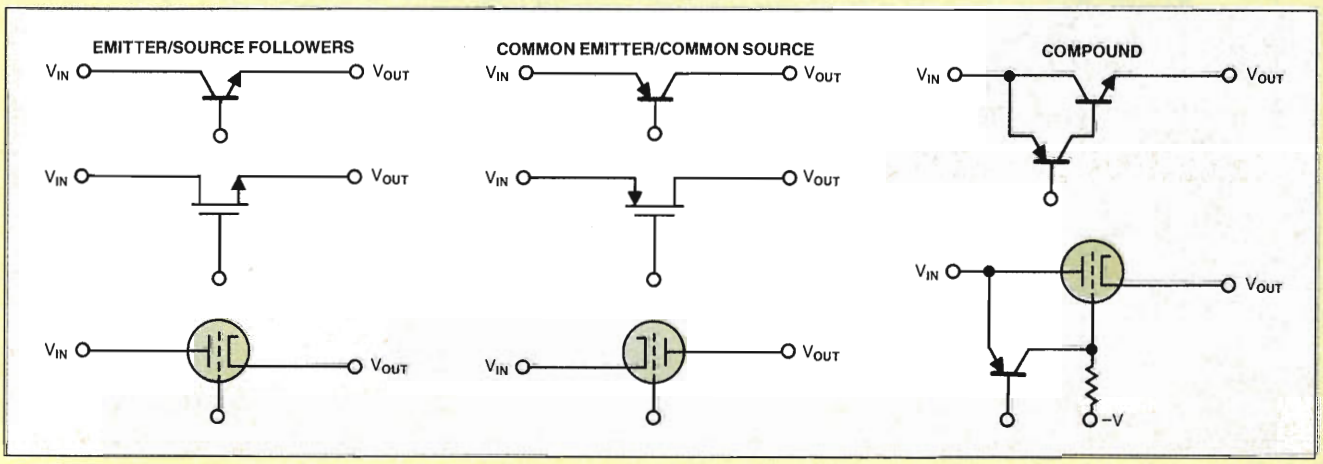

***Fig B—These three pass elements** offer various tradeoffs and advantages in achieving low dropout-voltage figures.*

Power-type regulators can also benefit from low-dropout design techniques.

output to the LT1004 reference and servo controls Q_1's gate to close the loop.

The gate-voltage overdrive provides the low-dropout characteristic for this regualtor by enabling Q_1 to attain a 0.028Ω saturation level. The 1N966 zener diode clamps excessive gate-source voltage, and the 0.001-μF capacitor stabilizes the loop. IC_{1B} senses current across the 0.01Ω shunt to provide current limiting by forcing IC_{1A}'s inverting input to swing negatively. The low-resistance shunt limits loss to only 100 mV at 10A outputs. Circuit roll-off is smooth and evidences no oscillation or undesirable characteristics.

Fig 6 combines the best features of the previous designs to develop a regulator that features high efficiency at high power levels. This circuit combines **Fig 4**'s preregulator techniques with the low-dropout design feature of **Fig 5.** There are, of course, some modifications.

For example, there is no boost supply for the linear regulator, and the 1N967A has a slightly higher zener voltage than the 1N966 in **Fig 5.** In addition, a single 1.2V reference serves the needs of both the preregulator and the linear-output regulator. The increase in zener-clamp values ensures adequate boost voltage lev-

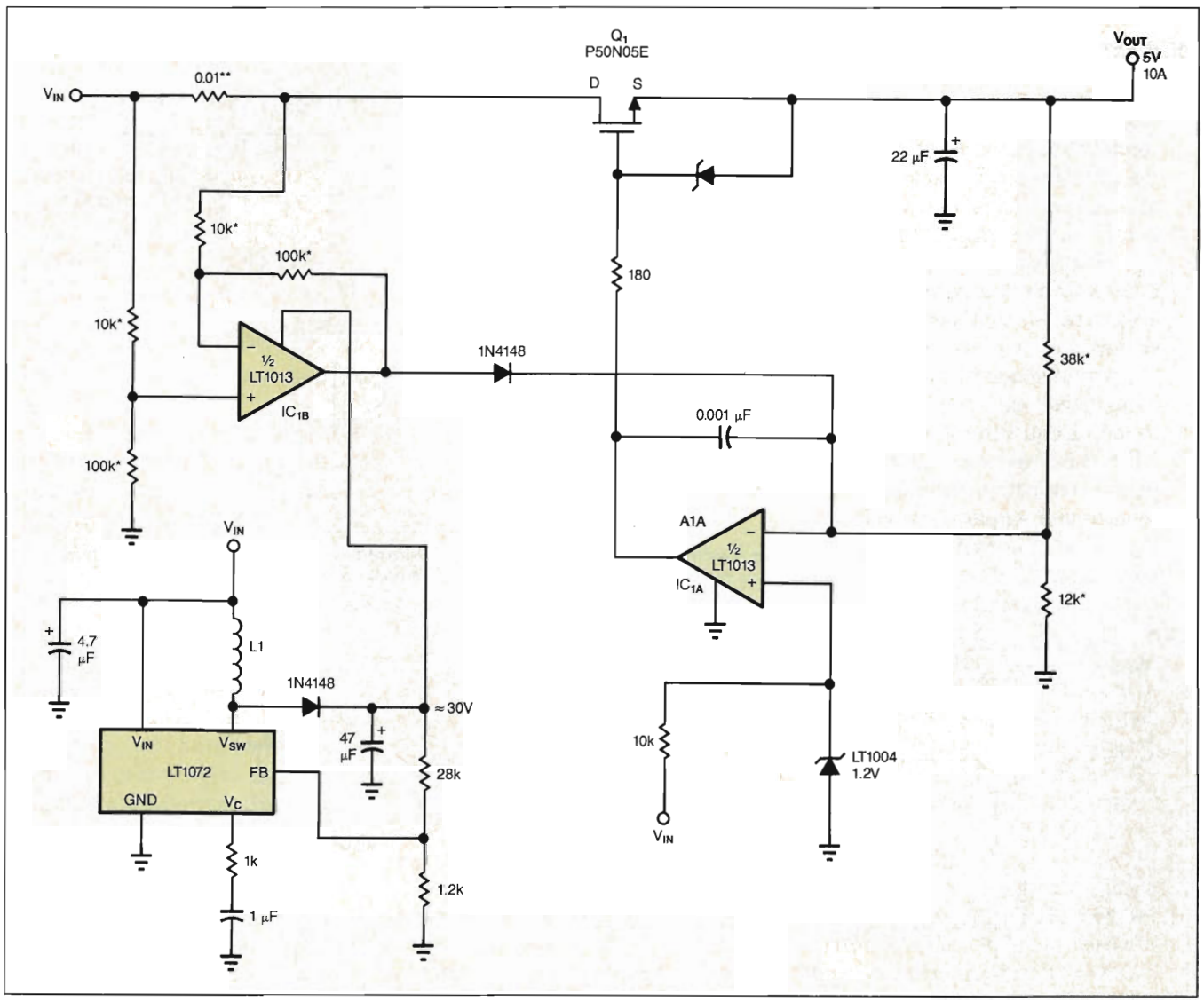

Fig 5—Extremely low saturation resistance *is a key benefit provided by the source-follower techniques employed in this regulator. Although it's somewhat complex, the design features a 400-mV dropout voltage at 10A output levels.*

els for low-voltage input conditions. The preregulator's feedback resistors set the linear regulator's input voltage just above its 400-mV dropout level.

Although **Fig 6**'s circuit is complex, its performance is impressive. The circuit's efficiency is 86% at a 1A output level and decreases to 76% at full load. Circuit losses are essentially shared by the MOSFETs and the MBR1060 catch diode. You can improve efficiency by 3 to 5% by replacing the catch diode with a synchronously switched FET and trimming the linear regulator's input to the lowest possible dropout value.

Power linear regulators are not the only circuits that can benefit from the above techniques. **Fig 7**'s preregulated micropower linear regulator features excellent efficiency and low noise. A drop at the preregulator's output—pin 3 of the LT1020 regulator—causes the LT1020's comparator to go high. This transition switches the 74C04 inverter chain and biases the p-channel MOSFET on, thus allowing current to flow through the inductor. When the voltage at the junction of the inductor and the 220-μF capacitor gets high enough, the comparator output goes low and turns off the MOSFET's current flow. This loop action regulates the LT1020's input pin at a value established by the

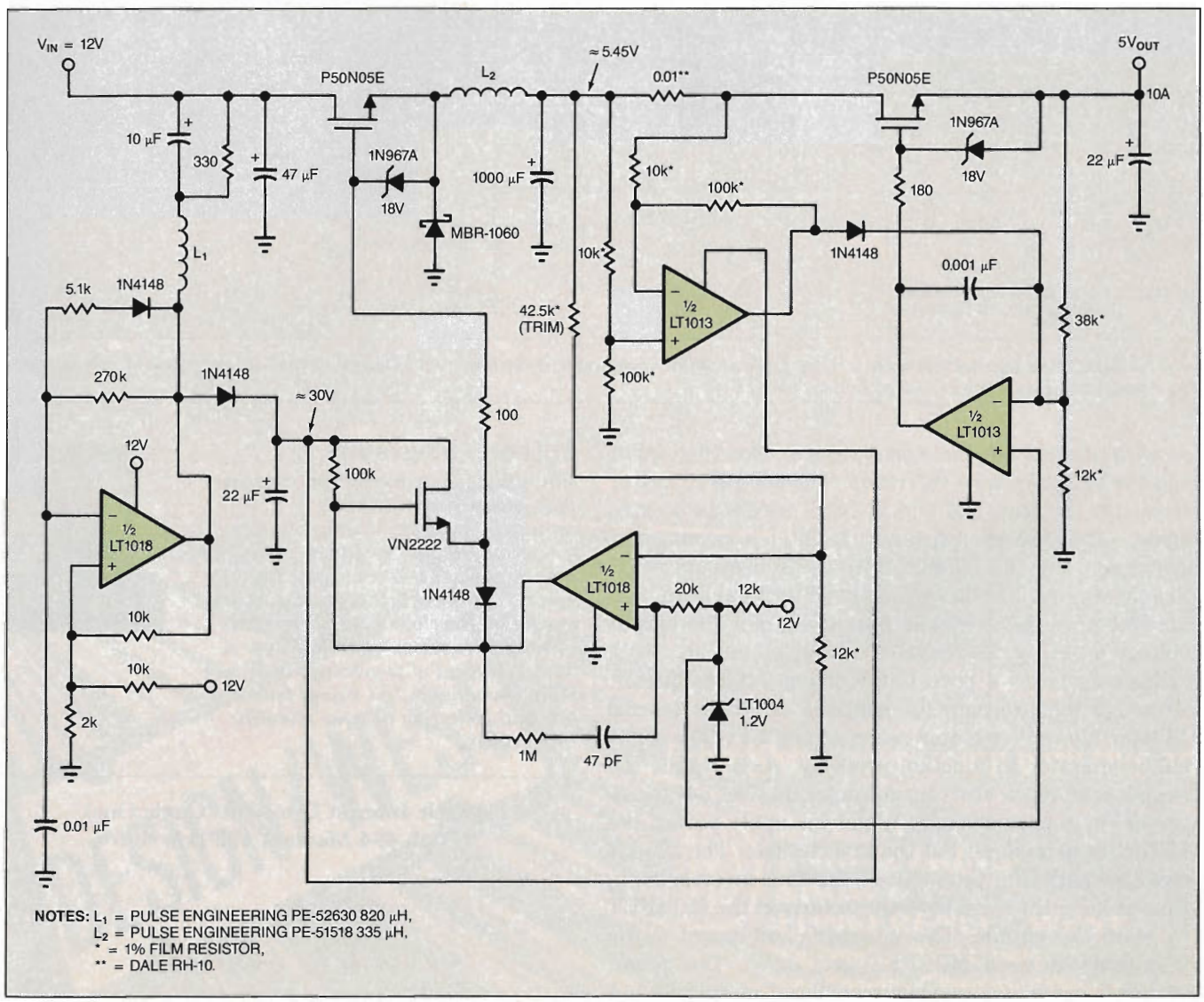

Fig 6—To achieve highly efficient linear regulation, *this circuit combines a preregulator with a low-dropout regulator design. The circuit's efficiency is 86% for 1A outputs and 76% at full load.*

The on-impedance limitations of regulator pass elements determine dropout-voltage figures.

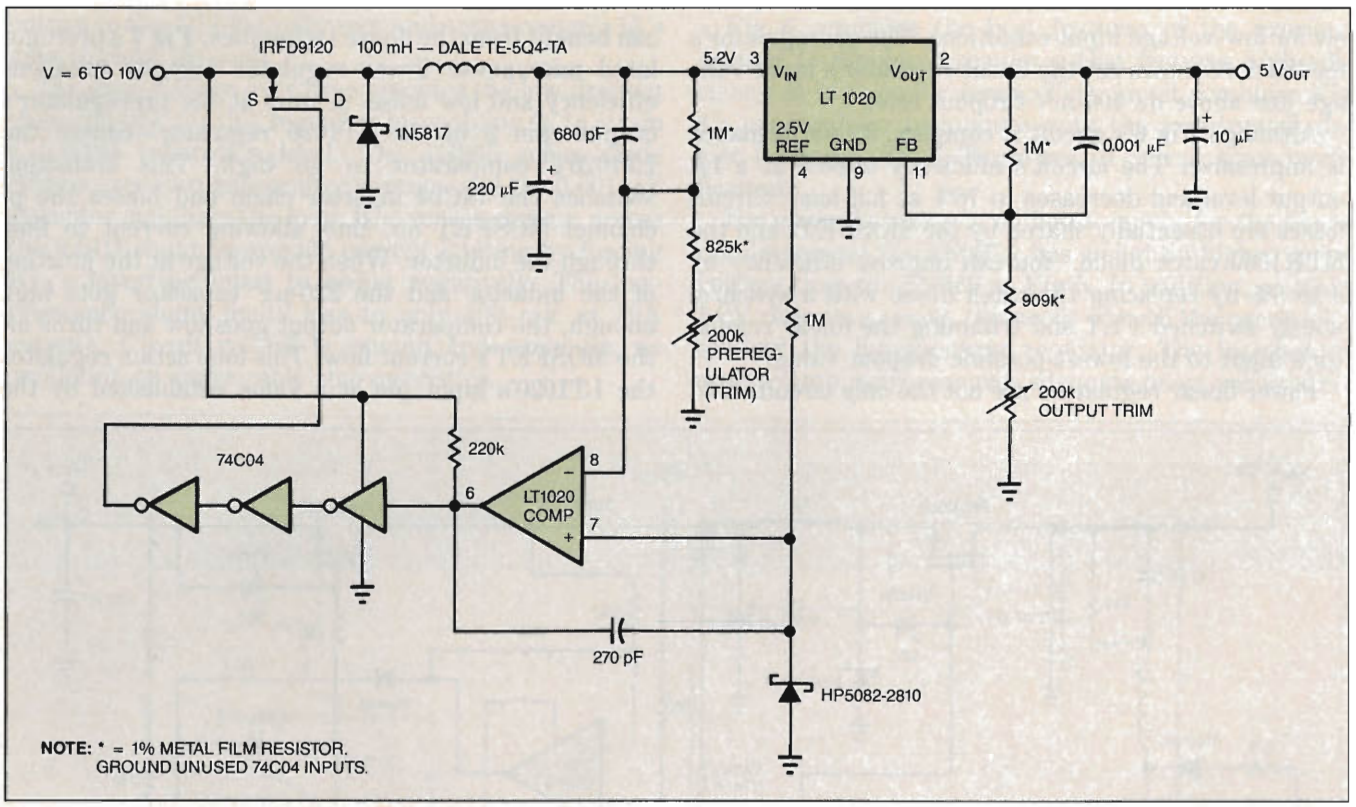

Fig 7—High efficiency and low noise *are key features of this micropower regulator circuit. Despite its low, 40-µA quiescent current drain, the circuit can achieve efficiencies exceeding 80%.*

resistor divider at the comparator's inverting input and the LT1020's 2.5V reference. The 680-pF capacitor stabilizes the loop and the 1N5817 serves as a catch diode. The 270-pF capacitor facilitates comparator switching, and the HP5082-2810 diode prevents negative overdrives. The low-dropout LT1020 linear regulator smoothes the switched output signal. The output voltage is set by the resistive divider on pin 11.

Start-up poses a potential problem for this circuit. Although the preregulator supplies the input for the LT1020, the preregulator relies on the LT1020's internal comparator to function properly. As a result, the circuit requires a start-up mechanism. The 74C04 inverter chain provides one. When you apply power, the LT1020 sees no input but the inverters do. The 220-kΩ resistive path lifts the input of the first inverter high, thus causing the third inverter to turn on the MOSFET to start the circuit. The inverter's rail-to-rail swing also provides good MOSFET grid drive. The circuit in **Fig 7** has a quiescent current level of only 40 µA and achieves efficiencies in excess of 80% at output levels as high as 50 mA. EDN

Author's biography

Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art, and collecting antique scientific instruments.